

EIA/JEDEC PUBLICATION

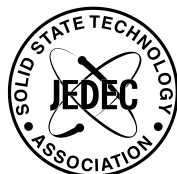
Signature Analysis

JEP136

JULY 1999

ELECTRONIC INDUSTRIES ALLIANCE

JEDEC Solid State Technology Association



NOTICE

EIA/JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

EIA/JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

EIA/JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the EIA/JEDEC standards or publications.

The information included in EIA/JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an EIA/JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this EIA/JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
©ELECTRONIC INDUSTRIES ALLIANCE 1999
Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201-3834

This document may be downloaded free of charge, however EIA retains the copyright on this material. By downloading this file the individual agrees not to charge or resell the resulting material.

**PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering
Documents, USA and Canada (1-800-854-7179), International (303-397-7956)**

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by the Electronic Industries Alliance and may not be reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

SIGNATURE ANALYSIS

CONTENTS

	Page
1 Introduction	1
2 Purpose	2
3 Scope	2
4 Definitions	3
5 Signature analysis procedure for an ongoing process	3
5.1 Overview	3
5.2 SA process flow	4
5.3 Signature analysis definition phase	4
5.4 SA validation	5
5.5 Revalidation	5
6 Signature analysis procedure for a finite population	5
7 Examples	6
7.1 Finite population case	6
7.2 Ongoing process	6
Annex A An approach of signature analysis risk assessment procedures for an ongoing process	7
A.1 Statistical terms and variables	7
A.2 Statistical derivation of an estimate for θ	8
A.3 Statistical derivation of confidence intervals for θ_A	9
Annex B An approach to signature analysis risk assessment procedures for a finite population	11
Annex C An approach to signature analysis risk assessment procedures for a process with correlated failures	13
C.1 Statistical terms and definitions	13

SIGNATURE ANALYSIS

(From JEDEC Board Ballot JCB-98-124, formulated under the cognizance of the 14.6 Committee on Failure Analysis.)

1 Introduction

Device Analysis is a limited resource that should be targeted at solving unknown problems, rather than analyzing repetitive failures. Signature Analysis (SA) is a lab resource management tool in that it provides a formal method of reducing the number of these repetitive failures requiring full analysis. Two statistical models are presented, both of which assign a confidence level to any number of units with the same failure characteristics (i.e., signature) and same failure mechanism, allowing the statement “I am A% sure that greater than B% of other parts with this signature will also have this failure mechanism”. One model is for use when the failing population size is finite and known, and will be referred to as ‘finite population analysis’ (FPA). It would be used, for example, to define the sampling plan for a low yielding wafer lot, i.e., to determine how many failing dice from each failure category must be fully analyzed in order to infer information about that whole wafer lot. The other model, referred to as ‘ongoing process analysis’ (OPA) assumes the population of future fails is unknown or infinite, and would be used to infer information about failures collected over time from multiple events, lots or labs. The use of two models also allows us to build-in the engineering bias that we would expect higher confidence levels when we do failure analysis by inference on finite population failures, than on ones collected over time.

The backlog of analysis labs often includes device failures for which both the product engineer and analyst ‘know’ what will be found during analysis. However, corporate specifications and/or customer requirements often dictate that the analysis be performed anyway. There is a need to be able to assign a failure mechanism (with a statistically determined confidence level) to devices that are analyzed by inference to historical data.

There is a desire to promote a common definition of this system of analysis by inference, using the same statistical techniques, and to recognize that it is a formal means of doing failure analysis.