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Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)

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PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)

(From JEDEC Board Ballot JCB-03-43, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This procedure is intended for VNA (Vector Network Analyzer) based measurement of pin input capacitance for devices with SSTL (Stub Series Terminated Logic) interface . This procedure does not mandate a specific method for measuring input capacitance. It has only to be considered mandatory if it is explicitly referred to by a component specification in conjunction with a value of an input capacitance defined in such a specification.

The procedure outlined below

- ... was written having DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) devices in mind.
- ... is expected to yield an accuracy of 10% (or 100 fF, whichever is greater) and a accuracy of 10% (or 50 fF, whichever is greater) for measuring capacitance differences (C_{Δ}).
- ... ignores (in its simplified version) the error introduced by the inductance of the test fixture.
- ... ignores the inductance of the input pin.
- ... is intended for application frequencies < 200 MHz; pin inductance < 7 nH and input capacitance $C_{in} > 1$ pF.
- ... allows S-parameter based de-embedding of the test fixture, if those parameters are known.
- ... may be applied to interfaces other than SSTL.

2 Equipment requirements and preparation

2.1 Required hardware

- Vector Network Analyzer (e.g. Agilent 8753ES or equivalent) with minimum bandwidth of 3 GHz.
- Microwave probes (DC to 40 GHz, (G,S) or (S,G) footprint, 3.5 mm connector compatible, low-loss coaxial technique). Probe needs to support SOL (Short, Open, Load) calibration.