

JEDEC PUBLICATION

Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface- Mount Components

JEP150.01

(Minor revision of JEP150, May 2005, Reaffirmed JUNE 2011)

JUNE 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by
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Introduction

The present solid state component level qualification procedures do not always ensure that the packaged component will operate reliably after assembly on printed wire boards (PWBs), or the like, since the free standing device level qualification may not induce the same thermomechanical stresses present in the post second level assembly state. As component interconnections decrease in size, e.g., the component is closer to the PWB; the interaction of the second level assembly becomes increasingly more likely on the component's performance. This document demonstrates how to evaluate the effect of assembly level operations and structures on components. As such, this document pertains predominantly to the following set of solid state devices and component packages that are described in the Scope. Knowledge of and comparison with packaged component failure mechanisms and modes is needed between the free standing and the assembled state. To ensure an effective qualification methodology for this set of solid state surface-mounted components, testing shall be performed in both the free standing and assembled state, including attached heat sinks where applicable. It should be noted that peripheral leaded surface-mount components are not considered in this document because, in general, the thermomechanical stresses imparted to the component in its assembled state are minimal, due to the inherent flexibility of their leads.

Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components

(From JEDEC Board Ballot, JCB-05-56, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, in particular leadless chip carriers, ball grid array (BGA) packages, direct chip attach die and packages with exposed pads that are attached to the PWB for thermal considerations. Assembly level testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the component is not known, there could be reliability concerns for that component that are not evident in component level testing. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that component due to its assembly to a PWB.

These reliability stress tests have been found capable of stimulating and precipitating failures in assembled components in an accelerated manner, but these tests should not be used indiscriminately. Each qualification should be examined for:

- a) Any potential new and unique failure mechanisms.
- b) Any situation where these tests and/or conditions may induce false failures.

In either case the set of reliability requirements, tests and/or conditions should be appropriately modified to properly comprehend the new situations.

This document does not relieve the supplier of the responsibility to meet internal or customer specified qualification programs.

2 Terms and definitions

second level assembly: The attachment of a component to the next level of assembly packaging.

packaged device: A semiconductor device within an enclosure that allows electrical connection to and provides mechanical and environmental protection for that device.

free-standing state (of a component): The state of a component that is not attached to the next level of assembly packaging.

assembled state (of a component): The state of a component that has been attached to a second level assembly.

2 Terms and definitions (cont'd)

chip package interaction (CPI): The interaction between the semiconductor package stresses and the semiconductor device.

peripheral-leaded surface-mount component: A component with a metal frame that provides external surface-mountable terminals located around the periphery of the body of the component.

3 Reference Documents

JEP122, “Failure Mechanisms and Models for Silicon Semiconductor Devices”

JESD74, “Early Life Failure Rate Calculation Procedure for Electronic Components”

JESD85, “Calculation of Failure Rate in Units of FITs”

JESD91, “Method for Developing Acceleration Models for Electronic Component Failure Mechanisms”

JESD94, “Application Specific Qualification using Knowledge Based Test Methodology”

JESD22, “Reliability Test Methods for Packaged Devices”

JEP131, “Process Failure Modes and Effect Analysis (FMEA)”

JESD47, “Failure Mechanisms and Models for Silicon Semiconductor Devices”

IPC/JEDEC 9702, “Monotonic Bend Characterization of Board-Level Interconnects”

IPC 9701, “Solder Joint Reliability Test Method”

SEMATECH White Paper #99083810A-XFR, “Use Condition Based Reliability Evaluation of New Semiconductor Technologies”

SEMATECH White Paper #99083813A-XFR, “Use Condition Based Reliability Evaluation: An Example Applied to Ball Grid Array (BGA) Packages”

4 Understanding stress interactions

The apparent stresses and distribution of stresses imparted to the solid state component during free-standing component qualification testing may not match the actual stresses and associated distribution that the component will be subjected to when surface mounted on a printed wiring board (PWB). Failure modes may also be different. Figure 1 shows the various interactions that exist between the packaged device and its free-standing and assembled state that can affect the component’s reliability in the final field application.

Area 1 in Figure 1 refers to the reliability of the free-standing component prior to assembly to a PWB. Qualification procedures have been established for components, see JESD47 (Stress Test Driven Methodology) and JESD94 (Application Specific Qualification using Knowledge Based Test Methodology).