

JEDEC PUBLICATION

Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface- Mount Devices

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STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH ASSEMBLED SOLID STATE SURFACE-MOUNT DEVICES

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STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH ASSEMBLED SOLID STATE SURFACE-MOUNT DEVICES

Introduction

The present solid state device level qualification procedures do not always ensure that the packaged device will operate reliably after assembly on printed wiring boards (PWBs), or the like, since the free-standing device level qualification may not induce the same thermomechanical stresses present in the post second level assembly state. This document demonstrates how to evaluate the effect of assembly level operations and structures on devices. As such, this document pertains predominantly to the set of solid state devices and device packages that are described in the Scope. Knowledge of and comparison with packaged device failure mechanisms and modes is needed between the free standing and the assembled state. To ensure an effective qualification methodology for this set of solid state surface-mounted devices, reliability testing should be performed in both the free standing and assembled state, including attached heat sinks where applicable. It should be noted that devices in peripheral-leaded surface-mount packages (PQFP, TQFP, ceramic QFP, etc.,) are not considered in this document because, in general, the thermomechanical stresses imparted to the device in its assembled state are minimal, due to the inherent flexibility of the package leads.

STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH ASSEMBLED SOLID STATE SURFACE-MOUNT DEVICES

(From JEDEC Board Ballot, JCB-23-42, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

The electronics industry has qualification standards for loose devices (e.g., JESD47, JESD94), printed wiring boards (PWBs) (e.g., IPC standards), and 2nd level interconnect reliability (i.e., solder joints) (e.g., IPC standards) that are performed as separate activities. This publication only addresses evaluating the intersection of how the stress state within a device may be altered once it is attached to a PWB, it does not address 2nd level interconnect reliability. This publication proposes a methodology on how to assess a device in package type whose stress state is susceptible to being altered once attached to a PWB. The severity or location of a failure mechanism and/or its time to failure may be altered from testing the device in the free-standing state versus testing in the assembled state.

This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, that are in packages whose construction is such that when mounted to a PWB the stress state in the package may be significantly different from when stressed in a free-standing state. Such packages may include but are not limited to leadless chip carriers (e.g., OFN), ball grid array (BGA) packages, and packages with exposed pads that are attached to the PWB for thermal considerations. New package constructions should also be assessed as there does not exist historical knowledge of how the package stress state may be altered when tested in the assembled state. These could include fan out wafer level packages (FOWLP) and wafer level chip scale packages (WLCSP).

Assembled state testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the device is not known, there could be reliability concerns for that device that are not evident in device level testing. Clause 4 describes the relationship between device level, PWB level, assembly level qualification testing in more detail and Clause 5 describes when assembly level qualification testing may be required. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that device due to its assembly to a PWB. Clause 8 provides guidance on the PWB to be used for the assembly level testing.

These reliability stress tests have been found capable of stimulating and precipitating failures in assembled devices in an accelerated manner, but these tests should not be used indiscriminately. Each qualification should be examined for:

- a) Any potential new and unique failure mechanisms.
- b) Any situation where these tests and/or conditions may induce false failures.

In either case the set of reliability requirements, tests and/or conditions should be appropriately modified to properly comprehend the new situations.

This document does not relieve the supplier of the responsibility to meet internal or customer specified qualification programs.

2 Terms and Definitions

second level assembly: The attachment of a device to the next level of assembly packaging.

packaged device: A semiconductor device within an enclosure that allows electrical connection to and provides mechanical and environmental protection for that device.

free-standing state (of a device): The state of a device that is not attached to the next level of assembly. For example: a packaged die, such as a flip chip BGA, bumped die, QFN, etc., that is not connected to the next level of assembly, such as a PWB, module, etc.

NOTE See Figure 1, Area 1.

assembled state (of a device): The state of a device that has been attached to the next assembly level. For example: a packaged die connected to a PWB, module, etc.

NOTE See Figure 1, the intersection of Area 1 and Area 3.

chip package interaction (CPI): The interaction between the semiconductor package stresses and the semiconductor device.

peripheral-leaded surface-mount device: A device with a metal frame that provides external surface-mountable terminals located around the periphery of the body of the device.

3 Reference Documents

IPC 9701, “*Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*”

IPC/JEDEC 9702, “*Monotonic Bend Characterization of Board-Level Interconnects*”

IPC/JEDEC-9706, “*Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection*”

JEP122, “*Failure Mechanisms and Models for Silicon Semiconductor Devices*”

JEP131, “*Potential Failure Mode and Effects Analysis (FMEA)*”

JEP154, “*Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress*”

JESD22, “*Reliability Test Methods for Packaged Devices*”

JESD47, “*Stress-Test-Driven Qualification of Integrated Circuits*”

JESD61, “*Isothermal Electromigration Test Procedure*”

JESD74, “*Early Life Failure Rate Calculation Procedure for Electronic Components*”

JESD85, “*Methods for Calculating Failure Rate in Units of FITs*”

JESD91, “*Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*”

JESD94, “*Application Specific Qualification using Knowledge Based Test Methodology*”

JESD202, “*Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress*”

4 Understanding Stress Interactions

The apparent stresses and distribution of stresses imparted to the solid state device during free-standing device qualification testing may not match the actual stresses and associated stress distribution that the device will be subjected to when surface mounted on a printed wiring board (PWB). Failure modes may also be different. Figure 1 shows the various interactions that exist between the packaged device and its free-standing and assembled state that can affect the device's reliability in the final field application.

Area 1 in Figure 1 refers to the reliability of the free-standing device prior to assembly to a PWB. Qualification procedures have been established for devices, see JESD47 (Stress Test Driven Methodology) and JESD94 (Application Specific Qualification using Knowledge Based Test Methodology).

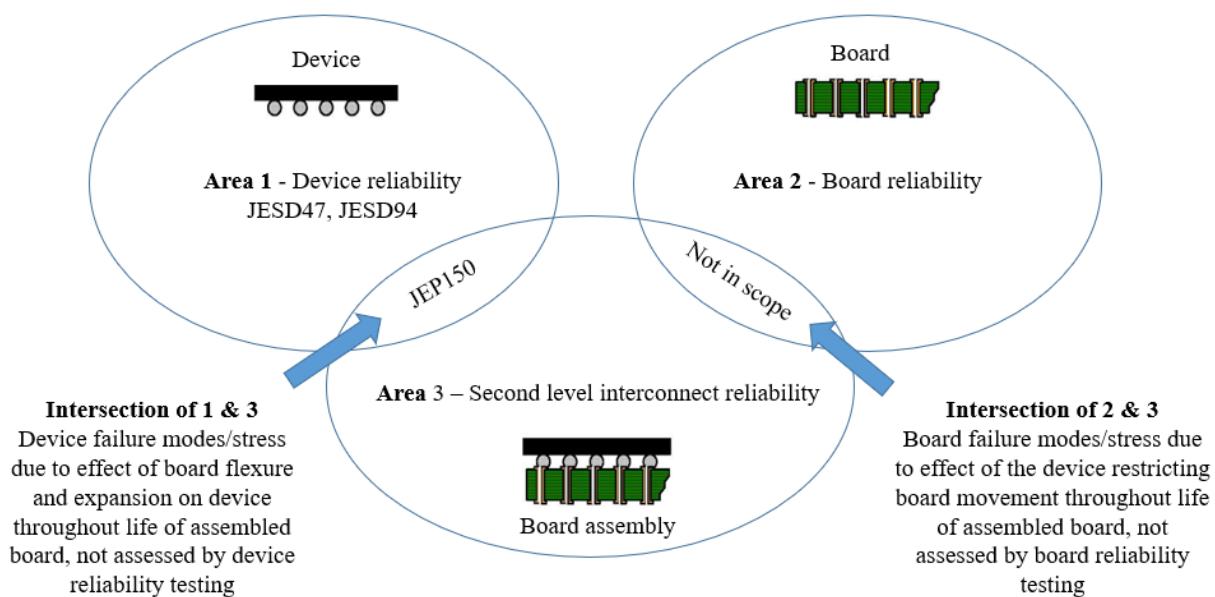


Figure 1 — Levels of Assembly - Interaction of Packaging Technical Concerns

When the device is assembled onto a printed wiring board (PWB), or the like, the assembly process can affect the reliability of the device by exposing it to new or altered assembly related stress levels and stress distributions as shown by the intersection of Area 1 and Area 3 in Figure 1. This is the primary focus in this document. The major concern is that the device, as assembled, will exhibit failure modes that were not detected during the qualification of the free-standing device. Failures can be found in the various areas of the device including the package materials, package circuitry and the silicon device due to chip to package interactions.

Example: A specific example of this is beam lead failures seen in micro BGA packages. The micro BGA package typically uses a highly compliant and low modulus elastomer to de-couple the die from the flex tape. Failures are generally not seen during the device level qualification. However, when the package is assembled on the next level, there is a shift in the composite coefficient of thermal expansion (CTE) of the assembled device. This mismatch drives stresses from the solder joints to the copper beam leads inside the package. This may result in beam lead failures, which can be detected during thermal cycling tests of the assembled device.