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Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress

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Introduction

Bump Electromigration Failure Mechanism

Electromigration of solder bumps is a failure mechanism that leads to increased resistance sometimes accompanied by events such as formation of intermetallic compounds (IMC), voids and cracks that can disrupt the solder joint and die and/or package metallization leading into the bump. The resistance increase can ultimately lead to an open circuit. The stress drivers for this failure mechanism are current density and elevated temperature. The failure mechanisms for bump electromigration can be varied and depend on the metals present both on the die side and the substrate side. The failure location is determined by electron flow which is set by the current flow which is in the opposite direction.

Model for Solder Bump Electromigration

Black's model (equation 1), which has been applied for many years to semiconductor die metallization, has also been applied to solder bump electromigration [1].

$$TTF \propto J^{-n} \exp\left(\frac{E_a}{kT}\right) \quad (1)$$

This equation contains a model parameter relating to temperature (T): the thermal activation energy, E_a . It also contains a model parameter relating to current density (J): the current density exponent, n . In order to verify that Black's model applies to the type of bump structures being tested, or to derive a new model, testing at multiple stress temperatures and current densities is needed. Extraction of these model parameters from the test results is addressed later in this publication.

Overview of the Test

The electromigration test described in this document is performed in an oven at constant temperature and with a constant current source. The resistance of the bump electromigration structure (EM device) is measured using a 4-point measurement technique with the measurement points as close to the bump as possible. The EM device is considered to have failed when its resistance change (either absolute value or percent increase) reaches a predetermined value. The test is ideally continued until most of the test structures have met the predetermined failure criterion. The test structure may consist of a single bump or a chain of bumps.

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GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS

(From JEDEC Board Ballot JCB-23-57, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This document describes a method to test the electromigration (EM) susceptibility of solder bumps, including other types of bumps, such as solder capped copper pillars, used in flip-chip packages. The method is valid for Sn/Pb eutectic, high Pb, and Pb-free solder bumps. The document discusses the advantages and concerns associated with EM testing, as well as options for data analysis. The tests are performed on packaged bump electromigration test devices (EM devices). The bump electromigration test techniques described in this document can be used to assess the electromigration reliability of different types of solder bumps and metallizations, to make materials decisions, and to establish maximum bump current specifications. Thermal migration is also known to exist but is outside the scope of this document.

2 Normative References

JEP153 - Characterization and Monitoring of Thermal Stress Test Oven Temperatures

JESD22-B113 - Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

JESD33 - Standard Method of Measuring and Using Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line

3 Terms and Definitions

For the purpose of this standard, the following terms and definitions apply.

anode: A circuit element to which positive bias is applied.

NOTE For the purpose of this document, when the die is the anode the electron flow is from the substrate through the solder bump to the die and the current flow is in the opposite direction.

cathode: A circuit element to which negative bias is applied.

NOTE For the purpose of this document, when the die is the cathode the electron flow is from the die through the solder bump to the substrate and the current flow is in the opposite direction.

censored data: A set of data for which a portion of the test samples had testing discontinued prior to failing or survived until the end of the test.

EM device: A device under stress and may contain multiple electromigration (EM) test structures.

3 Terms and Definitions (cont'd)

intermetallic compound (IMC): A substance formed when solder comes in contact with another metal at elevated temperature.

NOTE The IMC is composed of multiple constituents from the solder and the other metal. This material has unique mechanical and electrical properties, which are different from those of the initial solder and the other metallization.

modified daisy chain: A daisy chain designed to excite failures of only one polarity (electron flow direction) for bumps of interest in the chain.

NOTE A common design for a modified daisy chain is to have multiple bumps providing current to the bump of interest. See Figure 2 for an example.

simple daisy chain: A daisy chain consisting of a single series of bumps in a chain.

NOTE A current through the series of bumps will alternate in direction in successive bumps. The number of bumps where electrons flow out of the die and the number of bumps where electrons flow into the die are equal.

Solder bump: Solder containing interconnect; this includes Sn/Pb eutectic, high Pb, and Pb-free solder bumps as well as solder capped copper pillars.

NOTE The methods in this document may be used for performing electromigration testing of direct copper-to-copper bonding interconnect.

substrate, (package): A platform that mechanically supports a bumped die within a package and electrically connects the solder bump landing pads to external terminals, using;

1. layered dielectric materials and conductive traces, or
2. a metal leadframe.

suspended samples: Samples that had testing discontinued prior to failing or that survived until the end of the test.

under-bump metallization (UBM): A patterned, thin-film stack of material that provides 1) an electrical connection from the die to a solder bump; 2) a barrier function to limit unwanted diffusion from the bump to the die; and 3) a mechanical interconnection of the solder bump to the die through adhesion to the die passivation and attachment to a solder bump pad.

Wheatstone bridge: A 4-arm bridge forming a diamond, all of whose arms are predominantly resistive, with three resistors of known values in three of the arms and the unknown resistor in the fourth.

NOTE 1 A voltage source, e.g., a battery, is connected across two opposite points of the diamond and a current-detecting instrument (e.g., a galvanometer) is connected across the other two points. The values of one or two of the known resistors are varied until no current flows through the galvanometer. The bridge is then balanced and the value of the unknown resistor can be calculated in terms of the other three.

NOTE 2 A method using the Wheatstone bridge for monitoring resistance of solder bumps in electromigration tests has greater sensitivity to resistance change than other methods. Net resistance changes due to electromigration of only the solder bumps, excluding the Al or Cu traces, can be deduced by this method.

4 Test Structures

4.1 Materials and Process Factors

Bump electromigration is strongly dependent on several factors. These include the following:

- bump composition;
- bump fabrication method (e.g., electroplated, printed paste, or evaporated [2]);
- composition of the under bump metallization (UBM) on the die [3];
- the UBM layer thicknesses [4];
- the substrate type; and
- the substrate pre-solder layers, e.g., Ni/Au, Copper/Organic Solder Protect (OSP), Copper/Solder on Pad (SOP) and their thickness [5,6].

The semiconductor die metallization, passivation composition and test structure details, including via openings and design features, may also have a significant effect on Joule heating and current crowding. As such, it is very important that the test structure and materials accurately replicate the product design being assessed. If not, deviations from the product design need to be clearly described.

4.2 Bump Geometry and Structures

Bump geometry and structures can affect bump EM performance based on effects of current crowding. Important geometrical considerations in bump electromigration are: bump geometry (height, shape and diameter); UBM size; UBM stack composition and layer thicknesses; passivation type and opening dimension; the die top metal pad size and thickness; semiconductor die metallization and thickness into the bump structure; and substrate pad size and composition. For flipchip on leadframe structures the solder connection to the leadframe may not be uniform from one bump to the next, and thus this should be taken into account when determining test site bump geometry. As mentioned above, to accurately evaluate product, the test structure should reflect these key attributes. If this is not done, the parts under test may not accurately represent current density and current crowding considerations for that product. It should also be noted that the bump geometry and structure used in any specific test vehicle may not represent the current carrying capability of any other geometries or structures.

Due to its tetragonal crystal structure, it has been established that the diffusivities of typical barrier level metal materials like Cu and Ni in Sn are significantly higher/faster in the C-axis direction than for the other axes [7, 8]. Because of that, Sn grain orientation can play a significant role in any diffusion driven mechanisms, and electromigration test results can be directly impacted by the grain orientation(s) of the solder structures under test. This has been clearly demonstrated for a Sn based Pb free solder system [9] and makes clear that an understanding of the grain orientations involved in producing electromigration failures is key.

Although a desired goal, it is not possible to control the grain orientation of an array of solder bumps when attaching a flip chip die to a carrier, and so the orientations found in an EM test sample will invariably contain a wide range of grain structures. Sampling multiple bumps within an array and evaluating multiple samples within an EM study, with the expectation of evaluating a range of different grain orientations, is very necessary since EM results will vary with the grain structures involved. It is strongly recommended that post stress cross-sections, with grain orientation analysis using a technique like electron backscatter diffraction (EBSD), be performed to provide an assessment of failure data as a function of grain orientation.

4.3 Distribution of Current to the Bump(s)

It has been well established that confinement of the current within the bump, or current crowding, plays a significant role in void formation and bump failure during bump electromigration testing [10-14]. Current crowding can lead to damage initiation where the current density is at its peak. Thus, bumps with nominally identical geometry and composition can exhibit different degrees of damage for the same applied current. Bumps with different current distributions can perform differently in an electromigration test even when stressed with the same conditions.

Consequently, different current distributions may yield different values of maximum bump current density. For this reason, it is important that the EM test structures represent as closely as possible the configuration that will be used in the product. The die and package metal current feed lines must be made large enough that the metal lines do not experience electromigration failures due to large amounts of joule heating or affect the resistance measurement of the bump during the test, since much higher currents and temperatures are used in the electromigration test than would be used in a product. Due to these considerations, the metallization geometries and linewidths used in the product cannot effectively be used in the test structure. Nevertheless, the distribution of current to the bump should be arranged so that it matches actual product as closely as possible.

A metric sometimes used to assess current crowding is the ratio of the peak current density to the average current density in the bump (called the current crowding ratio) [4]. Modeling can be performed in order to evaluate the current crowding ratio in the test structure and to assess its relationship to product. It is important when presenting bump electromigration data that the details of the test structure be included in the report so that the reader can determine whether the test structure is representative of the current distribution in the actual product. In fact, a variety of current distribution configurations may need to be tested in order to adequately cover the range of product configurations intended.

4.4 Resistance of the Test Structure

The resistance of an individual solder bump interconnection is very low, typically between 5 m Ω to 20 m Ω . The resistance of external wiring connections to the pads above and below the bump will generally be much larger than the interconnect resistance, on the order of a few tenths of an ohm to over 1 ohm. This external parasitic resistance will depend on temperature and may also degrade during the course of an electromigration stress test. As mentioned previously, Joule heating in the external wiring can introduce additional complications into the test. This external parasitic resistance can be reduced by increasing the wire width and thickness; however, this may result in an EM device structure which is very different from product designs. For single bump test structures, the external wiring resistance may not present a difficulty for current drive. However, for multi-bump chain structures with one or few voltage taps, it is important to reduce the wiring resistance as much as possible, increasing the proportion of bump interconnect resistance to the total resistance. In EM testing one needs to balance the ability to accelerate the test through use of a robust test structure versus testing a structure which is non-representative of product structures and current distributions.

4.5 Types of Test Structures

There are typically two basic types of structures used in EM:

- a) a single bump, and
- b) daisy chain (a chain of multiple bumps).

4.5.1 Single-Bump Structures

This structure measures the resistance of a single bump. The die and substrate bump pads form the bump terminals, which are connected to both a current force connector and a voltage sense connector on each side. The resistance measured is that of the bump plus the series resistance of the connecting wires. Ideally, most of the resistance would be in the bump itself.

As a practical matter, the series connections up to the place where the current force and voltage sense lines diverge can account for a significant fraction of the total resistance of the structure. Due to the 3-dimensional distribution of current in pads and bumps, the exact location of the current and voltage taps can influence the measured resistance. Since bump resistance can be of the same order as wiring resistance, the lines on the EM device or substrate cannot be regarded as having the same voltage potential. Setting the voltage taps slightly away from the bump, along the current feed line, adds some unwanted wiring resistance to the measured value but assures that all parts of the bump and pad structure are included. For feeding the stress current to the tested bump, several bumps should be used to prevent premature failure of the non-tested bumps.

Advantages of the single bump structure:

- Accurate single bump resistance.
- Defined stress current direction.
- Easier failure analysis since there is only one bump to investigate.
- A resistance change, ΔR , of the structure can be used as a measure for bump degradation.

Disadvantages of the single bump structure:

- Low statistical confidence of the lower tail of the failure distribution unless a very large sample size is used.
- Defect-driven early bump failures may be hard to detect due to small test population.

4.5.2 Daisy Chains

Daisy chains consist of multiple bumps in the EM test structure. In daisy chains, alternate bumps are stressed with current flowing in opposite directions. That is, electrons flow out of the die in one bump and out of the substrate in the adjacent bump. For this document, a “simple daisy chain” is defined as a structure in which the same current flows through a single bump in one direction, then through a second bump in the opposite direction, and then continues to alternate, as illustrated in Figure 1. Analyzing daisy chain data is less straight-forward than analyzing data from single bumps. In analyzing EM data for daisy chain bumps, it is sometimes assumed that the majority of the resistance increase of the chain is due to one strongly degraded bump (e.g., weakest link model [15]). If this is assumed, it should be confirmed through failure analysis. Assuming a weakest link model, testing a daisy chain using a small increase in resistance as the failure criterion should yield the time to serious degradation of the fastest degrading bump. Data analysis procedures for daisy chains are discussed in 7.2.

For the purpose of this document, the cathode terminal is the negative terminal. When the die is the cathode, electrons flow from the die to the substrate. The anode terminal is the positive terminal. When the die is the anode, electrons flow from the substrate to the die. It should be noted that some of the literature reverses this definition, and care must be taken to understand the direction of electron flow. A simple daisy chain can possibly have failures of both cathode and anode bumps. If one is interested only in the time to failure of a product (which presumably contains anode and cathode bumps in approximately equal numbers), this mixing of failure modes may be acceptable. However, it may give a bimodal distribution of the failure data or possibly increase the apparent spread (e.g., standard deviation) of failure times. If it is desired to distinguish the degradation from the two current directions, a daisy chain is needed that uses current flow in one direction through multiple bumps and a single bump for current flow in the other direction. Such a structure is described in more detail in 4.7.

Due to their higher total resistance, Joule heating is generally more significant in daisy chains than in single-bump structures. Care must be taken in the structure lay-out so that heating is uniform for the whole chain and that the temperature can be effectively monitored. If the temperature is not uniform for all bumps, erroneous results can occur. If the structure is spread out over a large area, the ratio of metal line resistance to bump resistance can be quite high. Ideally, the total structure resistance would be less than a few tenths of an ohm, which limits the number of bumps that can be effectively used in a chain. A daisy chain can be divided into several sub-chains with a full set of I/Os for every sub-chain. This setup facilitates physical failure analysis by providing the failure site in a specific sub-chain. It also enables for the continuation of the stress test on the other functional sub-chains, thus providing more information about the failure distribution.

4.5.2 Daisy Chains (cont'd)

Advantages of daisy chains:

- Defect-driven early bump failures can be detected more easily.
- Better statistical confidence for the lower tail of the failure distribution.
- With daisy chains, stress tests can be focused on first fail bumps resulting in shorter test times and good coverage of the lower tail of the failure distribution. Continuing a stress test after the first bump failed yields more information about the failure distribution but also results in longer test times.

Disadvantages of daisy chains:

- Difficulty in separating failures from each current direction without detailed failure analysis. This shortcoming can be addressed with a structure which contains multiple bumps in one direction of current flow and one bump in the other direction.
- After the first bump fails, the rest of the chain can no longer be stressed unless taps are added to the test structure to isolate failing bumps that allow for continued stressing of the surviving bumps in the chain.
- In order to focus on one direction of current flow, the total number of bumps in the structure can become quite large
- It can be more difficult to identify the failed bump. Failure analysis is facilitated if all bumps are in a single line. This problem can be mitigated by separating the chain structure into sub-chains with a set of I/Os for every sub-chain.
- Most of the chain's resistance is due to the interconnect rather than the bump. Therefore, small increases in bump resistance in one bump are very difficult to detect, as that value is averaged over all the bumps in the chain.

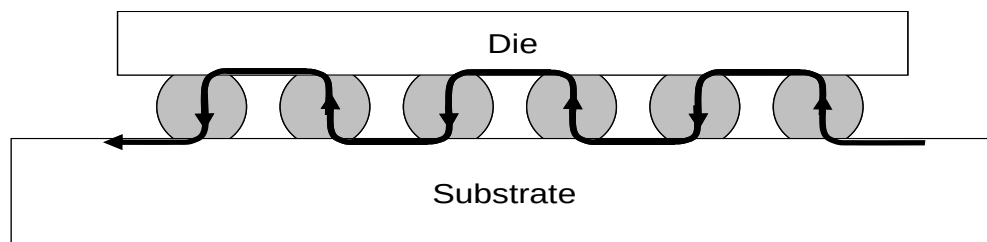


Figure 1 — Diagram of a Simple Daisy Chain EM Structure