

JEDEC PUBLICATION

Recommended ESD Target Level for HBM Qualification

JEP155B

(Revision of JEP155A.01, March 2012)

JULY 2018

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2018
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

sobco

RECOMMENDED ESD TARGET LEVEL FOR HBM QUALIFICATION

Contents

Foreword	ii
Introduction	ii
1 Scope	1
2 References	1
3 Terms, definitions, and letter symbols	4
4 Historical Perspective on HBM/MM ESD Requirements	5
4.1 Motivation for the HBM Target Level	5
4.2 Motivation for Introducing Machine Model (MM)	5
5 Changes and Improvements in ESD and Control Environment	6
5.1 Historic ESD Handling Procedures	6
5.2 Global Implementation of ESD Control	7
5.2.1 Ground and Bond all Conductors:	8
5.2.2 Control Charges on Insulators	8
5.2.3 Use Protective Packaging for Transit and Storage	8
5.2.4 ESD Control Programs and Resulting Data	9
5.2.5 Advantage of Process Analysis	10
5.3 Change of HBM Hazard Scenario by Increasing the Automation Level	12
6 Consolidated Industry Data on HBM Levels vs. Field Returns	13
6.1 Field Return Rates versus HBM Level	13
6.2 Case Studies	16
6.2.1 Devices with Failure Levels below 500 V HBM	16
6.2.2 Devices that Fail between 500-1000 V HBM	16
6.2.3 Devices that Fail between 1000-2000 V HBM	17
6.3 Conclusion	17
7 Impact of ESD Requirements from Customers and Suppliers	18
7.1 ESD Requirements and Specification Failures	18
7.2 Impact of “ESD Failures”	18
7.3 Impact of a Revised ESD Target Level	20
8 IC Technology Scaling Effects on Component Level ESD	21
8.1 Scaling Effects on ESD Robustness	21
8.2 Protection Design Window	24
8.3 ESD Capacitive Loading Requirements	26
8.4 Package Effects	29
8.5 ESD Technology Roadmap	30
8.6 Discussion	31
9 Differences between Component ESD and System Level ESD	32
9.1 The History of System Level ESD	32
9.2 Differences in Component and System Level ESD Stress Models	32
9.3 Case Studies	34
9.4 Conclusion	34
10 Recommendations for a New ESD Target Level	35
10.1 New Realistic Target Level for HBM	35
10.2 Treatment of Special Pins	36
10.3 Timeframe for Applying New Recommendations	36
10.4 Future Cost of ESD Design	36
10.5 Product ESD Evaluation Criteria	37
10.6 Looking Forward	38
Annex A (informative) Frequently Asked Questions	39
Annex B (informative) Machine Model – Correlation between HBM and MM ESD	44
B.1 Correlation: HBM vs. MM	44
B.1.1 Consequence of 1 kV HBM Target	45
B.2 Exceptions to HBM/MM Ratio	47
B.2.1 Bipolar vs. Unipolar Stress	47
B.2.2 Advanced Technologies	48
B.3 Conclusions	49
Annex C (informative) Differences between JEP155B and JEP155A.01	50

RECOMMENDED ESD TARGET LEVEL FOR HBM QUALIFICATION

Foreword

For more than 20 years, IC component level ESD target levels for both HBM (2 kV) and MM (200 V) have essentially stayed constant, with no focus on data to change these levels. Today's enhanced static control methods required by OEMs do not justify these higher HBM/MM levels as data will show in this document. ESD over-design to these levels in today's latest silicon technologies is increasingly constraining silicon area as well as performance, and is leading to more frequent delays in the product innovation cycle. Based on improved static control technology, field failure rate, case study and ESD design data, collected from IC suppliers and contract manufacturers, we propose a more realistic and safe HBM ESD target level which ensures a minimum MM performance level. This new HBM level (1 kV HBM) is easily achievable with static control methods mandated by customers and with today's modern ESD design methods. As discussed in JEP172, MM testing is redundant to HBM and produces the same failure mechanisms. As a result, target level discussions for MM have been removed from this document as they are not applicable in component level testing (see JESD47 [1]). In addition, Clause 6 from the first revision of this document has been moved to Annex B. This is to preserve the data for future reference.

Introduction

This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD level requirements. It will be shown through this document why realistic lowering of the ESD target level for HBM component level ESD is not only essential but is also urgent. The document is organized in different sections to give as many technical details as possible to support the purpose given in the abstract. Additionally, frequently asked questions (FAQ) in the annex are intended to avoid any misconceptions that commonly occur while interpreting the data and the conclusions herein. All component level ESD testing specified within this document adheres to the methods defined in the appropriate JEDEC and ESDA/ANSI specifications.

In June 2009, the formulating committee unanimously approved the addition of the ESDA logo on the covers of this document.

Since the first release of JEP155, additional work has been completed to show that MM qualification testing is not needed. This has been released as a separate JEDEC publication, JEP172 [2]. MM qualification testing is not a required component level qualification test per JEDEC (see JESD47 [1]), EOS/ESD Association, AEC and JEITA. HBM and CDM testing are sufficient component level qualification tests to assess IC ESD robustness. In response to JEP172, this update to JEP155 will remove references to MM qualification testing, with Clause 6 being moved to Annex B. It should be noted that this discussion is only for MM *qualification testing*, this does not imply that there are no risks in an ESD protected area (EPA) due to isolated conductors. The Industry Council recommends an appropriate ESD control program is put in place as per ANSI/ESD S20.20 or IEC 61340-5-1 in order to ensure low risk to isolated conductors. An assessment of MM performance can be determined by the HBM qualification test data as discussed in Annex B.

It should be noted that several figures related to technology nodes are from the initial release of the publication. While the data is older, the trends and conclusions from that data still hold true today.

RECOMMENDED ESD TARGET LEVEL FOR HBM QUALIFICATION

(From JEDEC Board Ballot JCB-18-14, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

The intent of this report is to document and provide critical information to assess and make decisions on safe ESD level requirements. The scope of this document is to provide this information to quality organizations in both semiconductor companies and their IC customers.

1.1 Special Notes on the System Level ESD:

1. This work and the recommendations therein are intended for Component Level safe ESD requirements and will have little or no effect on system level ESD results.
2. Systems and System boards should continue to be designed to meet appropriate ESD threats regardless of the components in the systems that are meeting the new recommendations from this work, and that all proper system reliability must be assessed through the IEC test method.

1.2 Special Notes on the Machine Model:

1. The machine model (MM) method as specified by some customers and suppliers is not a qualification methodology by JEDEC for use in place of or in addition to HBM and CDM test qualification.

2 References

- [1] JEDEC Standard JESD47, "Stress-Test-Driven Qualification of Integrated Circuits", www.jedec.org
- [2] JEDEC Publication JEP172, "Discontinuing Use of the Machine Model for Device ESD Qualification", www.jedec.org
- [3] W.M. King, "Dynamic waveform Characteristics of Personnel Electrostatic Discharge", EOS/ESD Symposium Proceedings, EOS-1, 78 (1979).
- [4] L. Avery, private communication.
- [5] D.L. Lin, M.S. Strauss, and T.L. Welsher, "On the Validity of ESD Threshold Data Obtained Using Commercial Human-Body Model Simulators", Proceedings of the 25th International Reliability Physics Symposium, 77 (1987).
- [6] M.S. Strauss, D.L. Lin, and T.L. Welsher, "Variations in Failure Modes and Cumulative Effects Produced by Commercial Human-Body Model Simulators", EOS/ESD Symposium Proceedings, EOS-9, 59-63 (1987).
- [7] ANSI/ESD S20.20-2014; Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)
- [8] IEC 61340-5-1; Electrostatics – Part 5: Specification for the protection of electronic devices from electrostatic phenomena – Section 1: General requirements; 12.1998

2 References (cont'd)

- [9] R. Gaertner; Do we expect ESD-failures in an EPA designed according to international standards? The need for a process related risk analysis; ESD Symposium 2007; Anaheim, CA, USA
- [10] ANSI/ESD STM5.1-2001 or JESD22-A114C.01
- [11] ANSI/ESD STM5.2-1999 or JESD22-A115-A
- [12] M. Kelly et al., 'A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices', EOS/ESD Symposium, pp. 175-185, 1995
- [13] A. Amerasekera and C. Duvvury, 'ESD in Silicon Integrated Circuits', 2002
- [14] G. Notermans et al., 'Pitfalls When Correlating TLP, HBM and MM Testing', EOS/ESD Symposium, pp. 170-176, 1998
- [15] M.D. Ker et al., 'Electrostatic discharge implantation to improve machine-model ESD robustness of stacked NMOS in mixed I/O interface circuits', ISQED, pp. 363-368, 2003
- [16] D. Pierce, 'ESD Failure Mechanisms', ESD Symposium Tutorial, 1995-2005
- [17] J. Whitfield et al., 'ESD MM Failures resulting from transient reverse currents', 44th IEEE IRPS, pp. 136-139, 2006
- [18] C. Duvvury and G. Boselli, "ESD and latch-up reliability for nanometer CMOS technologies," IEDM, pp. 933-936, 2004.
- [19] S. Voldman, "ESD robustness and scaling implications for Aluminum and Copper interconnects in advanced semiconductor technology," ESD Symposium 1997.
- [20] K.H. Oh, K. Banerjee, C. Duvvury and R. Dutton, "Non-uniform conduction induced reverse channel length dependence of ESD reliability for silicided NMOS transistors," IEDM, pp. 341-344, 2002.
- [21] G. Boselli, J. Rodriguez, C. Duvvury, V. Reddy, P.R. Chidambaram and B. Hornung, "Technology scaling effects on the ESD design parameters in sub-100nm CMOS transistors," IEDM, pp. 507-510, 2003.
- [22] C. Russ, H. Gossner, T. Schultz, N. Chaudhary, K. Schroefer, W. Xiong, A. Marhsall, C. Duvvury and C. Cleavelin, "ESD Evaluation of the emerging MuGFET technology, EOS/ESD Symp. 2005.
- [23] H. Gossner, C. Russ, F. Siegelin, J. Schneider, K. Schroefer, T. Schlutz, C. Duvvury, R. Cleavelin and W. Xiong, "Unique ESD failure mechanisms in a MuGFET technology," IEDM 2006.
- [24] A. Salman, R. Gauthier, E. Wu, P. Riess, C. Putnam, M. Muhammad, J. Woo, D. Ioannou, "Electrostatic Discharge induced oxide breakdown characterization in a 0.1 um CMOS technology," IRPS 2002.
- [25] A. Ille, W. Stadler, A. Kerber, T. Pompei, T. Brodbeck, K. Esmark and A. Bravix, "Ultra-thin gate oxide reliability in the ESD time domain," EOS/ESD Symp. pp. 285-294, 2006.
- [26] G. Boselli, J. Rodriguez, C. Duvvury and J. Smith, "Analysis of ESD protection components in 65nm CMOS technology: scaling perspective and impact on ESD design window," EOS/ESD Symp. 2005.
- [27] A. Jahanzeb, Y. Lin, S. Marum, J. Seichl, and C. Duvvury, "Investigation of device body size on CDM tester peak currents and variability," International ESD Workshop, 2007.
- [28] M. Mergens et al., "Diode- Triggered SCR (DTSCR) for RF-ESD Protection of BiCMOS SiGe and CMOS Ultra-Thin Gate Oxides", IEDM Digest, 2003.

2 References (cont'd)

- [29] ESD Association Road Map: <http://www.esda.org/>
- [30] ESD Association White Paper II: Trends in Silicon Technology and ESD Testing, 2006, <http://www.esda.org>
- [31] IEC standard 61000-4-2 edition 1.2, 2001 “EMC – Part 4.2: Testing and Measurement Techniques – ESD Immunity Test”
- [32] W. Stadler “State-of-the-Art in ESD Standards”, Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 127-147, 2007
- [33] ANSI/ESDA/JEDEC Joint Standard, JS-001, “Human Body Model (HBM) – Component Level”, www.jedec.org
- [34] W. Stadler, S. Bargstaedt-Franke, T. Brodbeck, R. Gärtner, M. Goroll, H. Gossner, N. Jensen and C. Müller “From the ESD Robustness of Products to the System ESD Robustness”, EOS/ESD Symp., 2004, pp. 67, 2004
- [35] S. Marum, R. Watson, and C. Duvvury, “Effects of Low Level IEC 61000-4-2 Stress on Integrated Circuits” Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 262-273, 2007
- [36] W. Stadler, T. Brodbeck, R. Gärtner and H. Gossner “Cable Discharges into Communication Interfaces”, EOS/ESD Symposium, 2006, pp. 144-151, 2006.
- [37] B. Reynolds, M. Muhammad and R. Gauthier, “A Test Method to Determine Cable Discharge Event Sensitivity at the Module Level”, Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 252-261, 2007
- [38] T. Smedes, J. Van Zwol, G. De Raad, T. Brodbeck and H. Wolf, “Relations Between System Level ESD and (vf-) TLP”, EOS/ESD Symposium, 2006, pp. 136-143, 2006
- [39] N. Lacrampe, F. Caignet, M. Bafleur and N. Nolhier, “VF-TLP based methodology for the prediction of ESD immunity of a PCB”, Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 240-251, 2007.
- [40] S. Marum, D. Wang and A. Chadwick “Monitoring Clamp Voltage during IEC 61000-4-2 Stress”, Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 450-457, 2007
- [41] J. Barth, J. Richner and L. G. Henry “System Level ESD Radiation Test Far Exceeds Real Human Metal Discharge”, Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 467-478, 2007
- [42] J_H Ko, S_J Kim, K_S Im, K-K Jeon, S-J Song, C-S Kim, C-H Jeon, K-T Lee, H-G Kim, I-H Son “Abnormal HBM and MM Stress at Mobile LCD Module by Set-ESD gun”, Proc. of 1st International ESD Workshop, Lake Tahoe, 2007, pp. 450-457, 2007

3 Terms, definitions, and letter symbols

BGA	ball grid array
CDE	cable discharge event
CDM	charged-device model
CM	contract manufacturer
DIP	dual-in-line package
DSP	digital signal processor
DTSCR	diode-triggered SCR
EMS	electronic manufacturing supplier
EOS	electrical overstress
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association
FinFET	fin field-effect transistor
FOD	field oxide device
HBM	human body model
HF	high frequency
HSS	high-speed serial link
IEC	International Electrotechnical Commission
LNA	low-noise amplifier
MCM	multichip module
MM	machine model
MugFET	multigate field-effect transistor
PCB	printed circuit board
RF	radio frequency
SCR	silicon controlled rectifier
SERDES	serializer/deserializer transceiver that converts parallel data to serial data
SiP	system-in-package
SoC	system-on-chip
SOI	silicon-on-insulator
TDDb	time-dependent dielectric breakdown
TLU	transient latchup
TVS	transient voltage suppressor
ULSI	ultra-large-scale integration
VDD	positive voltage supply
VSS	negative voltage supply

ESD design window: The ESD protection design space for meeting a specific ESD target level while maintaining the required I/O performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced technology node.

ESD robustness: The capability of a device to withstand the required ESD-specification tests and still be fully functional.

It2: The current point where a transistor enters its second breakdown region under ESD pulse conditions and it is irreversibly damaged.

node: Within a circuit, a point of interconnection between two or more components.

protection impedance: The turn-on impedance of any ESD clamp during the ESD current flow

4 Historical Perspective on HBM/MM ESD Requirements

4.1 Motivation for the HBM Target Level

The early 1970s saw the first systematic measurements of HBM on people (e.g., H-P study) including people in moving chairs. A good summary of some of this early work on the human body model was published at the first EOS/ESD Symposium [3]. Workers in these early HBM studies found that even while wearing wrist straps, one could easily generate 1-2 kV HBM. Later in the 1970s and early 1980s, the automotive industry began instituting ESD pass levels, with Ford adopting the MM and 200 V, GM and Chrysler more focused on the HBM, and Chrysler specifying 2 kV HBM minimum after lengthy consideration of even higher voltages. Meanwhile, RCA TV division settled on 2 kV HBM and a specially devised "Kinescope" test model, but no one accepted the latter [4].

Following these kinds of requirements from customers, by the mid-1980s, semiconductor companies began to set internal HBM standards for components, and the 2 kV HBM specification became most common among them. Even at that time, CDM was recognized as a major cause of device failure, not necessarily predicted with HBM testing, and so to some extent CDM testing was also desired.

Most of this early HBM testing was with various testers that were aligned with HBM as described by Mil Spec 883C, Method 3015.X. Workers who were active in the greatest improvements in that spec in the 1980s will remember 3015.4 through 3015.7 (the last being in 1989) in particular, where major changes in the waveform standard followed studies showing that the testers aligned to the earlier version of 3015 produced widely differing failure voltages in semiconductor devices [5, 6]. Only after a short-circuit current waveform spec was introduced were the internal tester parasitic brought under control to an extent that allowed some consistency among testers aligned to 3015. All the while, 2 kV remained as a convenient target for a "passing" voltage. When the HBM test reached Method 3015.7 (1989), the tester waveforms were much improved, but at that point the US Military stopped revising the spec and further HBM spec development passed on to standards committees at the ESD Association and JEDEC.

4.2 Motivation for Introducing Machine Model (MM)

The reasons were:

- a) MM simulated the failures caused by an ungrounded soldering iron contacting a semiconductor pin lead.
- b) MM simulated field damage failures such as CDM at that time better than HBM did.
- c) The zero-ohm discharging resistance in the machine model results in a higher peak current than HBM test for the thermal damage, a lower voltage MM test can be done.

Reason A does not exist anymore due to the dramatic improvement of ESD controls in the advanced automated manufacturing. Reason B also does not exist anymore because the newer CDM test method reproduces these failures better than MM testing. As for reason C, the HBM test itself is not meaningful now because it does not correlate to overstress failures in the field (see Clause 6).

MM has been used for many years to verify the ESD performance of semiconductor devices in Japan. Historically, the first MM ESD test was reported before 1977. Discharging inductance was not defined as it is now, and no discharging waveform was defined either. It was adopted as the Japanese standard, EIAJ

4.2 Motivation for Introducing Machine Model (MM) (cont'd)

IC-121-1982. Because of no discharging resistance and inductance, it was closer to a real metal to metal contact ESD than the existing HBM standard.

Several years later, a MM standard returned from the US with a discharging inductance and oscillating waveform. Since then the MM standard has not simulated metal to metal contact which is now simulated better by CDM. Because of these reasons JEITA dropped the MM standard and added it in the HBM standard as a reference in 1994 (EIAJ ED4701).

5 Changes and Improvements in ESD and Control Environment

5.1 Historic ESD Handling Procedures

ESD control programs have been in place for many years. One of the earliest programs involved the production of gunpowder. This simple program simply kept the powder wet during manufacturing and handling. This kept the static charge low enough that the gunpowder would not ignite.

In the 1950s and 1960s, electronics were not that sensitive to ESD events. The devices of the time could withstand most events without a problem. Even if they did fail for ESD events, the failures were a very small proportion of the overall failure rates.

In the late 1970s, with the introduction of large scale integration (LSI), ESD was noted as a problem. A group of industry experts realized that this was a problem and organized the first ESD Symposium in 1979 in the US. At the time, technical papers were exchanged and there were workshops on problems and solutions. Companies at this time also started to implement ESD control programs. Each company had their unique program and did not share the information. The need for standardized programs was not recognized at that time.

The US Military was one of the first organizations to recognize the problems with static electricity and ESD. The first standard to address ESD process control was Mil-STD-1686 released in May of 1980. This standard along with its companion handbook Mil-HBK-263 represented the first ESD control standard in the industry. All of the suppliers of electronics to the military were required to comply with this standard. However, most of the private sector still followed company developed procedures.

These early standards were focused on people and packaging. Controls in place for insulators were left mostly to the end user without much consideration except for the removal of non-required insulators. Tools, machines and automated equipment were not addressed or really considered as most of the processes were manual. The basic instructions were to keep everything and everyone at the same potential.

An additional issue with these first ESD control programs was that the materials that were used to control static electricity did not have standards to qualify the materials. This led to many different types of testing, different methods and different instrumentation that caused different results. In some cases, materials measured by these methods did not perform well in controlling static. In the early 1980s, a technical

5.1 Historic ESD Handling Procedures (cont'd)

association, the ESD Association (ESDA) was formed to try to resolve some of the issues surrounding material testing. The first standards from the ESDA were simple material tests for items such as wrist straps, work surfaces and flooring.

The standards did create a way to compare one product with another product. Suppliers of these materials were able to use the standards to improve the products to make them better. For example, the simple wrist strap has gone through many changes in the industry. What started out as a simple metal bead band has evolved into a system that makes better contact with a person and in some cases allows for continuous monitoring. They provide a much more reliable connection than before and last longer. The standards also provide a way to test the wrist straps in a consistent manner so that one that becomes defective can be removed and replaced. Before this, materials were used until they were physically damaged without regard to the electrical properties.

In the 1980s and 1990s the electronics manufacturing industry changed from each company having all the manufacturing reside within the company to a model that included many contract manufactures (CM) or electronic manufacturing suppliers (EMS). The military standard and the European standard, CECC 00 015:1991, became out of date. They were either too restrictive or did not address all aspects of a control program.

The ESDA in 1995 was given the task of replacing Mil-Std-1686 with an industry standard. The standard ANSI/ESD S20.20-1999 [7] was the replacement for ESD process control. Following this standard, a third party certification program was established to demonstrate compliance to the standard. Today, this standard has been updated and replaced by ANSI/ESD S20.20-2014. In parallel, the IEC updated IEC 61340-5-1 [8] to become technically equivalent to ANSI/ESD S20.20-2014. These standards when followed are written to safely handle 100 V human body model devices. All of these standards have improved control materials, understanding and ESD control processes.

5.2 Global Implementation of ESD Control

Manufacturing of ESD sensitive products is currently performed in all parts of the globe. However, since the late 1990s there has been an ever increasing trend to move electronics production from high cost to low cost geographies.

Globally, there is a large difference in the types and levels of ESD programs that are in existence today. ESD control programs range from:

- a) Little or no ESD control
- b) Basic ESD controls
- c) Detailed ESD control programs

The level of ESD controls is not strictly related to geography but in many cases is driven by customer requirement. There are many ways to establish an effective ESD control program. This leads to considerable differences in effective ESD program design and the controls that are ultimately used.

5.2 Global Implementation of ESD Control (cont'd)

However, every well established and maintained ESD control program is based on the following three fundamental principles:

- Ground and bond all conductors
- Control charges on insulators
- Use protective packaging for transit and storage

In the following each of these principles is described in more detail.

5.2.1 Ground and Bond all Conductors:

Maintaining ESD sensitive devices and every item that they come into contact with at the same electrical potential will ensure that ESD related events do not happen. This equi-potential situation can be achieved by attaching all of the conductors in the environment to ground (earth) or by bonding them together to maintain an equal potential. Conductors in this situation refers to people, working surfaces, ESD sensitive devices and any process related conductors and dissipative materials that come into contact with ESD sensitive devices. The grounding and bonding of conductors will minimize the chance of HBM and MM discharges from occurring.

5.2.2 Control Charges on Insulators

Every good ESD control program will do the following:

- 1) Remove **unnecessary** process related insulators from the operations where ESD sensitive devices are handled.
- 2) Determine what constitutes an unacceptable electrostatic field on insulators that are required in the manufacturing / handling process (for details see ANSI/ESD S20.20).

Controlling charges on insulators will help to minimize the chance of CDM related ESD events from occurring.

5.2.3 Use Protective Packaging for Transit and Storage

Finally, in order to ensure that ESD events do not occur between manufacturing process steps or during the shipment of ESD sensitive devices to other locations (customer or next processing facility) the devices should be packaged in ESD protective packaging. The adequate level of protection provided by the packaging can be achieved by different packaging systems and has to be defined by the responsible companies.

5.2.4 ESD Control Programs and Resulting Data

A. Little or no ESD control

For the few companies that have not even implemented a basic ESD control program (this means little or no controls used and not verified on a consistent basis) it is very likely that these companies would not be able to handle ESD sensitive devices that have an ESD sensitivity of even 2 kV Human Body Model. Figure 1 shows the voltage on a person's body as they walk in a manufacturing environment that has no ESD floor or footwear. In this situation, the person could damage a device with an ESD HBM sensitivity of 2 kV.

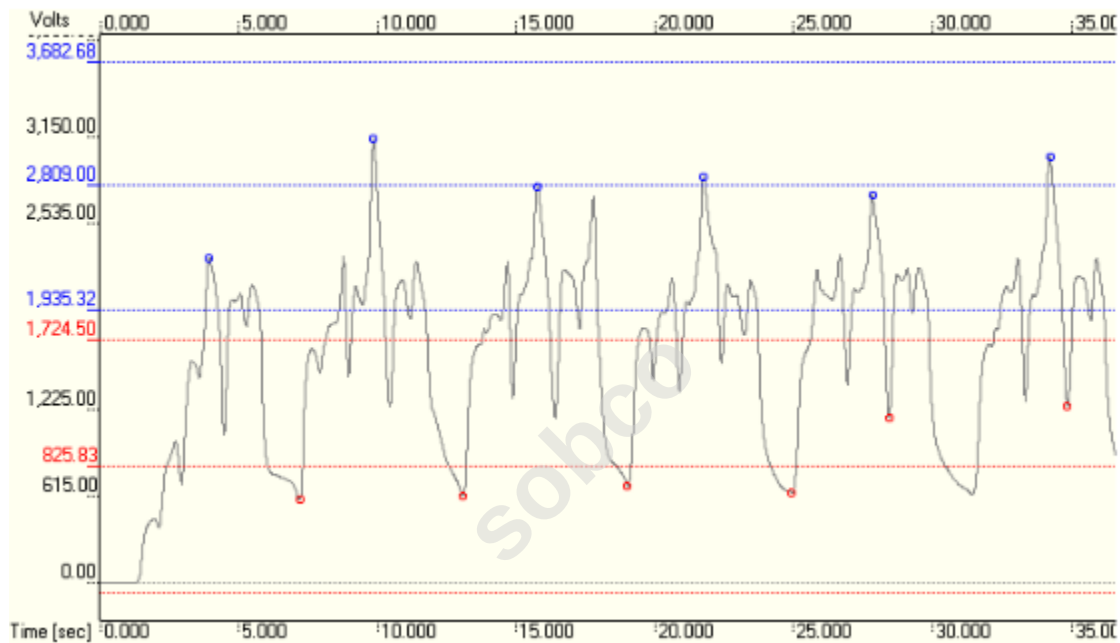


Figure 1 — Voltage on a person's body when walking in a manufacturing environment without ESD floor or footwear

B. Basic ESD Controls

Some companies have implemented a basic ESD control program. A basic ESD control has all the required control elements but no redundancies. The simplest ESD control program consists of personnel grounded with wrist straps, a grounded surface where ESD sensitive devices are handled and all static generating materials are removed and protective packaging for movement of ESD sensitive devices through the process. This type of program is often used by companies where:

- The manufacturing operation is confined to a small area.
- The number of employees handling ESD sensitive devices is small.
- The value of the product is low.
- The reliability of the products being produced is low.

5.2.4 ESD Control Programs and Resulting Data (cont'd)

However, simple does not mean that the program cannot be effective. A well-grounded wrist strap system will keep the voltage on personnel to less than 10 V. As long as the program is audited on a frequent basis this program can be every bit as effective as one where multiple ESD controls are utilized.

C. Detailed ESD Control Program

Finally, many companies utilize detailed ESD control programs to ensure that the devices that they handle will not be damaged. The use of constant monitors, ionization systems and ESD flooring and footwear can add a degree of redundancy and convenience to ESD programs where:

- a) The devices are very ESD sensitive
- b) The value of the finished product is high.
- c) There is a large employee population with a high turnover rate.
- d) The product has high reliability requirements.

All of these factors and more can drive the need for a more complex ESD control program to be implemented.

5.2.5 Advantage of Process Analysis

This example shows the difference between just implementing ESD control measures and doing a deeper ESD control process analysis. Figure 2 shows an example of a manufacturing location that had a conductive ESD flooring system installed. Unfortunately, the company did not make an effort to evaluate the ESD footwear system that was used for its employees. As you can see the voltage on personnel was well above the 100 V HBM threshold that the company had established for itself. The footwear used was chosen based solely on price. However even these shoes would provide adequate protection for a 500 V device.

5.2.5 Advantage of Process Analysis (cont'd)

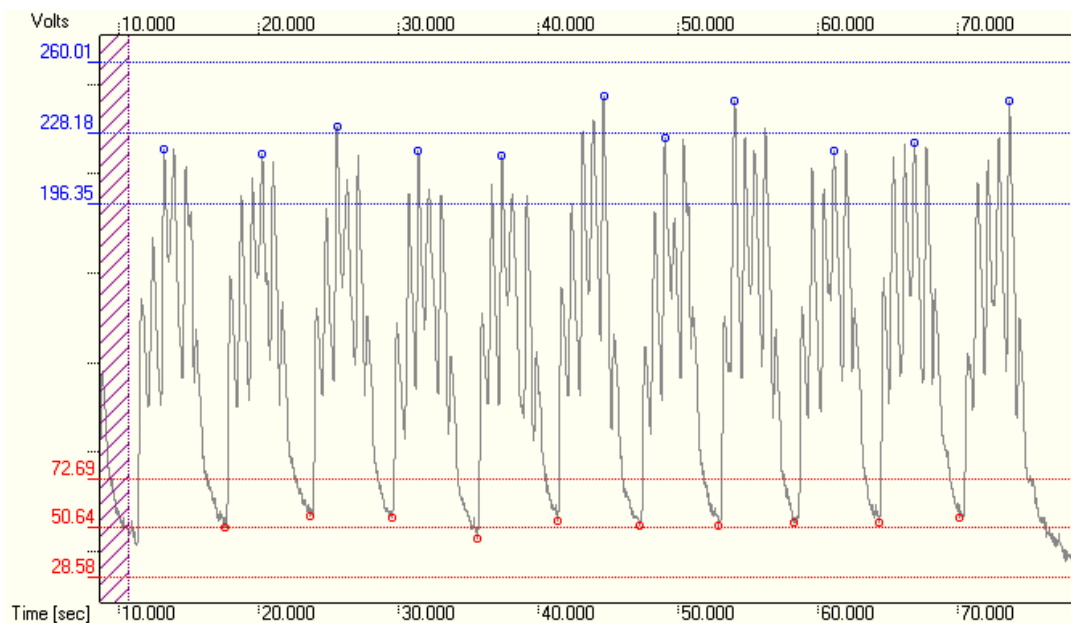


Figure 2 — Voltage of a person in a manufacturing environment when a conductive ESD flooring system was installed (in comparison to Figure 1)

However, once the company understood the implications of their decision, properly selected footwear was implemented and the company was now able to safely meet their goal of handling 100 V HBM sensitive devices as shown in Figure 3.

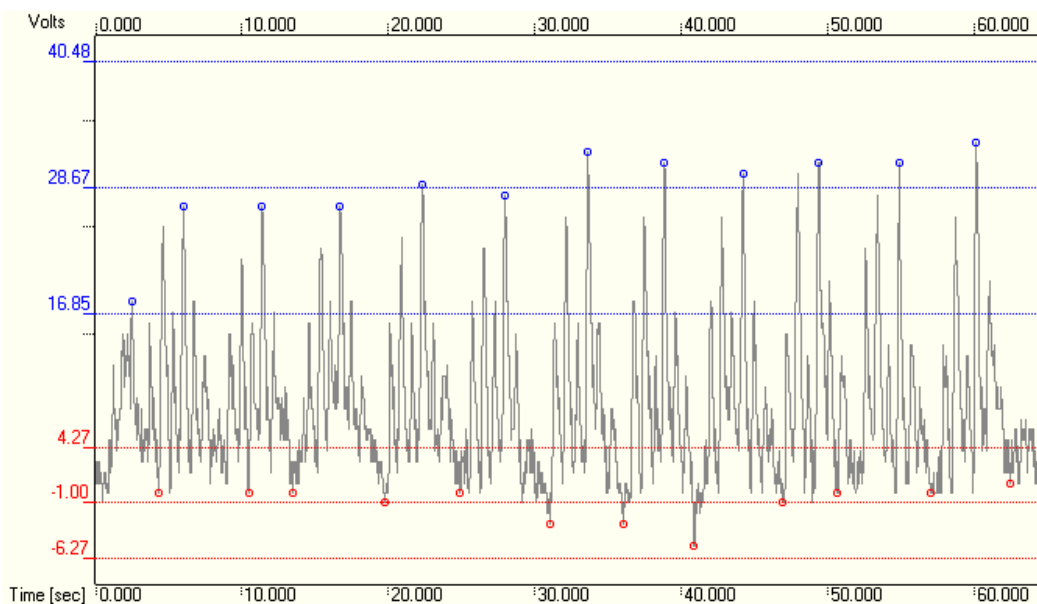


Figure 3 — Voltage of a person in the same manufacturing facility / ESD flooring as Figure 2 but with properly selected ESD control footwear

5.2.5 Advantage of Process Analysis (cont'd)

The other factor that can easily jeopardize an ESD program is infrequent verification that the ESD control elements are working. Most successful companies audit their ESD programs frequently to ensure that all of the control elements are functioning as intended.

Two good resources for establishing an ESD control program are through the implementation of ANSI/ESD S20.20 which is published by the ESD Association or IEC 61340-5-1. Both of these documents will provide the structure and guidance necessary to establish an ESD control program that can safely handle 100 V HBM sensitive devices and higher.

Conclusion:

By establishing an ESD control program and frequently verifying that the ESD controls are working as installed most companies can easily handle ESD sensitive devices with a sensitivity of 500 V HBM or higher. However, with slightly more attention to the selection of ESD control items a 100 V HBM program is easily attainable.

5.3 Change of HBM Hazard Scenario by Increasing the Automation Level

The complexity and automation level of printed circuit board (PCB) manufacturing has increased significantly in recent years. Years ago most devices used packaging with easily contactable pins, with pin counts being lower and pin-to-pin pitch relatively high. These devices were generally assembled manually by operators. In this environment there was the probability of human discharge to a single pin.

Modern packages today can contain up to thousands of I/O, and these I/O can be either pins on the package periphery, balls (as in BGA) or chip-scale packages. The I/O to I/O pitch has decreased dramatically to allow high pin count die to be packaged in a reasonable size. As a result the packaged parts cannot be assembled manually, and the process is automated by non-human handling (grounded machines / tools / pick and place). Modern ESD control programs have evolved to become very effective in control in these types of handling environments, as discussed in 5.2. Therefore for automated assembly lines with modern, frequently audited ESD control programs, the risk of HBM or MM events is very low.

Nevertheless there are still manufacturing areas, such as rework / optical inspection areas, usually smaller areas, where human contact with devices does happen. ESD control programs if effectively implemented and audited minimize the HBM / MM discharge risk in these areas.

It is also confirmed by literature, that most of the ESD related field fails are due to CDM like stress and not due to HBM like stress [9].