

JEDEC PUBLICATION

Recommended ESD-CDM Target Levels

JEP157A

APRIL 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by
©JEDEC Solid State Technology Association 2022
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Suite 240 South
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RECOMMEND ESD-CDM TARGET LEVELS

Foreword

CDM has become the primary real-world ESD event metric describing ESD charging and rapid discharge events in automated handling, manufacturing, and assembly of IC devices. Its importance has dramatically increased over the years as package feature sizes, capacitance, and pin count have scaled upward. In years past, arbitrary CDM protection levels had been specified as IC qualification goals with little background information available on actual/realistic CDM event levels and the protection methods available in manufacturing controls and device design for the safe production of IC components. The rapid advancement of IC technology scaling, coupled with the increased demand for high-speed circuit performance, made it increasingly difficult to guarantee a customer-specified “500 volts” CDM specification and as this update will discuss, even 250 volts can create challenges. At the same time, the required static control methods available for production area CDM protection at each process step have not been fully outlined. Therefore, a realistic CDM specification target must be defined in terms of available and commonly practiced CDM control methods and must reflect current ESD design constraints. Additionally, as technology scaling continues, very high-speed I/Os are being introduced which demand the need for lower CDM target levels in order to achieve the needed I/O performance. This is the scope of this latest update to JEP157.

By balancing improved static ESD controls specific to CDM, and limited ESD design capability in today’s leading technologies, we recommend a CDM specification target level of 250 volts with consideration for lower CDM target levels in unique cases where very high-speed I/O performance is needed. These target levels are a realistic and safe CDM level for manufacturing and handling today’s products using basic CDM control methods or advanced CDM control techniques as needed based on the target level.

At the same time, we show that the current trend of silicon technology scaling will continue to place further restrictions on achievable CDM levels. It is, therefore, necessary that the Industry Council presents a realistic CDM roadmap for consideration by the industry moving forward to 7 nm technologies and beyond, including 2.5D and 3D technologies.

Introduction

It is well understood in the IC industry that the charged device model (CDM) is the ESD model that best describes real-world component-level ESD events during IC manufacturing and handling. [See Clause 4 for details.](#) In contrast to HBM, where basic ESD control measures in manufacturing ensure a safe and realistic specification level (i.e. 1000 volts HBM as reported in JEP155 [1]), CDM protection requires these basic ESD controls as well as additional ESD controls such as managing against the charging of insulators, at specific process steps, to ensure safe and realistic levels for all product designs below 200 volts. Some of these additional process assessment techniques that may need to be involved are detailed out in a recently released standard practice from the ESDA entitled “Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques”, ANSI/ESD SP17.1. As IC applications have moved towards ultra-high-speed I/O interfaces (> 200 Gb/s) over the last decade, this CDM threat has been further exacerbated in terms of qualification levels to achieve design performance. This has driven the need for advanced control methods to be implemented for safe manufacturing in the production area. Combined with these new developments the sensitivity and accuracy for CDM testing have become more

critical than ever. This update to JEP157 addresses the current requirements for CDM presenting a holistic view of the CDM roadmap including both standard and advanced high-speed products.

Some important aspects of the CDM challenge must be understood:

IC Design / Development Constraints: Constraints from silicon technology scaling, IC high-speed circuit design requirements, and larger IC package size trends are impacting ESD protection capability, [see Clause 5 for details](#). These constraints can inhibit the ESD design methodology required to meet the customer-specified 500 or 250 volt CDM levels. This is especially true for very high-speed high-performance pin design types, which have limitations in CDM discharge peak current. As a result, practical designs are restricted to 2-6 amperes of peak CDM current, which translates to a CDM target level of 125-400 volts for many advanced technology products (depending on pin-count). In the same vein, ultra-high-speed designs > 200 Gb/s in the sub-10 nm technologies can be constrained by even tighter CDM peak currents in the range of 2 to 3 amperes for non-RF I/O.

Evolution of Perceived CDM Requirements: 500 volts can no longer be routinely met for the reasons discussed above, often leading to delays in qualification and time-to-market. The more important focus should be that the designs can no longer support these previous levels and that with the available CDM control methods there is no need for higher CDM levels (≥ 500 volts) that make the designs nearly impossible to meet circuit performance. In addition, even if only a small portion of the IC products are designed to be in the market with a high-speed interface, these high-speed interfaces now require consideration for even lower CDM targets compared to most products without these interfaces. Estimates from the ESD Association's Technology Roadmap [2] do show an expected increase in the number of products that are predicted to have CDM levels below 125 volts by 2025 as shown in Figure 1.

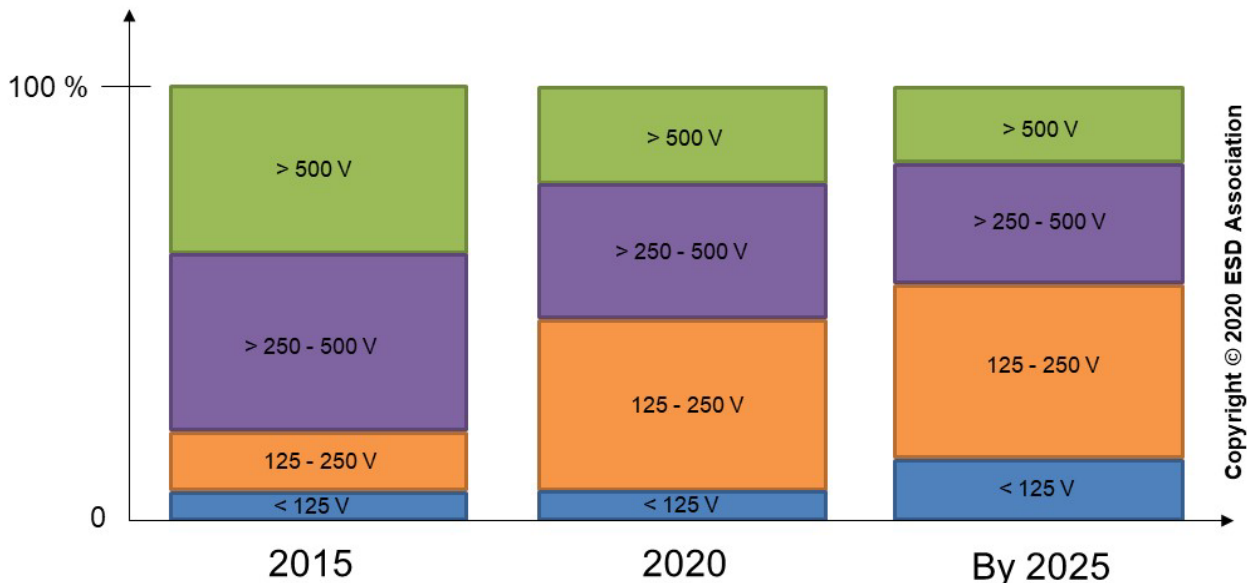


Figure 1 — Forward-Looking Charged Device Model Sensitivity Distribution Groups

Improved state-of-the-art CDM ESD control methods in practice in the industry today. Basic controls allow safe handling for devices with CDM pass voltage levels as low as 200 volts and with process assessment techniques as discussed in [Clause 6](#) and further in ANSI/ESD SP17.1 enabling lower levels. This work has revealed several important findings that need to be considered.

- A. Field return data from 11 billion IC devices show that customer returns can occur for products with CDM pass levels from 200 volts to 2000 volts, meaning control of CDM at production sites is more important than a specific performance target level. [See Clause 7.](#)
- B. Field failures also can occur when proper CDM control is not established during a product ramp-up (pre-qualification), meaning that production failures must be addressed by correcting the CDM control methods at critical process steps rather than requiring the designs to pass at higher voltages than are achievable by design. [See Clause 6.](#)
- C. CDM control measures are available throughout the industry to meet safe manufacturing and handling of products at 200 volts or above, meaning that products designed for CDM levels at 250 volts or 500 volts can be equally safe and reliable. Process assessment techniques as discussed in [Clause 6](#) and further in ANSI/ESD SP17.1 can be used to address even lower CDM target levels.
- D. Thus, any product with a CDM passing level of 250 volts or higher can be handled safely and reliably in a facility with basic CDM control measures. This level of protection should result in minimal impact on design and IC circuit performance requirements and make them compatible with current technology trends. [See Clause 8.](#)
- E. As future IC technologies are enabled, there should be a continuous improvement of CDM control with even more advanced methods coming into practice.
- F. Recently, a standard practice document ANSI/ESD SP17.1 [3] was developed by the ESD Association introducing advanced process assessment techniques valuable for assessing risks below 200V and which can be utilized for dealing with CDM at or below 125 volts. [See Clause 6.](#)

Recommended CDM Levels: Based on this extensive study, a safe and practical CDM passing level of 250 volts is recommended as outlined in Table 1 below. Products with a CDM target level lower than 250 volts should implement additional process-specific measures for CDM control, especially during product ramp-up. For products in this category, process-specific techniques, as described in ANSI/ESD SP17.1, are mandatory.

Table 1 — Recommended CDM Classification Based on Factory CDM Control

CDM classification level (tested acc. to ANSI/ESDA/JEDEC JS-002)	ESD Control Requirements
$V_{\text{CDM}} \geq 200 \text{ V}$	• Basic ESD control methods with the grounding of metallic machine parts and control of insulators according to standards like ANSI/ESD S20.20, IEC 61340-5-1, or JEDEC JESD625
$V_{\text{CDM}} < 200 \text{ V}$	• Basic ESD control methods with the grounding of metallic machine parts and control of insulators + • Process specific measures to reduce the charging of the device OR to avoid a hard discharge (high resistive material in contact with the device leads) + • Charging/discharging measurements at critical process steps following ANSI/ESD SP17.1

Updated Roadmap for continued silicon technology scaling. With more recent developments requiring ultra-high-speed interface designs in technologies of sub-10 nm, the CDM Roadmap has been revised as shown in Figure 2. This was driven by targets for 5 nm SoCs and beyond for operations @ 56 GHz

(Nyquist) or 224 Gb/s PAM4. As designs are now limited to 75 fF of ESD loading capacitance, a target level of 125 volts has become necessary (as indicated by the red bar in the figure) for this ultra-high-speed interface. Package sizes for large ICs, such as microprocessors, at these performance levels, dictate the CDM peak discharge current. To recognize this constraint, the Industry Council is also recommending that the max target peak current of associated 224 Gb/s PAM4 high-speed IP blocks be 2.5 amperes. Advanced process assessment techniques as specified in ANSI/ESD SP17.1 can enable a path to safe manufacturing at these lower target levels. At the same time, lower performance I/Os such as standard GPIO interfaces should still be targeted at 250 volts leveraging basic control methods as described in ANSI/ESD S20.20 [4], IEC 61340-5-1 [5], and JEDEC JESD625 [6] this will help minimize the manufacturing risks on products that may have a high-performance I/O. This is explicitly shown in the figure at the 7 to 5 nm node with the green bar at 250 volts in the figure for standard I/Os, and the red bar at 125 volts for ultra-high-speed 224 Gb/s PAM4 I/O interfaces. The choice of qualification thus depends on the I/O applications.

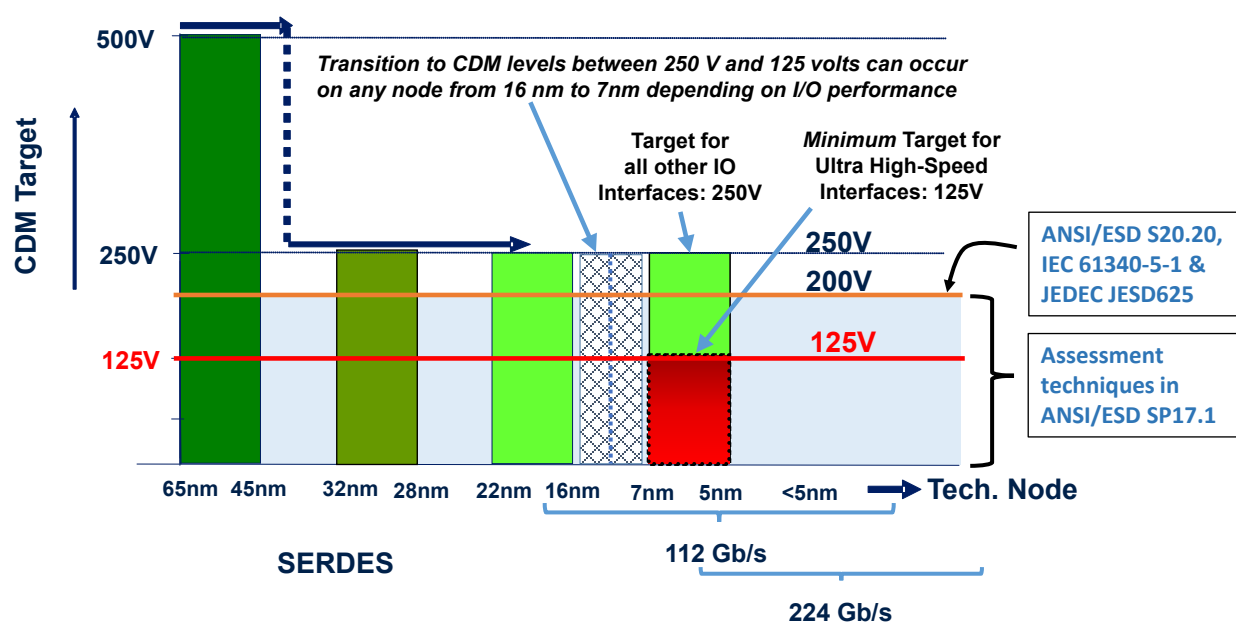


Figure 2 — Technology scaling effects on practical CDM levels and the associated CDM control requirements

As I/O performance levels increase above 56 Gb/s PAM4, a reduction in the maximum peak current design target will be needed for CDM due to reductions in the ESD design window based on technology, package size, and I/O performance. This means that even 250 volts may not be achievable and still meet performance requirements. However, care should be taken on the design side to ensure that if a target level of 250 volts cannot be met as a function of the ESD window, package size, and performance reasons, as discussed in [Clause 5](#), that the achievable target level is *maximized* to reduce manufacturing risks. The designed target level for the product must also be in line with the manufacturing capability. Simply reducing the target level directly to 125 volts may not be prudent for the manufacturing capability. It should be noted that as CDM target levels drop below 200 volts, data, as shown in [Clause 7](#) is limited, and proper manufacturing ESD controls may not have been implemented yet. Care should also be taken to ensure that proper ESD controls are in place and that the proper process assessments have been made in the manufacturing flow as per ANSI/ESD SP17.1 for whatever CDM target level is achievable. This will ensure the manufacturing environment can manage the risks with component target levels moving towards 125 volts.

3D IC CDM Targets: As described in the GSA roadmap [7] for 3D ICs, in 2.5D and 3D packaging processes, with die stacking some micro-bumps are not connected to the external package ball, but can experience ESD exposure during a few process steps of the manufacturing process. In these packaging technologies, the number of micro-bumps can range from hundreds up to tens of thousands, a CDM target I_{PEAK} range from 100 milliamps to 1 ampere is discussed for qualification. Careful consideration of ESD controls in a few critical process steps will guarantee the safe handling of these micro-bumps in manufacturing. The qualification can be done by assessing these internal bumps with very fast TLP (VF-TLP) or wafer-level CC-TLP equipment.

External/Internal High-Speed I/Os: Externally exposed high-speed I/Os require extra ESD control precautions in the handling, manufacturing, assembly, testing, and system installation phases. At the same time, internal I/O are not immune to ESD risks. [Annex A](#) explains how the risk of CDM events is limited with a product's internal I/O but can exist especially during printed circuit board (PCB) and system assembly if ESD control precautions are not fully implemented, while external I/O have extra precautions that may need to be taken to ensure these I/O are safe in real-world environments.

CDM Qualification of Interface IP: Determining whether an IP, when integrated into the product, is expected to pass the product's classification level is uncertain at best for the end-user. This is because the standard CDM qualification of an IP interface to a voltage class is not practical as products are qualified for a given package type or package size. For this purpose, a qualification method for IP based on a CDM peak current as a qualification parameter is suggested as guidance in [Annex B](#).

Test Methods for Sensitive CDM Targets: As the CDM target levels are reduced to below 250 volts, proper test methods and accuracy of the test will become critical. [See Annex C](#). Various techniques are being investigated to improve the present air discharge test method for its fidelity. At the same time, there is a much more serious effort to introduce contact-based testers for better reliability at lower CDM test voltages. It is likely a standard will be developed allowing for both air discharge and contact-based testers to be used alternatively. Currently, a method for contact based CDM testing called low-impedance contact CDM has been released as a standard practice [8]. These critical developments are concurrently taking place as CDM targets below 250 volts and as low as 125 volts are recommended.

Final Words: This revision of JEP157 addresses the critical need for CDM targets for ultra-high-speed I/O interfaces operating at data rates > 200 Gb/s and establishes that a safe level of 125 volts CDM can be recommended. At very high-speed I/O interface data rates > 56 Gb/s, a combination of factors, including the ESD design window for the technology, package size, and I/O performance can drive a reduction in the designed peak current target, meaning 250 volts may not be achievable, but design efforts should focus on maximizing the achievable peak current level to minimize manufacturing risk. Various process assessment techniques (as described in ANSI/ESD SP17.1) are necessary to address the added risks in manufacturing below 200 volts. It is important to emphasize again that all products with standard, lower performance I/Os, should still target 250 volts with manufacturing using known basic control methods such as described in ANSI/ESD S20.20, IEC 61340-5-1, and JEDEC JESD625. Better I_{PEAK} control for accuracy at lower voltages in the CDM standard test methods to validate these CDM target levels is in progress. Although not previously considered for any packaged product, interface IP qualification needs to be addressed and this can be achieved by using a recommended standard for peak current as the target. Finally, it is also recognized that exposed high-speed interface I/Os in a system need special ESD protection requirements, whether they are considered external to the system or not.

RECOMMEND ESD-CDM TARGET LEVELS

Contents

I	Introduction.....	i
1	Scope.....	1
2	References.....	1
3	Terms and Definitions.....	6
3	Terms and Definitions (cont'd).....	7
4	CDM Background and History	8
5	CDM Challenges to IC Component ESD Design	11
5.1	Introduction	11
5.2	The CDM Event from the ESD Designer's Perspective.....	11
5.3	Design Techniques for CDM	13
5.4	Technology Scaling Effects on CDM ESD Robustness.....	15
5.5	Examples of CDM Impact on Integrated Circuit ESD Design.....	17
5.6	Package Effects and Package Trends	22
5.7	ESD Designer's Perspective on Realistic CDM Targets.....	25
5.8	Further Technology Scaling Effects and Additional Impact to Realistic CDM Targets	27
5.9	High Speed/RF Circuits, Scaling Impact on CDM Targets.....	27
6	CDM Related ESD Control in Assembly Lines.....	35
6.1	Motivation.....	35
6.2	Basic Idea of CDM Protection and Process Related Risk Analysis	37
6.3	Process Capability & Transition Analysis.....	44
6.4	Advanced Process Risk Assessment Based on ANSI/ESD SP17.1.....	52
6.5	Conclusions	61
7	Consolidated Industry Data on CDM levels vs. Field Returns.....	62
7.1	Field Return Rates versus CDM Voltage Level	62
7.2	Analysis of Typical Examples.....	64
7.3	Conclusions	65
8	Recommendations for Realistic CDM Target Levels for the Present and an Outlook for the Future	66
8.1	Preface.....	66
8.2	Relevance of Current Level.....	66
8.3	Relevance of Voltage Level	67
8.4	Correlation to Control Measures in Manufacturing Environment.....	67
8.5	Recommended CDM Target Level	68
8.6	Outlook and CDM Roadmap from Silicon Technology Scaling.....	69
8.7	Outlook and CDM Roadmap from Silicon Technology Scaling– Impact of 3D ICs	71
8.8	Challenges and Future Direction of Low Voltage CDM Testing.....	73
8.9	Guidance for Design.....	73
8.10	Summary	74
Annex A	External Versus Internal High-Speed I/Os	75
A.1	Introduction	75
A.2	Exposed High-Speed I/Os	75
A.3	Product Internal High-speed I/Os.....	76
A.4	ESD Risk Classification with High-speed I/Os.....	76
Annex B	CDM Qualification of Interface IP Based on Peak Current	79
B.1	Introduction	79
B.2	Choose Target Peak Current.....	79
B.3	Determine Qualification Voltage Setting from Test Chip CDM Voltage and Peak Current Relationship....	81
B.4	Perform CDM Qualification Testing.....	82
B.5	Summary	83
Annex C	CDM Qualification and Test Methods	84
C.1	CDM Qualification Standards	84
C.2	Comparison of Existing CDM Industry Standards.....	87

C.3	Sources and Impact of Zap to Zap and Tester to Tester Variation	92
C.4	Emerging Test Methods	99
C.5	Conclusions and Outlook: CDM Test Methods	104
Annex D	Some Aspects of CDM Tester Circuit Modelling	106
D.1	Introduction	106
D.2	CDM Tester Model	107
D.3	Waveform Analysis	112
D.4	Conclusions	116
Annex E	CDM Tester Limitations in Representing Real World Events	118
E.1	Physics of Real World CDM	118
E.2	Consideration and Analysis of Real-World CDM	122
E.3	Differences Between Real World CDM and Tester World CDM	125
E.4	CDM Waveform Comparison Between Real World and Tester	126
E.5	Conclusions	129
Annex F	CDM – Does it Correlate to Other ESD Stresses?	130
F.1	Theoretical Analysis	130
F.2	Example and Case Studies	134
F.3	Conclusions	138
Annex G	Charged Board Events and Relationship to CDM	139
G.1	Charged Board Event Problem Statement	139
G.2	Charged Board Event (CBE) Overview	139
G.3	Relation of Charged Board Events to Component Level ESD Test Methods	140
G.4	Charged Board and Related Failure Case Studies	140
G.5	Example Charged Board Event Testing Methods	141
G.6	Charged Board Event Test Results	142
G.7	Identifying and Minimizing Charged Board Event (CBE) Failures	144
G.8	Summary	145
Annex H	Impact of CDM Requirements on Products	146
H.1	CDM ESD Requirements	146
H.2	Impact of Goals on Products	147
H.3	Supplier / Customer Impact of a Revision to the CDM Target Levels	149
Annex I	Frequently Asked Questions	150
Annex J	Revision History	159

RECOMMEND ESD-CDM TARGET LEVELS

(From JEDEC Board Ballot, JCB-22-02, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices reliability Qualification and Monitoring.)

1 Scope

The intent of this report is to document and provide critical information to assess and make decisions on safe CDM ESD level requirements. The scope of this document is to provide this information to quality organizations in both semiconductor companies and their IC customers.

Special Notes on System Level ESD:

1. This work and the recommendations therein are intended for component level safe ESD requirements and will have little or no effect on system level ESD results.
2. Systems and System boards should continue to be designed to meet appropriate ESD threats regardless of the components in the systems that are meeting the new recommendations from this work, and that all proper system reliability must be assessed through the IEC test method.

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3 Terms and Definitions

AEC	Automotive Electronics Council
BGA	ball grid array
CBE	charged board event
CBM	charged board model
CCD	charged coupled device
CC-TLP	capacitively-coupled transmission line pulse
CDM	charged device model
CMOS	complementary metal-oxide semiconductor
CPM	charge plate monitor
DC	direct current
DDR	double data rate
DIP	dual-in-line package
DPM	defects per million
DRAM	dynamic random-access memory
DSP	digital signal processor
DUT	device under test
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EOS	electrical overstress
EPA	ESD protected area
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association; EOS/ESD Association
ESDS	electrostatic discharge sensitive
ESVM	electrostatic voltmeter
FA	failure analysis
FAR	failure analysis report
FAQ	frequently asked question
FCDM (FICDM)	field-induced charged device model
FIM	field-induced model
FinFET	Fin field-effect transistor
FWHM	full width at half maximum
GND	ground, negative voltage supply
GPIO	general purpose I/O
GSA	Global Semiconductor Alliance
HBM	human body model
HDMI	high-definition multimedia interface
HSS (HSSL)	high-speed serial link
IC	integrated circuit
ICT	in-circuit test
IP	intellectual property
I/O	input/output
IEC	International Electrotechnical Commission
JEDEC	JEDEC Solid State Technology Association
JEITA	Japan Electronics and Information Technology Industries Association
LGA	land grid array
LICCDM	low-impedance contact charged device model
LNA	low noise amplifier

3 Terms and Definitions (cont'd)

LV	low voltage
MCM	multichip module
MIPI	mobile industry processor interface
MM	machine model
MV	medium voltage
NFET	N-type field-effect transistor
NMOS	N-channel metal-oxide-semiconductor
NPN	negative-positive-negative (transistor)
PAM	pulse-amplitude modulation
PCB	printed circuit board
PCTA	process capability and transition analysis
PFET	P-type field-effect transistor
PMOS	P-channel metal-oxide-semiconductor
QFP	quad flat pack
RC	resistor-capacitor network
RLC (LRC)	resistor-inductor-capacitor network
RLDRAM	reduced latency DRAM
RF	radio frequency
SATA	serial advanced technology attachment
SBLK	silicide blocked
SCR	silicon-controlled rectifier
SDM	socketed device model
SERDES	serializer/deserializer transceiver that converts parallel data to serial data
SMT	surface mount technology
SoC	system-on-chip
TIVA	thermally induced voltage alteration
TLP	transmission line pulse
TQFP	thin quad flat pack
USB	universal serial bus
ULSI	ultra-large-scale integration
VDD	positive voltage supply
V _{ds}	drain/source voltage
VF-TLP	very fast transmission line pulse
VSS	negative voltage supply
WCDM	wafer-level charged-device model
WSP	wafer-scale package
ZIF	zero insertion force

ESD Design Window: The ESD protection design space for meeting a specific ESD target level while maintaining the required I/O performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent technology node.

ESD robustness: The capability of a device to withstand the required ESD-specification tests and still be fully functional.

I_{t2} : The current point where a transistor enters its second breakdown region under ESD pulse conditions, and it is irreversibly damaged.

Node: Within a circuit, a point of interconnection between two or more components.

4 CDM Background and History

Since the 1970s, the charged device model (CDM) has been associated with the mechanical handling of integrated circuits (ICs) and is cited as a reason for the failure of those ICs. Much of the early work was done at Bell Laboratories [9, 10]. Some of this very useful early work at Bell used a simple vacuum relay to switch stored charge from a component to a nearby ground plane. This was simple but effective and allowed many designers (at many locations, due to Bell's willingness to talk and write about it) to improve their semiconductor components. Bell continued its work on CDM in the late 1980s and early 1990s in their development of a machine [11, 12] that evolved into the commercial testers of today. In the past, these CDM testers were usually built to be in agreement with CDM test standards by the ESD Association and JEDEC [13, 14], first released in the mid-1990s. Today the testers are built to meet the joint JEDEC/ESDA CDM standard, ANSI/ESDA/JEDEC JS-002-2018 [15]. We will call these CDM testers ns-CDM or non-socketed CDM testers.

Components become charged during handling because of triboelectrification or because of being discharged while in the presence of an electric field. Triboelectric charging results from frictional contact by dissimilar materials, while E-field induction takes place near a surface (e.g., nonconductive plastic) that is already charged. CDM ESD stress results when a component under such influence connects to a conductive surface (e.g., a pin touching grounded metal in a socket) at a different potential. For either the triboelectric or the E-field charging, the effective component area figures heavily in the total amount of CDM charge. For triboelectricity, the charge is expected to be proportional to the interfacial contact area with the other surface, while for E-fields, Gauss's Law (normal E-field proportional to surface charge per unit area) indicates that charge goes as component area.

The Bell Labs CDM tester [11, 12] for semiconductor components, a non-socketed CDM tester, was developed in order to duplicate real CDM events as closely as possible. These machines were set up so that the CDM stress depends on the semiconductor package being used, the charge scales with package area, and so on. The standards adopted by ESDA and JEDEC [13, 14, 15] allow a field-induced CDM test system, so called because it uses a field plate to induce a high potential on the component, although charge does not flow onto the component until the discharge event. Figure 3 is a sketch of the ns-CDM tester from several Bell publications that was reproduced in the original JEDEC CDM spec. This method is equivalent to the direct charging CDM method, whereby a single pin (usually a substrate pin) charges the device with respect to a ground plane located under the dielectric, and the CDM discharge is applied with the discharge probe. The ESDA CDM spec [13] allowed for both direct charging and field-induced test methods, with several commercial versions of the tester allowing for both kinds of CDM testing. The joint JEDEC/ESDA standard ANSI/ESDA/JEDEC JS-002 only supports field induction. Figure 4 shows a CDM waveform as sketched in the original CDM standards document, in this case, JEDEC. See Annex C for more details on CDM testing.

4 CDM Background and History (cont'd)

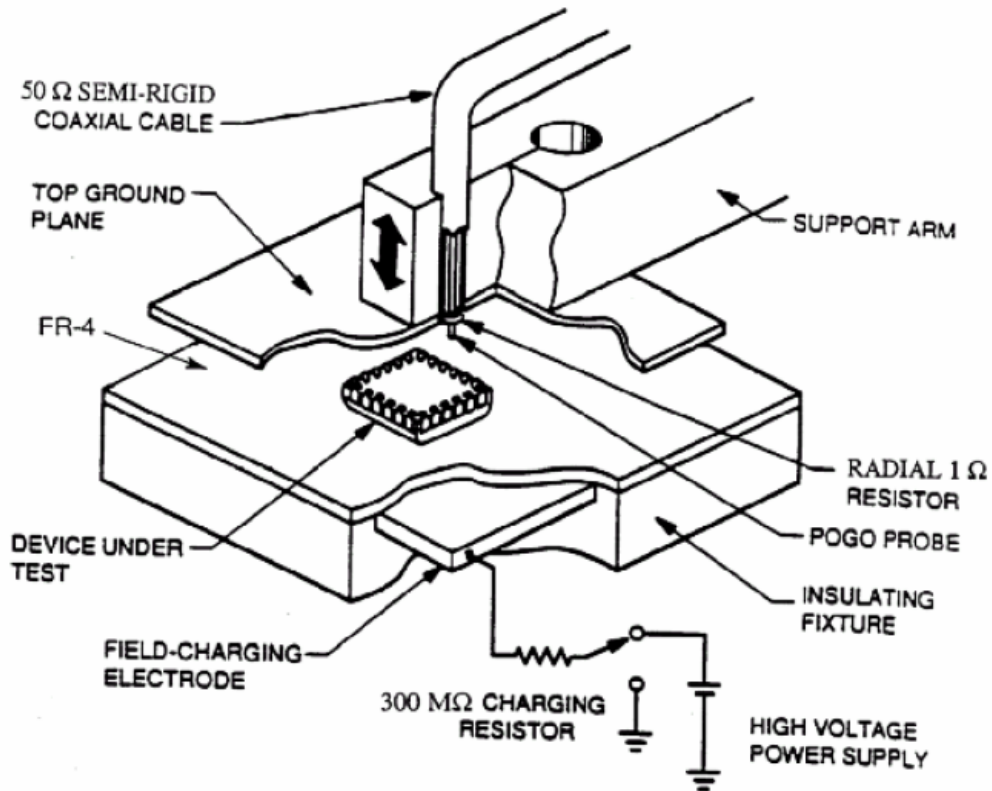


Figure 3 — Sketch of ns-CDM charge device model test system by Bell Labs and incorporated in JEDEC CDM specification.

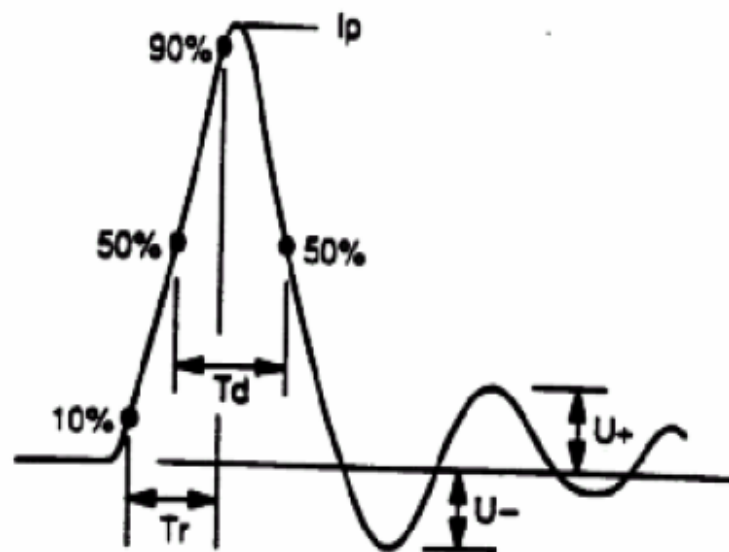


Figure 4 — CDM waveform from ns-CDM standard document. T_d is about 1 nanosecond.

4 CDM Background and History (cont'd)

Since the early 1990s, the socketed device model (SDM) has been a convenient way to exploit automated ESD testing equipment for CDM-like testing of components, using sockets and relays. The history of the first full decade of SDM testing is well-reviewed in a 2001 article [16], which followed shortly after the ESD Association technical report on SDM [17]. Waveforms and parasitics associated with SDM were found to be very different from ns-CDM, although both had the fast-pulse character of CDM and were useful in discerning product weaknesses to CDM. But the advances in process technology of the 1990s, along with much testing of components, made it clear that SDM and ns-CDM could not be unified into one standard. As of August 2017, the ESDA withdrew both the SDM standard practice and technical reports.

A brief history of CDM developments is as follows [18]:

- 1974: Model was first proposed by Speakman —“Human body model is not the only concern to semiconductor users”.
- 1980: Bossard et al — “ESD damage from triboelectrically charged pins”. Details of the potentially damaging model were given in this paper.
- 1985 and 1986: British Telecom workers made experimental investigations of the field-induced ESD model.
- 1985 and 1986: With the rapid introduction of automated handlers, CDM has become a major ESD failure mode.
- 1986: Japanese reported the first automated CDM testing system. (Fukuda et al, OKI Electronics)
- 1987: Siemens Group reported susceptibility of 256K DRAMs to the CDM testing versus real-world situations.
- 1987: Avery (RCA) reported design techniques for CDM protection.
- 1988: Maloney (Intel) reported more extensive design guidelines to avoid CDM failures.
- 1989: AT&T reported a field-induced charged device model simulator.
- 1995-Present: CDM failures became an important issue for IC devices with the shrinking of gate oxide thickness.

Much of this history was discussed in a review article about CDM [19].

In the initial stages of work on CDM and through the 1980s, the most common target voltage for CDM performance was 1500 volts. This was usually achievable with the equipment used and was achievable for the semiconductor devices. For relay-based methods, passing 1500 volts tended to compensate for the slow rise time and reduced peak currents of a relay-based system. However, as the testing hardware advanced, along with advances in semiconductor technology and our knowledge of what the components really experienced, opinions about the voltage target changed and lower voltage targets were accepted. The non-socketed CDM tester became better understood in terms of its actual rise time, peak currents, and waveform shapes. Users built up confidence in its ability to reproduce factory-level events. 500 volts had become acceptable to most of the industry as a non-socketed CDM voltage target for components that could be handled under “reasonable” static control conditions. A study of CDM stress in the factory and how it relates to the non-socketed CDM test voltage scale has revealed that 500-volt non-socketed CDM performance should usually meet those expectations comfortably [19]. As will be discussed later in this publication, advances in integrated circuit technology, the demand for higher performance devices, larger package sizes, and advances in ESD control in factories call for further lowering the required level of CDM robustness.

5 CDM Challenges to IC Component ESD Design

5.1 Introduction

Over the past two decades, charged device model ESD testing has increasingly become an industry requirement for the qualification of IC components. Unfortunately, over this same time interval, three trends have combined to greatly complicate the task of designing effective on-chip CDM ESD protection circuits.

1. The pin count and size range of IC components has grown significantly. This is a serious issue because the peak current produced during CDM testing at a given pre-charge voltage is a sensitive function of the die and especially package size. The net result is that the upper range of CDM currents seen on products is increasing rapidly. Large increases in ESD layout area on the die are required to protect fragile circuits at these higher currents. In some cases, the required ESD layout area becomes prohibitively large.
2. Advancements in IC process technologies with smaller and more fragile active devices as well as thinner and more resistive interconnects have degraded the ESD robustness of circuitry to be protected. This makes it more difficult to protect the component at a given CDM current level.
3. Mixed-signal ICs with high-speed digital, RF analog, and other performance-sensitive pins are becoming much more prevalent. Strict electrical performance limitations on these pins limit options for ESD protection. This often makes it impossible to meet typical CDM ESD qualification criteria.

Taken together, these trends have led to greatly increased challenges for the design of on-chip ESD protection. As a result, many products fail or are marginal to CDM qualification targets of 250 volts or 500 volts. This is a fundamental problem that will only get worse as these trends continue. This clause is an attempt to summarize the CDM challenges to IC component ESD design presented by these continuing trends. It also reflects the two stages this document has gone through. In the first release in 2010, the challenges of designing to a CDM target of 500 volts were discussed, and a new target level for all pins of 250 volts was proposed while demonstrating that 250 volts complies with ESD control methods already in place in 2010. This paved the way for the high performance and low power designs which have been created in advanced CMOS FinFET technologies since then. The proposed target of 250 volts CDM has been adopted by an overwhelming majority of the industry today. The current release of this document in 2021, presented here, includes the novel challenge of very high-speed interfaces which are currently in development, and due to performance reasons, cannot comply with the requirements of a CDM target level of 250 volts.

5.2 The CDM Event from the ESD Designer's Perspective

As described in Annex C, the CDM ESD test differs considerably from the HBM test, both in terms of the tester configuration and the current waveforms produced. These waveforms are compared in Figure 5 [20]. HBM is performed as a socketed device under test (DUT), with the stress pulse delivered between one or more stressed and grounded pins via an external pulse source. The resistor-capacitor (RC) network used in this source produces a relatively long pulse width of ~150 ns for HBM. For HBM, the peak ESD current at a given pre-charge voltage is more or less fixed, independent of the DUT. In contrast, during the non-socketed CDM test, the charge is distributed over the entire DUT and flows through multiple paths to a single grounded pin. Important consequences of this configuration are that the resulting pulse width is very short (~1 ns) and that the peak current produced can vary widely from DUT to DUT, depending on the die and package size.

5.2 The CDM Event from the ESD Designer's Perspective (cont'd)

As can be seen in Figure 5, CDM current amplitudes typically vary in a large range from 1-6 amperes. Note that, at the 6 amperes upper limit, the 250 volt CDM peak current exceeds that of a 1000 volt HBM event by approximately 9X.

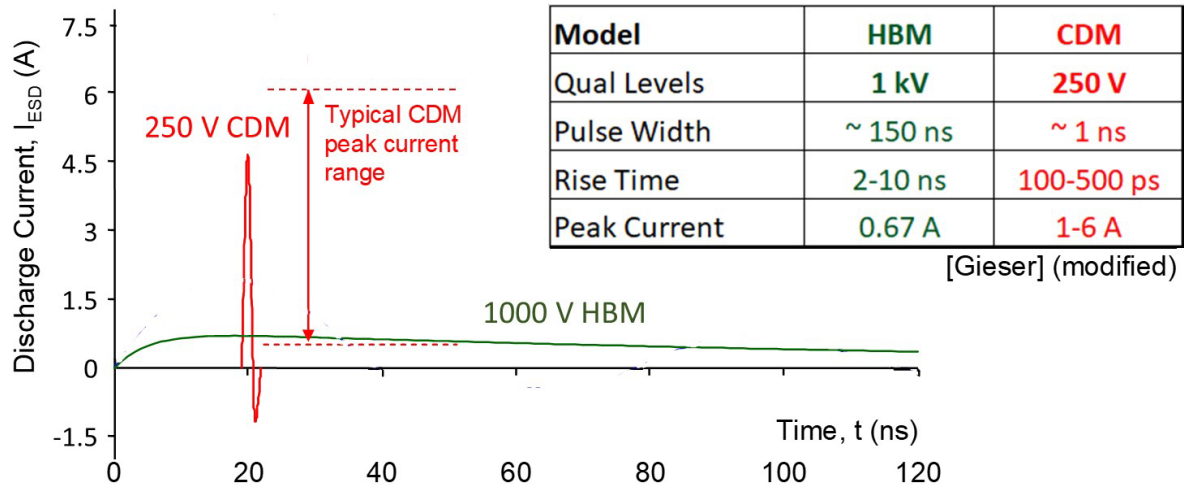


Figure 5 — Comparison of current waveforms for CDM and HBM ESD events.

While component ESD stress levels are typically defined in terms of a stress voltage (i.e. 1000 volts HBM or 250 volts CDM), these voltage values are largely meaningless to the ESD designer. Designers consider the ESD event in terms of the resulting current waveform. Elements in ESD protection circuits and ESD conduction paths are sized based on a target peak stress current and duration. In general, if the target peak current increases, the ESD elements, and conduction paths must be increased in size accordingly. As will be shown below, the ESD layout area on the IC increases not linearly, but exponentially with increasing CDM peak current targets.

Another challenge that is unique to CDM is the fact that the true peak current is not known until each new packaged component is tested. When designing, for example, ESD protection for an I/O cell library which may be used in a wide range of products, the designer is forced to estimate peak CDM currents based on the estimated capacitance of the largest expected die and package. Accurate capacitance information is often not available, forcing the ESD designer to more or less guess a CDM peak current target for the I/O cell library. Marginal component CDM ESD performance is often a result of inaccurate capacitance estimates in the ESD design phase of I/O cell library design. Furthermore, if a given product design changes to a larger IC package, it is expected that lower CDM performance could result. Further discussion on this and some proposals are discussed in Annex B.

5.3 Design Techniques for CDM

In advanced complementary metal-oxide-semiconductor (CMOS) technologies, circuitry which connects directly to input/output (I/O) pads are often most at risk of damage during a CDM ESD event.

In this section, two very common approaches to protecting I/O circuitry are briefly described. This will provide a framework for describing CDM ESD protection challenges in the following sections.

5.3.1 Dual Diode ESD Protection

A schematic of a dual diode I/O ESD protection strategy is shown in Figure 6 [21-25]. The I/O pad connects to receiver and driver circuitry which are powered by the Vddx and GND supply buses. Both primary and secondary ESD protection elements are placed to protect receiver transistors M1-M2 and driver transistors M3-M4, which are typically the I/O devices at greatest risk during ESD. Consider the case where the I/O pad is grounded during a negative CDM event. Most of the positive current will follow a primary path from the grounded I/O pad through the forward-biased D1 diode to the Vddx bus, then down the ESD power clamp to the GND bus, and then from the GND bus metal grid throughout the rest of the IC and package. Note that it is important to minimize the total voltage drop between the I/O pad and GND bus local to the stressed I/O pad during this ESD event. Diode D1 and associated interconnects must be adequately sized. It is also important to minimize parasitic Rvddx and Rgnd bus resistances since they add to the total voltage drop along this primary ESD current path. To better protect large banks of I/O cells in an IC, it is common for multiple power clamps to be distributed in parallel along the power buses.

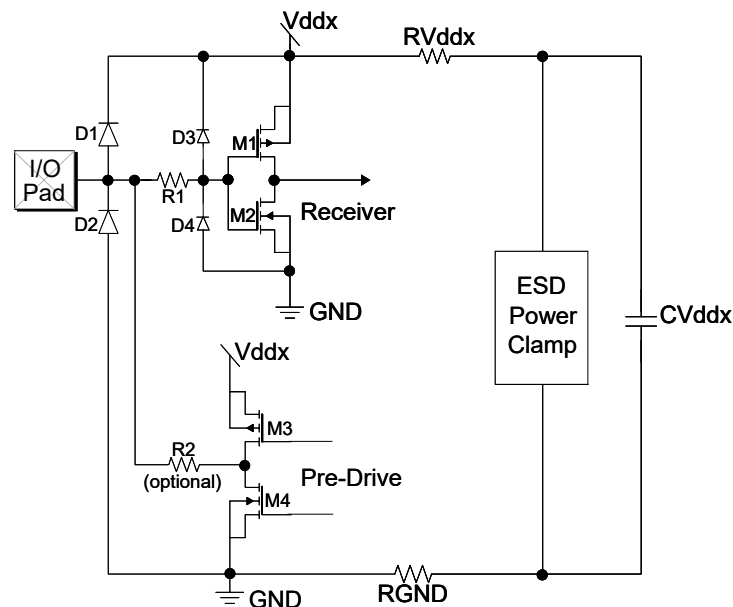


Figure 6 — Dual diode I/O ESD protection strategy

In the ESD strategy of Figure 6, separate secondary ESD protection elements are utilized for the receiver and driver circuitry. During the ESD event described above, a small fraction of the ESD current will flow to Vddx via a secondary path through resistor R1 and diode D3. The benefit of this secondary protection is that any IR drop across R1 will reduce the voltage stress seen across the fragile gates of receiver transistors M1-M2, as compared to the case where R1 is not present. R1 values from 100-5000 Ω are common for protecting receiver circuits.

5.3.1 Dual Diode ESD Protection (cont'd)

To better protect driver transistors M3-M4, there is another secondary path to Vddx via resistor R2 and the drain to N-well parasitic diode of PMOS transistor M3. Note that the use of R2 is shown as an option in Figure 6.

This is because many applications such as high-speed serial (HSS) links or low noise amplifiers (LNA) do not typically permit the use of any series resistance between the driver and pad due to performance constraints. Typical R2 values for digital applications can range from 5-100 Ω . This resistance can have a significant impact on the effective CDM robustness of driver transistors M3-M4.

5.3.2 SCR-Based ESD Protection

A schematic of an SCR-based ESD protection strategy is shown in Figure 7 [26-30]. Here the primary ESD protection comprises a diode string triggered SCR clamp from the I/O pad to the GND bus. Therefore, when the I/O pad is grounded during a negative CDM event, most of the positive current will flow from the pad directly to the GND rail via the SCR clamp and then from the GND bus metal grid throughout the IC and package. This direct clamp to GND is an advantage of the SCR-based protection scheme over the prior diode-based approach, especially in cases where the GND bus resistance is significantly lower than Vddx bus resistance. In addition, SCRs often have reduced capacitive loading for the same ESD protection level. On the other hand, diode string triggered SCRs can have the disadvantage of higher leakage during normal operation depending upon the maximum operating voltage required.

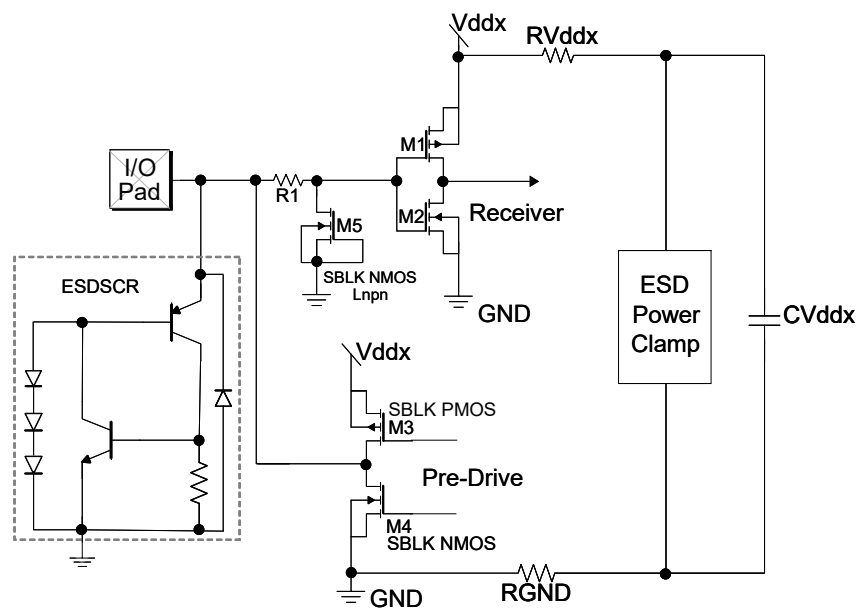


Figure 7 — Diode-string-triggered SCR based I/O ESD protection strategy.

Note that, in the ESD strategy of Figure 7, a different type of secondary protection is utilized to protect the receiver transistors M1-M2, as compared to that shown in Figure 6. Here a fraction of the ESD current will flow to GND via a secondary path through resistor R1 and clamp device M5. This clamp is a silicide blocked (SBLK) NMOS transistor which is intended to trigger and conduct as a lateral NPN bipolar during the ESD event.

5.3.2 SCR-Based ESD Protection (cont'd)

Blocking the silicide in the drain region adds local ballast resistance to the NPN, helping ensure uniform current flow across the device width during bipolar conduction, thereby increasing the failure current (I_{f2}). As before, any IR drop across R1 during ESD will reduce the voltage stress seen across the gates of receiver transistors M1-M2. Note, the secondary ESD NFET is shown for reference only, in this example, the secondary device could be replaced by dual diodes, forward-biased diode strings or another diode string triggered SCR.

The output drivers M3-M4 in Figures 6 and 7 can also be configured with silicide blocking in the transistor drain regions. Added ballast resistance increases the failure current (I_{f2}) of the drivers in the event they trigger and conduct as lateral bipolar transistors during ESD. Also, the added IR drop across this silicide block resistance increases the effective drain to source breakdown voltage the transistors can tolerate before suffering permanent physical damage. This provides more voltage margin to driver breakdown for the intended primary ESD path through the SCR clamp. Silicide block ballast resistance is commonly used to harden output driver transistors against ESD, typically increasing Vds breakdown voltages 1-3 volts, but at a cost in layout area and transistor performance, and process cost. Other design options, in place of these that have been discussed here, will also eventually lead to the same limitations.

5.4 Technology Scaling Effects on CDM ESD Robustness

Advancements in process technologies over the past 30 years have brought about impressive reductions in IC cost and gains in performance. Unfortunately, these advancements have come at a cost in terms of degraded ESD robustness. Technology scaling has produced smaller and more fragile active devices as well as thinner and more resistive interconnects. For these reasons, the ESD protection design becomes more challenging with each new technology node [1, 31].

5.4.1 Trends in ESD Robustness for NMOS Transistors

In Figure 8 the robustness of NMOS transistors across multiple advanced CMOS technology nodes is compared. The maximum core Vdd supply voltage is shown as a function of the technology node scaling for both feature size transistor length and gate oxide thickness. Also shown is the simultaneous reduction of the gate oxide breakdown voltage (V_{gs}) and drain to source breakdown voltage (V_{ds}) under 1.2 ns pulse stress conditions. This data was gathered with a very fast transmission line pulse (VF-TLP) characterization tool which best mimics the true CDM pulse event. All data was gathered on a baseline, minimum design rule, fully silicided NMOS transistors. The Vds breakdown data represents the minimum or worst-case value measured with varying DC Vgs bias applied during stress.

The data in Figure 8 clearly illustrates the reduction in NMOS transistor CDM robustness with each new technology node. While both the Vgs and Vds breakdown data trend downward with each new technology node, these NMOS devices are clearly more fragile under the drain to source stress. It turns out that PMOS transistors (not shown) exhibit similar trends but are slightly more robust than their NMOS counterparts. Compare, for example, the robustness of NMOS transistors at the 250 nm and 45 nm technology nodes. A 250 nm NMOS receiver device, such as transistor M2 in Figure 6, could survive 14 volts Vgs stress during CDM ESD, while the 45 nm device would fail at only 5.2 volts. Similarly, a 250 nm NMOS driver device, such as transistor M4 in Figure 6, could survive up to 6.2 volts Vds stress during CDM ESD, while the 45 nm device would fail at only 3.2 volts. It is clear that transistors become more fragile with each new technology node. This Vds breakdown trend has continued as the channel lengths continue to scale.

5.4.1 Trends in ESD Robustness for NMOS Transistors (cont'd)

It turns out that protecting output drivers with Vds breakdown values of less than 4 volts is a serious challenge for the CDM ESD designer. This is particularly true in applications that do not permit the use of secondary protection or silicide block ballast resistance. Consider, for example, an I/O circuit in a 90 nm technology, with ESD protection as described in Figure 6.

During a negative CDM stress event the NMOS driver M4 will fail if the local Vds voltage across this device exceeds 3.8 volts (see Figure 8). Assuming that the peak current produced by the CDM event equals 7.6 amperes, then the ESD elements and interconnect resistances in the primary ESD path must dissipate this current while limiting the total voltage drop seen across the NMOS driver M4 to less than 3.8 volts. Sizing the ESD elements and interconnects to achieve this 0.5 Ω effective impedance is extremely difficult.

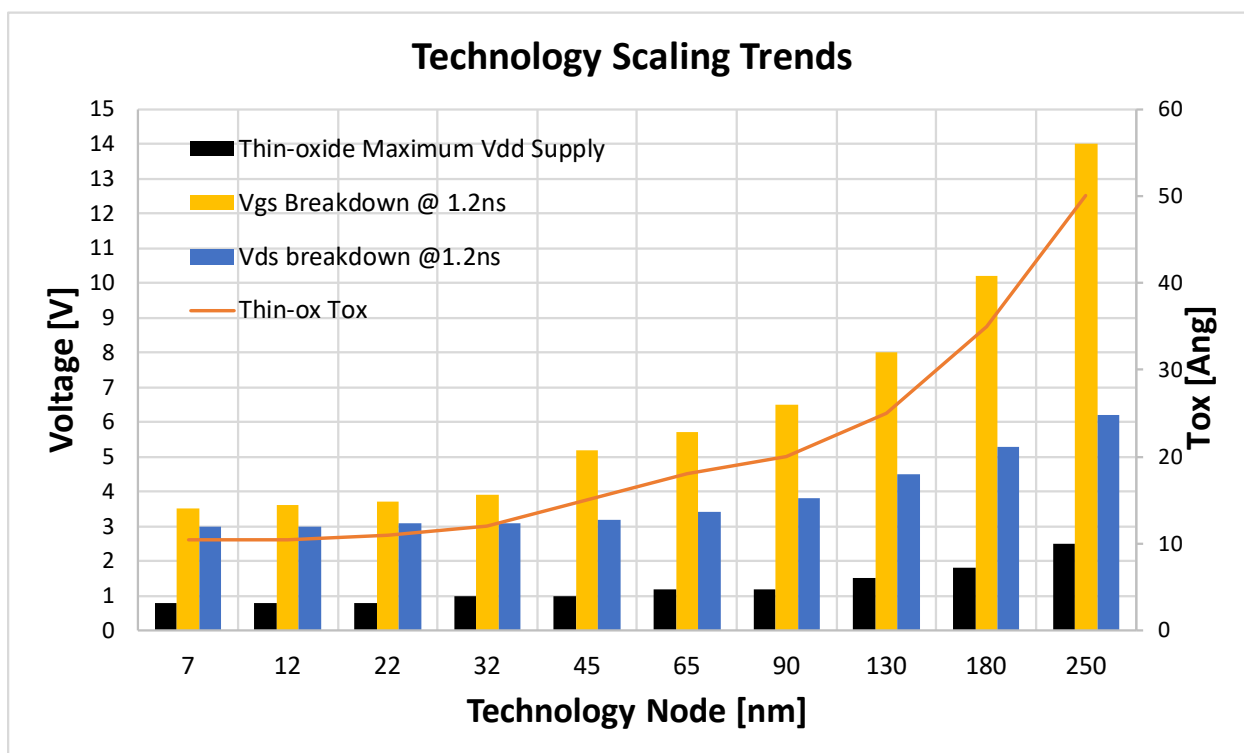


Figure 8 — Trends of NMOS transistor breakdown voltages with technology scaling.

5.4.2 Trends in Interconnect ESD Robustness

Another critical technology parameter for CDM design is the maximum allowed current density in the interconnect layers. This trend is shown in Figure 9 typically for a copper metal interconnect. Note that the actual failure current density is dependent on the particular metal thickness, but this trend is more of an illustration of the constraint. In the CDM domain, the current failure density is actually 3-5 times higher than in the HBM domain. However, if the CDM discharge current level requirements become relatively larger (for example, from large high pin count packaged devices meeting a target level of 500 volts) this could turn into the limiting factor for design. For example, at the 65 nm node, the current density limit of 0.5 A/ μ m requires a 20 μ m wide bus to carry 10 amperes of CDM current. In addition to the layout area, wider metal interconnects to the ESD diodes increase the pad capacitance. This in turn may have a negative impact on the circuit speed as will be discussed in 5.5.3.

5.4.2 Trends in Interconnect ESD Robustness (cont'd)

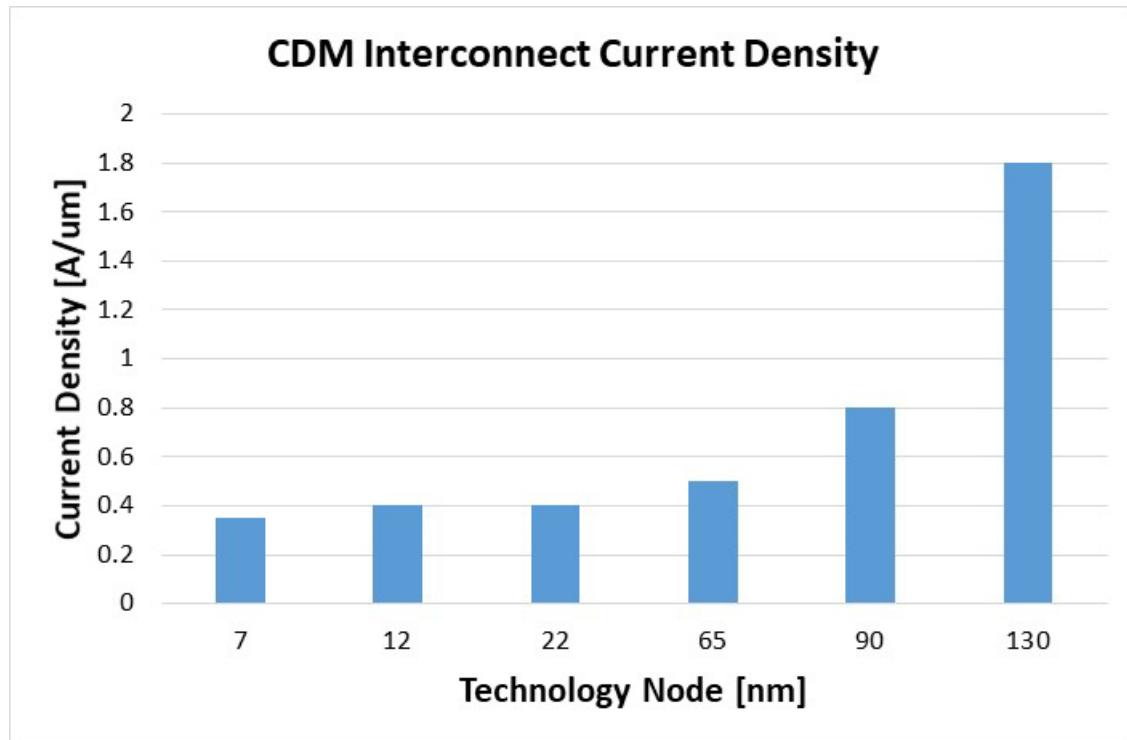


Figure 9 — Typical trends for copper interconnect ESD robustness with technology scaling.

5.5 Examples of CDM Impact on Integrated Circuit ESD Design

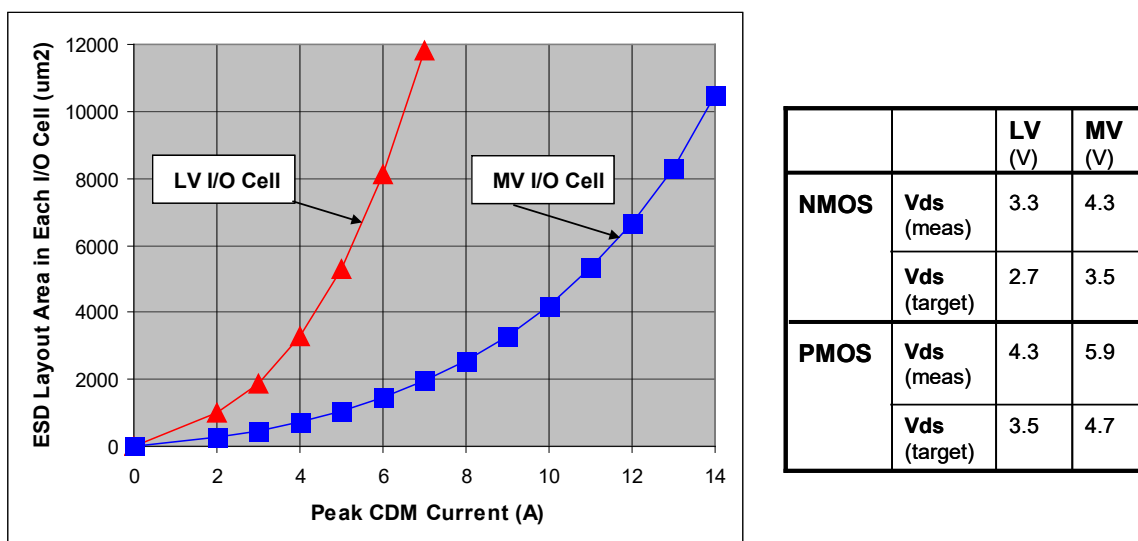
5.5.1 Impact on ESD Layout Area

The ESD layout area on the die required to protect an IC component from a 500-volt CDM event varies widely with product application and process technology. The target peak CDM current the ESD network must safely dissipate is a primary factor affecting layout area. As illustrated in Figure 5, peak CDM currents at 500 volts typically range from about 1 ampere, for the smallest die and package sizes, to 16 amperes or greater, for the largest. The process technology, which defines the efficiency of the ESD devices and interconnects along with the fragility of the circuitry to be protected, strongly influences the layout area. Finally, applications that do not permit the use of added secondary protection or silicide blocking to harden fragile input/output circuits will see significant increases in the layout area. In general terms, a very large IC component in the most advanced available process technology with driver/receiver circuits configured in the most fragile manner requires the greatest ESD layout area on the die.

The ESD layout area as a function of target peak CDM current is shown for two example 45 nm technology I/O library applications in Figure 10. The two I/O libraries differ in the type of transistor used in the driver and receiver circuitry. The low voltage (LV) I/O library, for use in V_{dd}=1.1V supply domains, utilizes the core (18 Angstrom Tox) transistors available in the technology. The medium voltage (MV) I/O library, for use in V_{dd}=1.8 volts supply domains, utilizes the I/O (28 Angstrom Tox) transistors.

5.5.1 Impact on ESD Layout Area (cont'd)

The dual-diode and rail clamp ESD protection approach described in Figure 6 was used in both the LV and MV I/O libraries. Small ESD power clamps were distributed in parallel in each I/O cell of an I/O bank within a supply domain. The ESD power clamps in both I/O libraries were built with the more robust I/O transistors. While secondary protection was utilized to harden the receiver circuitry in both I/O libraries, the application would not allow the option of placing either secondary protection or silicide blocking to harden the output driver devices. Therefore, the weak link for ESD in both the LV and MV I/O cells was assumed to be the NMOS output driver M4 in negative mode CDM events, and the PMOS output driver M3 in positive mode events. The measured V_{ds} breakdown values for the NMOS and PMOS driver devices in both the LV and MV I/O libraries are shown in the table in Figure 10. In order to provide a comfortable margin, the ESD networks in both I/O libraries were sized to protect both driver devices to targets 20 % lower than their measured breakdown voltages. Therefore, as shown in the table, the target stress limits were set to 2.65 volts/3.60 volts for the NMOS/PMOS drivers in the LV I/O library and 3.50 volts/5.20 volts for the NMOS/PMOS drivers in the MV I/O library.



NOTE: ESD layout area is plotted versus peak CDM current. The layout area is calculated for two different NMOS and PMOS output driver protection targets.

Figure 10 — Example estimate of the ESD layout area for I/O cell in two different I/O applications.

As shown in Figure 10, the size of the ESD elements in both the LV and MV I/O cells is a sensitive function of the target peak CDM ESD current the ESD network must safely dissipate. The area value includes the area for the ESD diodes and power clamp in each I/O cell. Note that, for both curves, the ESD layout area increases exponentially with peak CDM current. In fact, for the LV I/O cell, the increasing slope of the curve suggests that CDM current targets above about 7 amperes are not realistic since, beyond this ESD current ceiling, huge increases in layout area are required to achieve a small incremental increase in CDM current. It is important to note that the exponential nature of the ESD layout area vs. CDM current target curve is common to all process technologies and all ESD protection schemes. However, the actual ESD current ceiling will vary considerably from product to product, depending on process technology, circuit application, and ESD protection scheme.

5.5.1 Impact on ESD Layout Area (cont'd)

It is obvious from the drastic differences between the two curves in Figure 10 that the V_{ds} protection target for the output drivers M3-M4 has a major impact on the ESD layout area required at a given CDM current. While 7 amperes CDM protection can be achieved for the MV I/O cell with about 2000 um^2 of ESD layout area, the LV I/O cell requires almost $12,000 \text{ um}^2$ to meet the same protection level. This is a 6X increase. It should be pointed out that the layout area for full I/O cells (excluding ESD) in advanced CMOS technology products typically ranges from 2000 um^2 to 8000 um^2 . Therefore, depending on the CDM current target and the I/O application, the ESD layout area may grow to dominate the overall I/O cell layout area. This is an issue of particular concern for IC components in large packages.

5.5.2 Impact of the ESD Design Window on CDM

It has been well established through various studies that the “ESD Design Window” is rapidly shrinking with the advancement of silicon scaling technologies [29]. As shown in Figure 11, the window is essentially defined as the space between the IC operating voltage (V_{op}) and the IC breakdown voltage (V_{bd}). Although the operating voltages have been slowly reducing (flattened out in the 0.9-1.2 volts range), the breakdown voltages have been degrading at a much faster rate giving rise to the reduction in the window. The limitation of the breakdown voltage could come from either oxide breakdown voltage under ESD conditions (for input buffers) and/or from the avalanche junction breakdown voltage (for output buffers). This is indicated as the “IC Reliability Constraints” in Figure 11. On the other hand, for scaled technologies the metal interconnects are getting thinner, leading to more resistive busses for ESD design applications. Thus, designing to a given ESD current level the voltages at the I/O pads build up to the critical breakdown values at even lower current levels. This metal restriction is shown as “Thermal Failure” in Figure 11. This design window reduction applies to any type of I/O protection strategy even though some advanced designs might give a slight advantage. Nevertheless, the overall reduction makes it difficult to design for any high HBM or CDM levels. This is further elaborated in Figure 12.

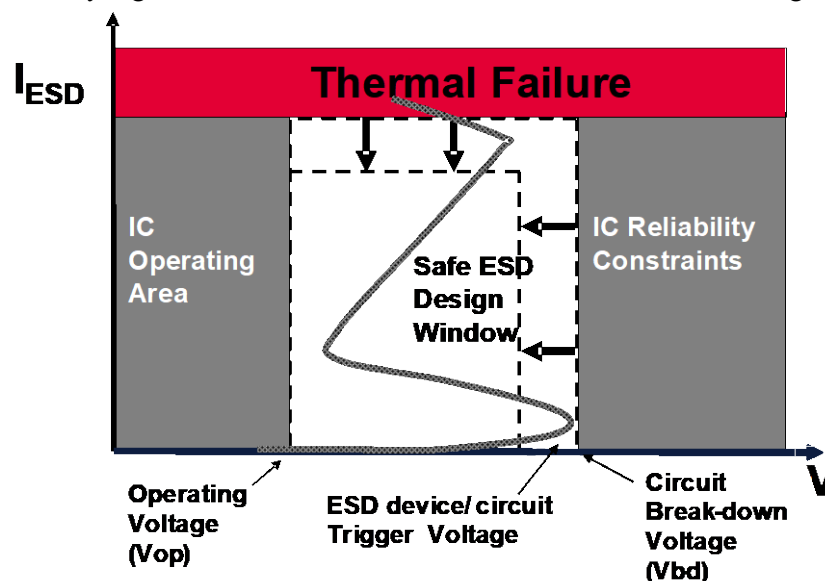


Figure 11 — ESD Design Window Definition

5.5.2 Impact of the ESD Design Window on CDM (cont'd)

Figure 12 shows how the ESD design window (V_{bd} minus V_{op} , defined in Figure 11) has scaled going from 350 nm down to 12 nm technology nodes. The design window has shrunk by approximately 2.9X scaling from 350 nm down to 12 nm while the ESD targets have not kept pace with this scaling. The ESD design window reduction requires either larger ESD devices to clamp the voltage to lower levels or it requires significant innovation in ESD devices as technologies scale. Increasing the ESD device sizes to compensate for the design window scaling is not practical for two main reasons: 1) the area allocations for ESD devices/circuits are scaling down at each technology node, and 2) the capacitive loading requirements are simultaneously also being reduced for each new technology generation.

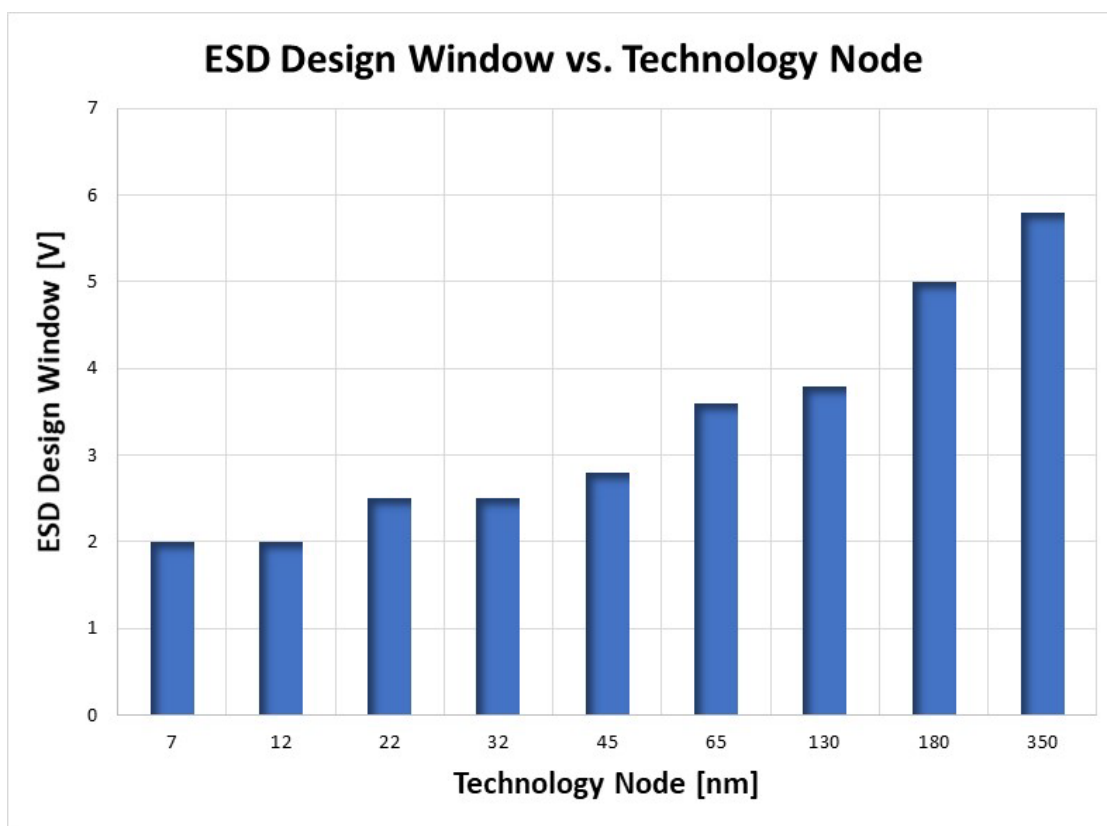


Figure 12 — The ESD Design Window versus Technology Node

5.5.3 Impact on HSS, RF and Analog Applications

In Figure 13 the acceptable ESD capacitive loading is shown for targeted HSS link data rates. The capacitive load of a high-speed data lane has a strong impact on the quality of the eye and the power per Bit. With increasing data rates the acceptable capacitive load declines more and more. However, the concept of the data rate of a SERDES link needs to be carefully assessed, when parallel lanes are used. Actually, the critical parameter is the data rate per lane, which depends on the Nyquist frequency and the modulation standard. The widely used modulation approach for interface speed below 56 Gb/s is NRZ (non-return-to-zero) standard. At 56 Gb/s and above the PAM4 modulation standard was introduced. The latter compresses the eye height and is more sensitive to degradation of the eye due to capacitive load. An increase of the Nyquist frequency to 56 GHz and above creates even a higher sensitivity to a capacitive load of the ESD protection.

5.5.3 Impact on HSS, RF and Analog Applications (cont'd)

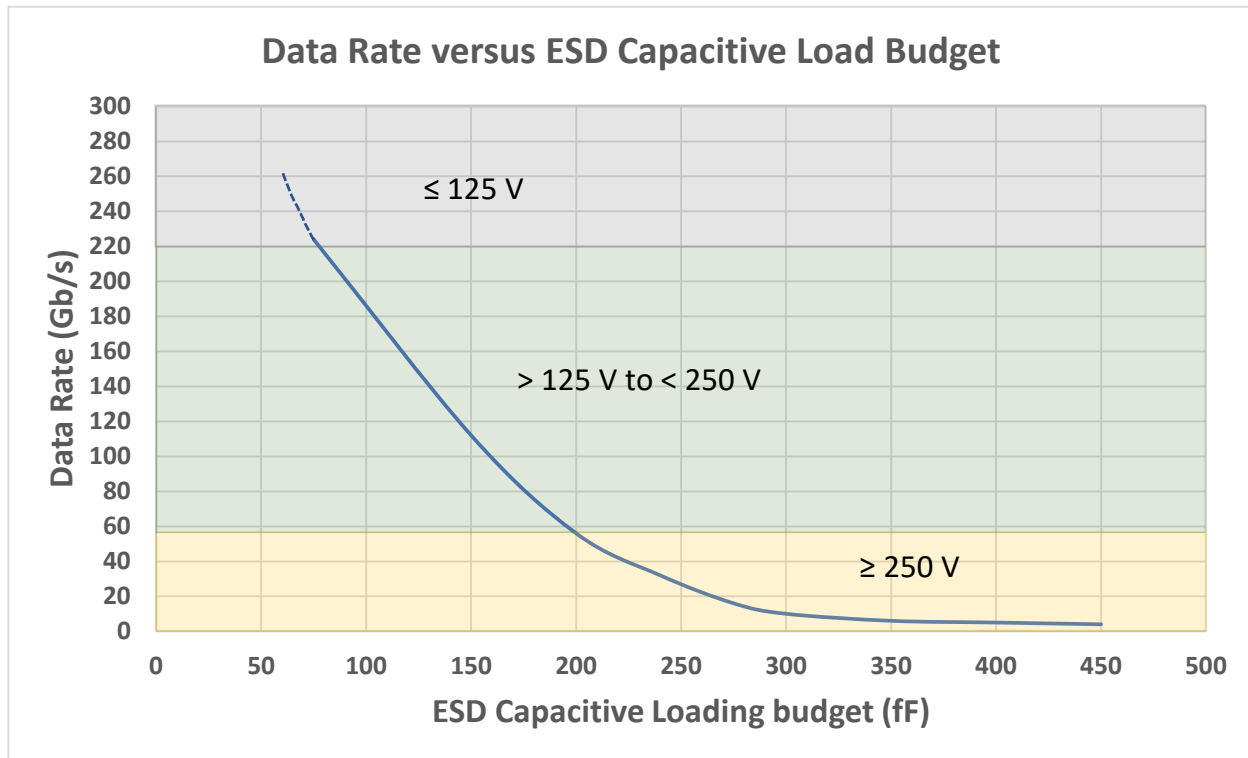


Figure 13 — Data Rates of single lane SERDES vs. Allowed ESD Capacitive Loading Budget of high-speed IO circuits. NRZ SERDES interfaces are considered up to 56 Gb/s. At 56 Gb/s and above PAM4 is assumed.

RF high-speed designs are even more restrictive than standard high-speed SERDES designs. For RF pins with 5-10 GHz performance requirements, ESD design can be quite a burden. The low noise amplifier (LNA) input circuits are especially intolerant to ESD protection device capacitance. In these circuits, the ESD ground is often isolated from the LNA ground and separated by diodes as shown in Figure 14. With the usual requirement of less than 100 fF capacitance for the ESD diodes, it is difficult to achieve even 1000-volt HBM protection without damaging the gate oxide. This is mostly due to the on-resistance of the small protection diodes used to meet the circuit RF functional requirements. CDM performance can be even more challenging than HBM for these RF applications.

5.5.3 Impact on HSS, RF and Analog Applications (cont'd)

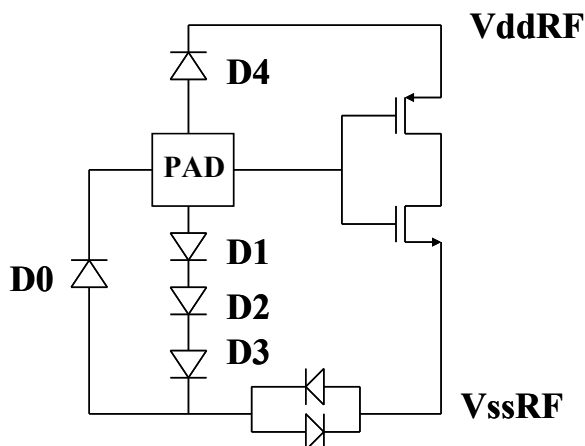


Figure 14 — Typical Low Noise Amplifier (LNA) pin with diode protection.

The reasons for the low CDM performance are: 1) absence of secondary clamp, 2) smaller sized protection diodes that build up the voltage to critical levels even for small CDM currents, and 3) isolation of the ESD clamp ground from the RF buffer ground. Regarding restriction #2 the situation could become worse if the input pad is directly connected to the core gate oxide in order to achieve high-speed input performance. The clamp diodes must be smaller in size to meet the low total capacitance budget at the pin.

RF pin application chips with system on chip (SoC) function usually employ small ball grid array (BGA) packages of 8 mm X 8 mm or 10 mm X 10 mm. The peak currents are quite low, not more than 3-4 amperes at 500 volts. However, these sensitive RF designs with small clamps can often only be effective for CDM current levels of 2 amperes or less, thus severely limiting their CDM performance to 200-300 volts. For example, for an RF application chip with 10 mm X 10 mm package size the LNA input ESD design can only handle 2 amperes which corresponds to only a passing level of about 200 volts.

5.6 Package Effects and Package Trends

Advances in packaging technology are based on the requirements of the different market segments [32]. For computer applications, advances are based on performance and reliability. While for the consumer market it is more about the form factor, price, and robustness. For automotive and military applications, it could be temperature sensitivity and reliability. Each type of package is then designed and selected according to the application. This proliferation has gone from the standard dual-in-line (DIP) packages to multi-chip modules (MCM) and to flip-chips and stacked die or even stacked packages. In the past few years, wafer-scale packages (WSP) have also become more common.

Although not particularly considered in the past or even at present, during the package development some attention should also be given to the ESD effects as well. The aggressive technological advances into newer types of packages might very well determine the achievable ESD performance for overall adequate reliability.

5.6 Package Effects and Package Trends (cont'd)

The most serious impact that packages have is on CDM where its performance strongly depends on the package type and package lead design. If the qualitatively assessed CDM risk is now imposed the TQFP package might pose lower CDM performance while the micro-star BGA (u*BGA) can show relatively better CDM performance. This is simply related to the peak current that is discharged during the stress and directly depends on the effective package capacitance. Some of the most significant impacts of packages on CDM would come from a variety of packaging factors. What could influence the CDM peak current and hence the CDM performance is summarized for a BGA package below:

- The die size where larger die would mean more capacitance
- The mold compound material and its thickness
- The lead frame metal routing including the number of pins

Chips with larger die sizes that incorporate larger packages would naturally pose a larger threat to CDM design. For example, the measured peak current at 250 volts as a function of the package area is shown in Figure 15 (scaled from 500 volts) [33].

While the HBM current at 1000 volts is independent of the package size, the CDM current rapidly increases with package area. Note that trend, extended out to very large packages in the $> 5000 \text{ mm}^2$ would near 6 amperes.

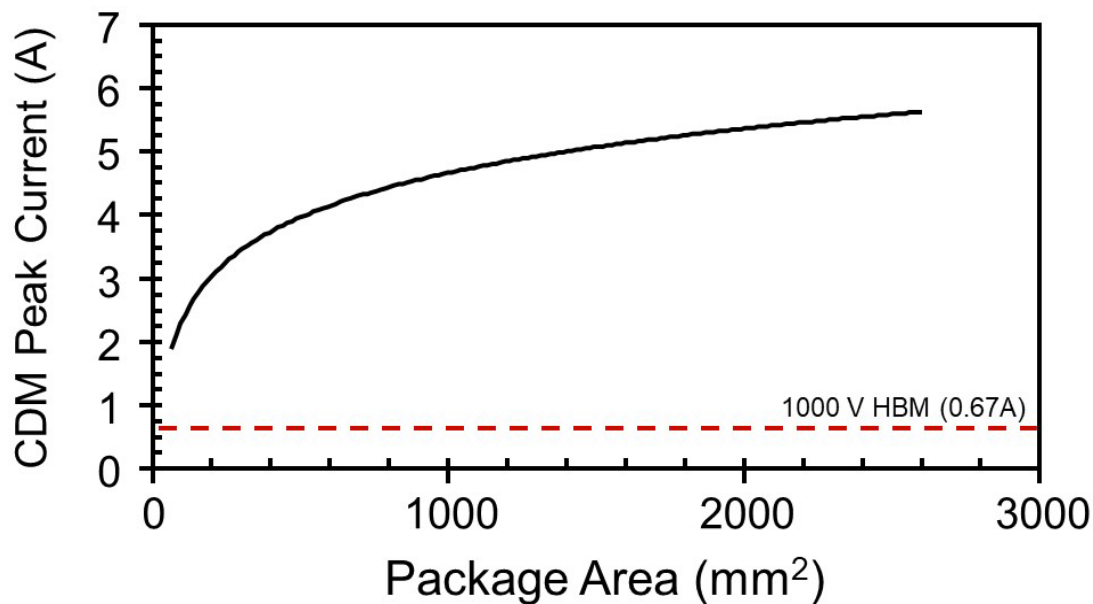


Figure 15 — CDM Peak Current data for BGA packages at 250 V CDM.

The most critical design constraint for CDM comes from the trend towards higher pin count packages. This market is driven mostly by ICs for internet switching (with high bandwidth) and microprocessors where very high pin count packages are commonly used. This bandwidth can be achieved by incorporating a balance between high-speed I/O's and wide parallel busses. Designs for such markets use chip-to-chip interfaces with DDR4 (1600 MHz), RLDRAM (1600 Mbps), and SERDES (112/224 Gb/s).

5.6 Package Effects and Package Trends (cont'd)

Although the trend for increased off-chip speed may reduce the number of I/O's required, it also leads to a higher number of power pins for thermal performance. The net result is an increase in the average pin count. This continued trend for high pin count is depicted in Figure 16 for BGA packages. With the advancement of 2.5D and 3D technologies, package sizes continue to grow. By 2016 pin counts were over 5000 and in 2020 they are nearing 6000. At this pin count, the package area is well above 5000 mm². Indeed, both the die area and the package area contribute to increased CDM peak current at a given voltage stress level. Invariably designs requiring high-speed I/O's tend to be placed in IC packages with high pin count which consequently places a constraint on the CDM design capability.

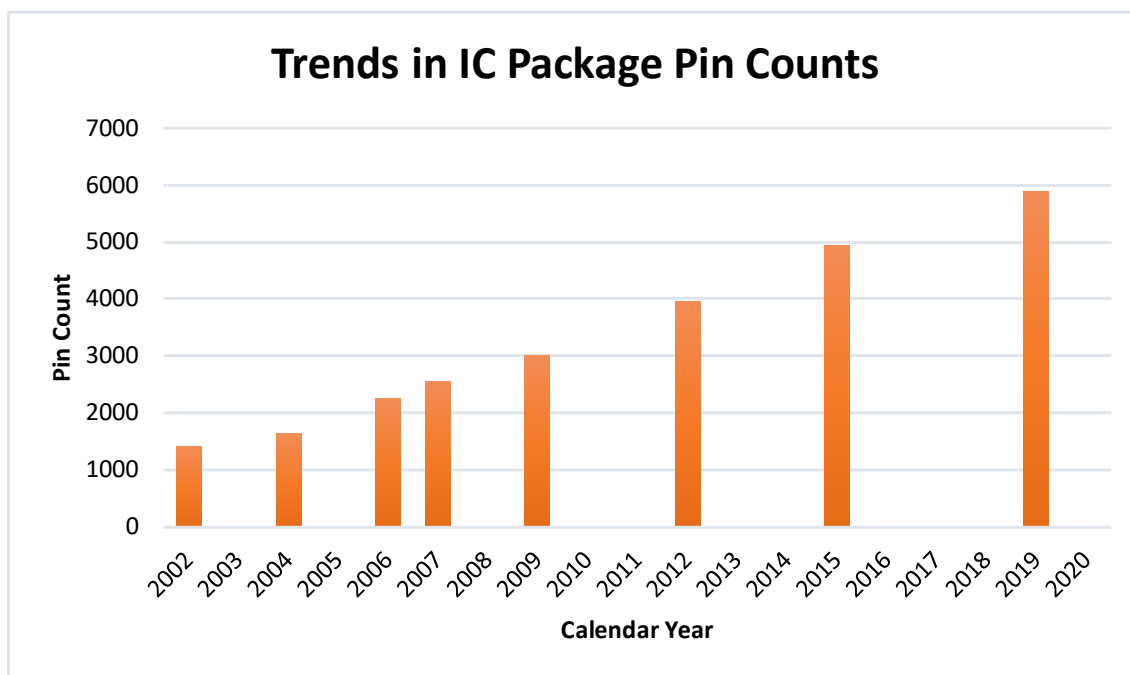


Figure 16 — Trend for high pin count BGA Packages

Meeting a 500 volt CDM level, or even a 250 volt CDM level for very high-speed pins, for larger packages will in general not be possible. The more realistic design windows for CDM for package sizes exceeding 1000 mm² are shown in Figure 17. First, it is seen the CDM peak current increases as the package area increases (assuming the same thickness package) and that this behavior linearly moves to higher current levels at higher stress levels. For example, a 1000 mm² BGA would produce 4 amperes at a 200-volt stress level and more than 10 amperes at a 500-volt stress level. However, the practical design windows dictated by circuit performance would limit the achievable CDM level. For the 65 nm HSS I/O designs with speeds of 5-20 Gb/s, the peak current in the ESD design is restricted to between 2.5 to 6 amperes. This is shown by the blue box in Figure 17. At the 45 nm node, this would degrade to the 2 to 5 ampere range, further lowering the achievable CDM levels. Figure 17 clearly illustrates that for these HSS designs with large package areas the CDM performance is limited to between 200 and 300 volts.

5.6 Package Effects and Package Trends (cont'd)

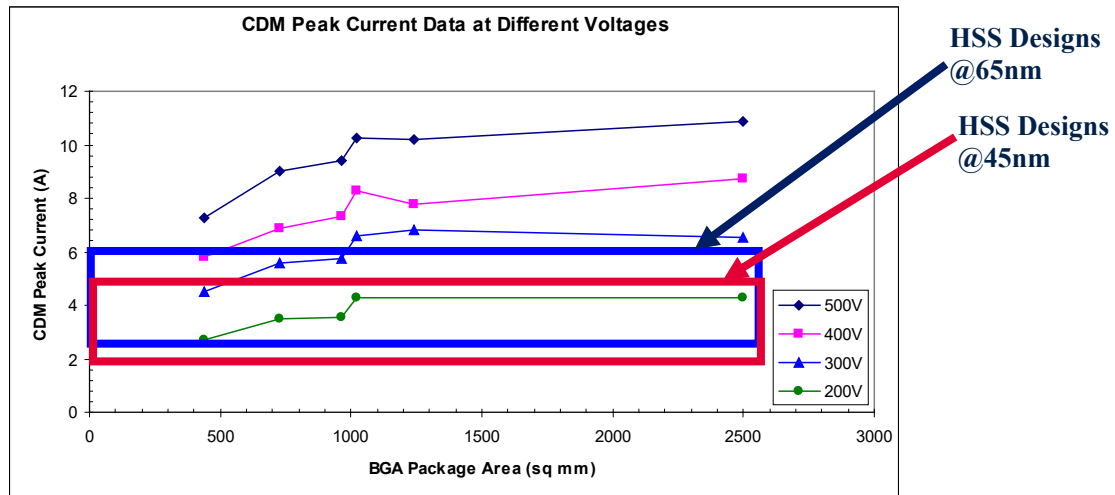


Figure 17 — CDM Peak Current data for various packages at various CDM stress levels.

In this manner, we can see that as chip sizes are made larger and built-in complex packages with many more pins (>2000) the CDM stress current will continue to increase in magnitude. Combined with the package effects presented here, RF designs that can tolerate very little capacitance from the protection device will have difficulty meeting the ever-larger CDM currents. In the future, CDM package issues will become worse for stacked packages and multi-chip modules. Moreover, conversion to new organic materials for environmental safety could potentially exacerbate the situation. Therefore, package engineers and ESD engineers need to work in close collaboration to maintain package performance and ESD reliability!

5.7 ESD Designer's Perspective on Realistic CDM Targets

The overall expected performance for CDM while meeting all of the design constraints is already challenging and, in the future, will become even more of a challenge. In order to understand this, we need to examine the total picture of the IC packages ranging from small pin count (<100) to medium pin count (300-500) and high pin count (500 to >1000) ranges. This package map is illustrated in Figure 18. The top row shows the package type trends as they progressed from DIP to BGA to LGA. It is expected that the trend toward a higher percentage of packages being BGAs will continue for the foreseeable future. The second row shows the corresponding number of pins. Based on physical data the markers for the package areas corresponding to the package pin numbers are shown in the third row. After measuring actual peak currents at various stress levels for the different package areas (pin count) the estimated CDM performance chart for different I/O designs is shown. This data was generated by measuring the CDM discharge currents from various sized packages with design constraints defined in terms of maximum tolerable current levels in each case. For example, if a practical I/O design with its CDM protection design can handle 8 amperes of peak current, for pin counts up to 1000 the previously accepted CDM level of 500 volts can be met. But if the pin count goes beyond 1000 to nearly 2000, the CDM performance can only be about 400 volts. These numbers currently reflect 45 nm and 65 nm technologies. The next row for high-speed I/O designs shows that packages devices with >200 pins or a package area of >250 mm² cannot meet the same expected 500 volts. It should be noted here that beyond 2500 pin packages the performance data is only an extrapolation based on the known relation between package area (capacitance) and the CDM peak current as a function of stress voltage.

5.7 ESD Designer's Perspective on Realistic CDM Targets (cont'd)

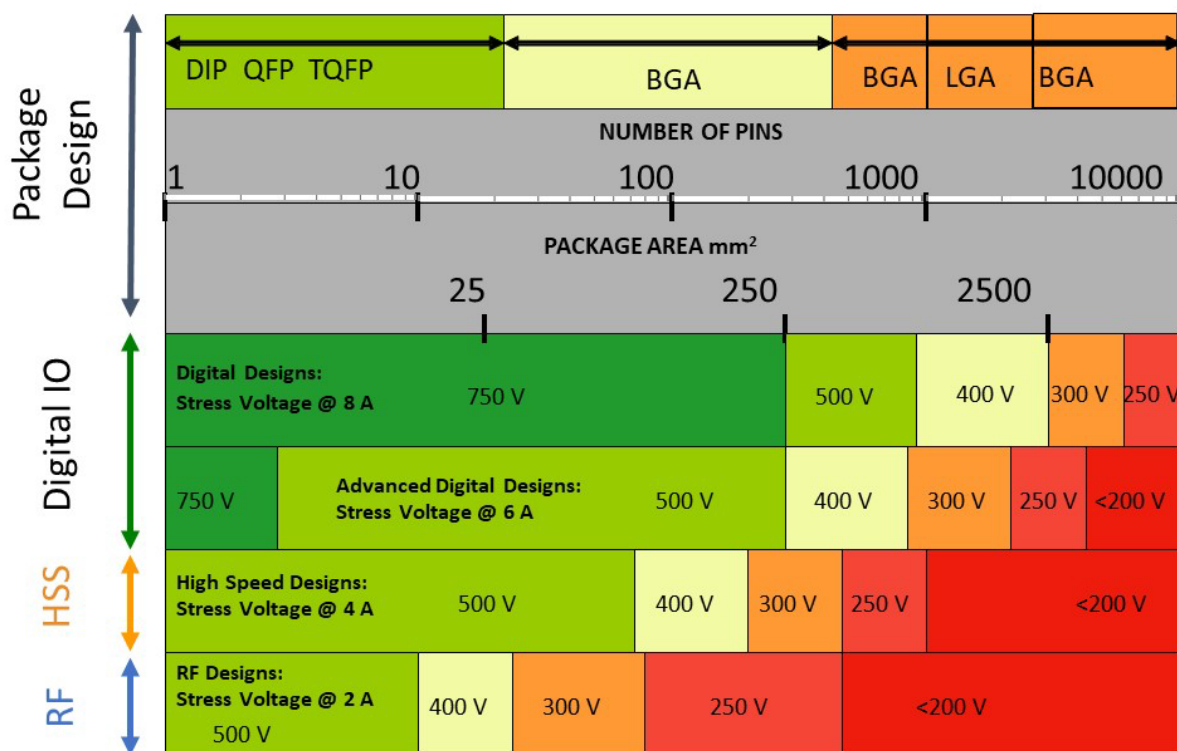


Figure 18 — CDM package map for 65 nm and 45 nm designs. Products with >1000 pins or 1200 mm² area are limited to 400 V CDM passing voltage for all practical designs; this would reduce to 300 V for high speed Serdes designs.

Following this trend, the CDM performance restriction faced by RF designs is indicated in the last row of Figure 18. Since most of the RF designs tend to be in smaller IC packages, they are not expected to face the severe degradation of performance as the high-speed serial link (HSSL) I/O's. However, even at smaller package areas, the RF pins are sensitive for CDM design as noted in Sub-clause 5.4.3 and thus are challenged to meet a 250-volt level for packages with even 300 pins.

5.8 Further Technology Scaling Effects and Additional Impact to Realistic CDM Targets

At 22 nm technologies and beyond, even a 250-volt level will place more severe restrictions on CDM protection design due to further scaling effects and the drive towards higher circuit speed performance at data rates exceeding 56 Gb/s. A revised package CDM map for the 22 nm and beyond is shown in Figure 19.

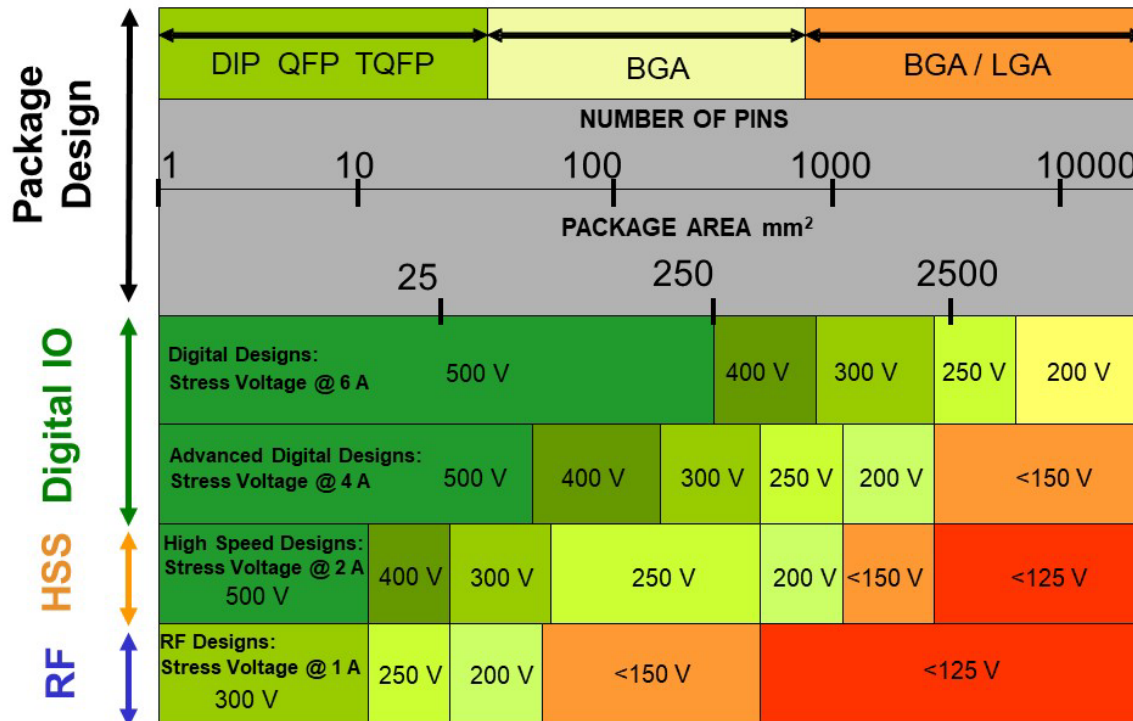


Figure 19 — CDM package map projected for 22 nm designs. Products with >1000 pins or 1200 mm² area would be limited to <150 V CDM passing voltage for all HSS and RF designs.

5.9 High Speed/RF Circuits, Scaling Impact on CDM Targets

As data rates of high-speed I/O interfaces continue to increase, this comes with the challenge of requiring reduced capacitances for ESD devices [34]. Reduced capacitances typically drive smaller ESD devices [34]. Technology scaling, in general, is driving larger area ESD devices when disruptive technologies like FinFETs come along as shown in Figure 20. In Figure 20, technology scaling from 130 nm down to 28 nm used standard planar CMOS, with the switch to FinFET based bulk CMOS technologies in 14 nm and 7 nm. The larger area in 14 nm and 7 nm also drives larger capacitance ESD devices as shown in Figure 21. Also shown in Figure 21, from 130 nm to 32 nm the capacitance increases a maximum 2X in 32 nm due to increased well doping to control FET short channel characteristics (device sized to meet 5.5 amperes using 1ns TLP failure current). However, as technologies moved to FinFET based on 14 nm and 7 nm this capacitance increase was 4-5X larger due to significantly less silicon volume in the same cross-sectional area compared to a 130 nm planar technology.

5.9 High Speed/RF Circuits, Scaling Impact on CDM Targets (cont'd)

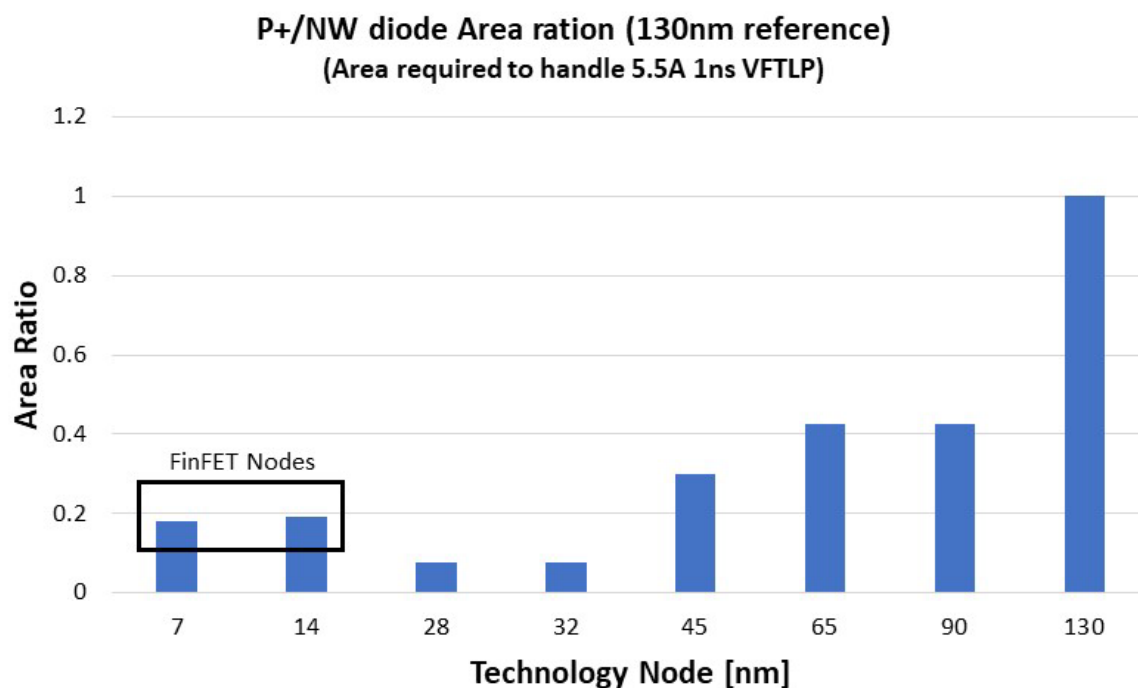


Figure 20 — ESD diode area required to achieve a 1ns TLP 5.5 A failure current versus Technology Node (ratio values referenced to 130 nm)

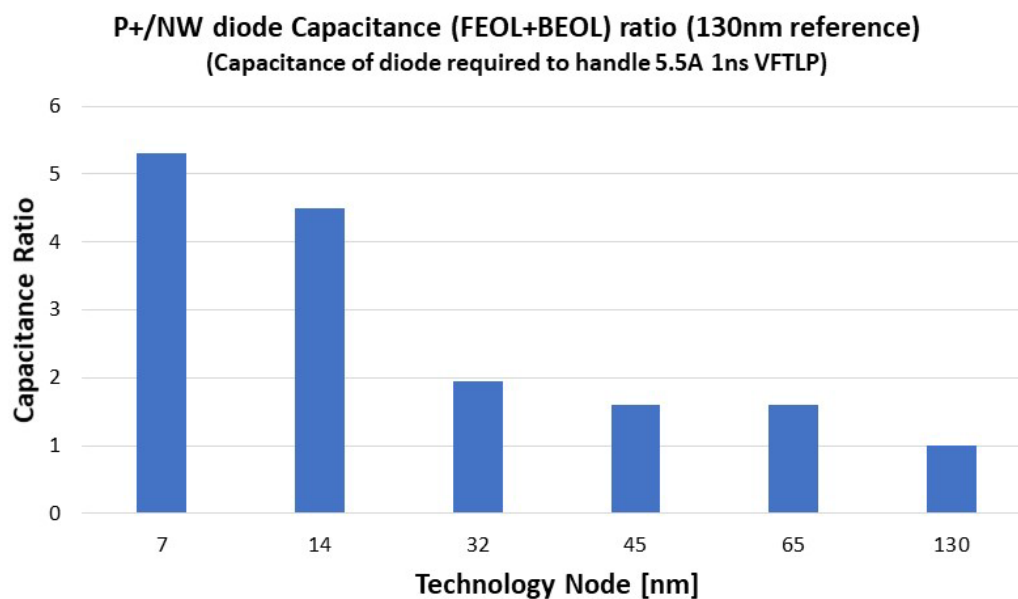


Figure 21 — ESD diode capacitance vs. Technology Node (diode sized to achieve 1ns TLP 5.5A failure current) (ratio values referenced to 130 nm)

5.9 High Speed/RF Circuits, Scaling Impact on CDM Targets (cont'd)

5.9.1 Data Rate/Frequency Scaling Challenges

As technologies continue to scale, so do the data rates/operation frequencies of various types of I/O interfaces. For example, if we refer to Figure 22 below, we can see the HSS link data rates have increased from ~10 Gb/s in 90 nm to ~112 Gb/s in 12 nm and to >200 Gb/s in 7 nm with continued data rate increases beyond 7 nm technology nodes expected. The data rates come from currently offered IP in the industry. From 90 nm down to 12 nm there has been greater than a 10X increase in data rates.

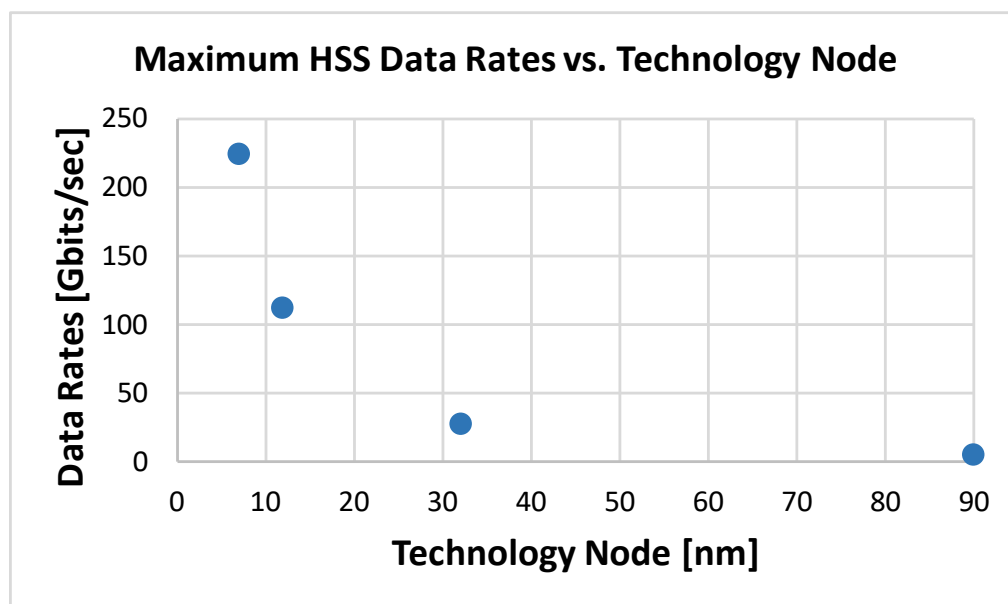
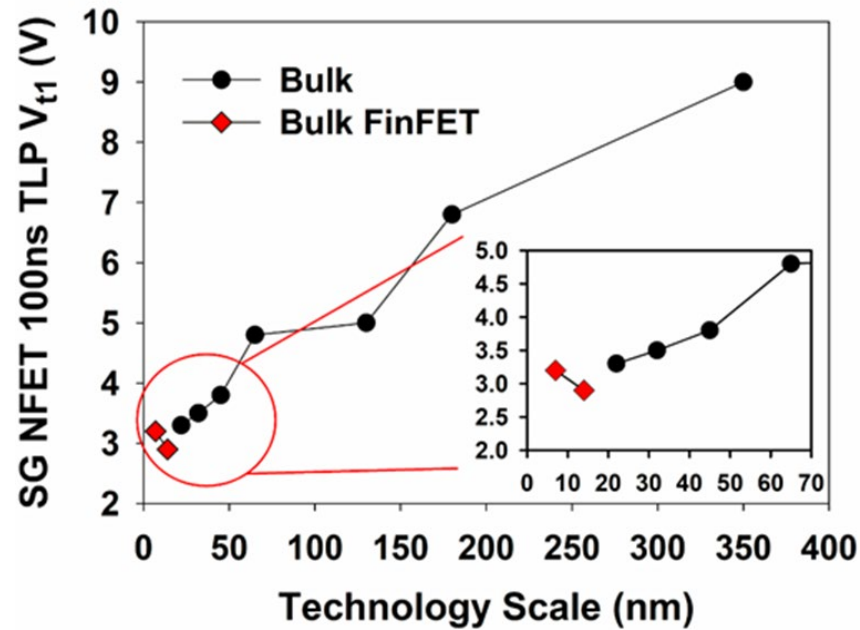


Figure 22 — HSS data rate scaling versus technology node.

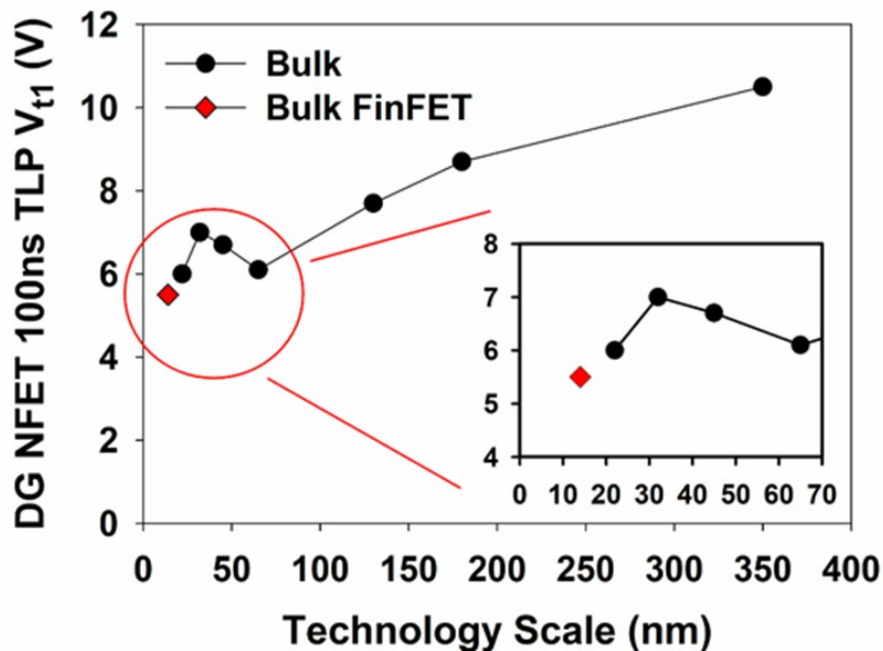
5.9.2 ESD Design Window Scaling as Technologies Scale

As bulk CMOS Technologies scale from 350 nm down to 7 nm thin-oxide (SG – single gate) NFET V_{t1} reduces from ~9 volts down to ~2.8 volts reducing the design window by nearly 3X, this can be seen in Figure 23A. In the same technology generations, thick-oxide (DG – dual gate) NFET V_{t1} reduces from ~10.5 volts down to ~5.5 volts, nearly a 2X reduction in the design window as shown in Figure 23B.

5.9.2 ESD Design Window Scaling as Technologies Scale (cont'd)



(A)

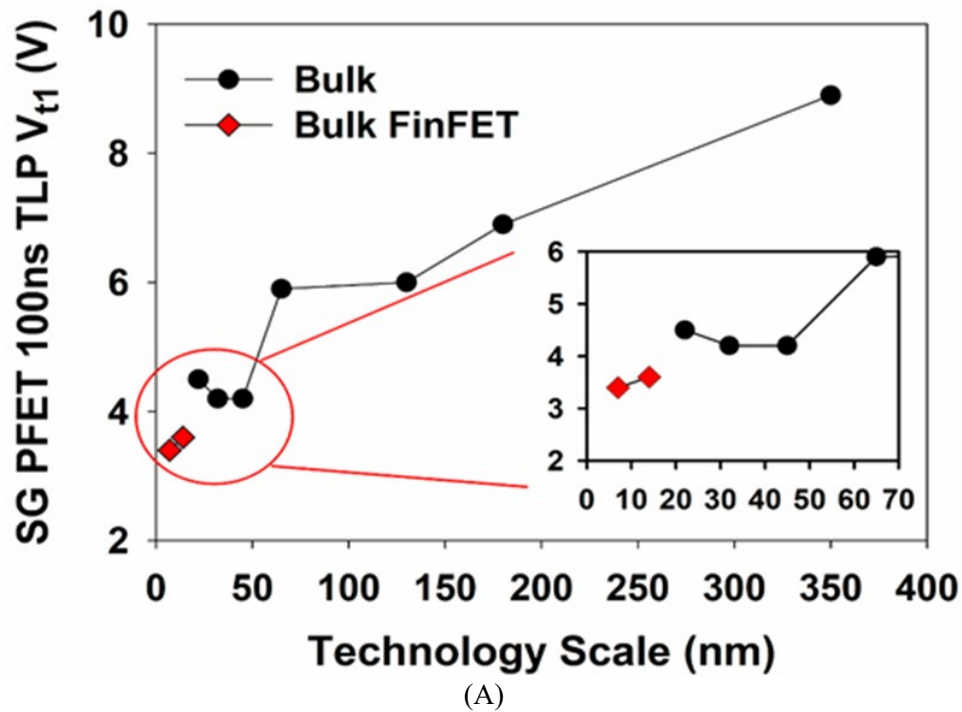


(B)

Figure 23 — A) Thin-oxide (SG) NFET trigger voltage V_{t1} vs. Technology Node B) Thick-oxide (DG) NFET trigger voltage V_{t1} vs. Technology Node

5.9.2 ESD Design Window Scaling as Technologies Scale (cont'd)

For the thin oxide (SG) PFET the V_{t1} reduction from 350 nm down to 7 nm is shown in Figure 24A where the V_{t1} is shown to reduce from ~9 volts down to ~3.5 volts. In Figure 24B the V_{t1} of the thick oxide (DG) PFET shows a reduction from ~12 volts down to ~5.8 volts.



5.9.2 ESD Design Window Scaling as Technologies Scale (cont'd)

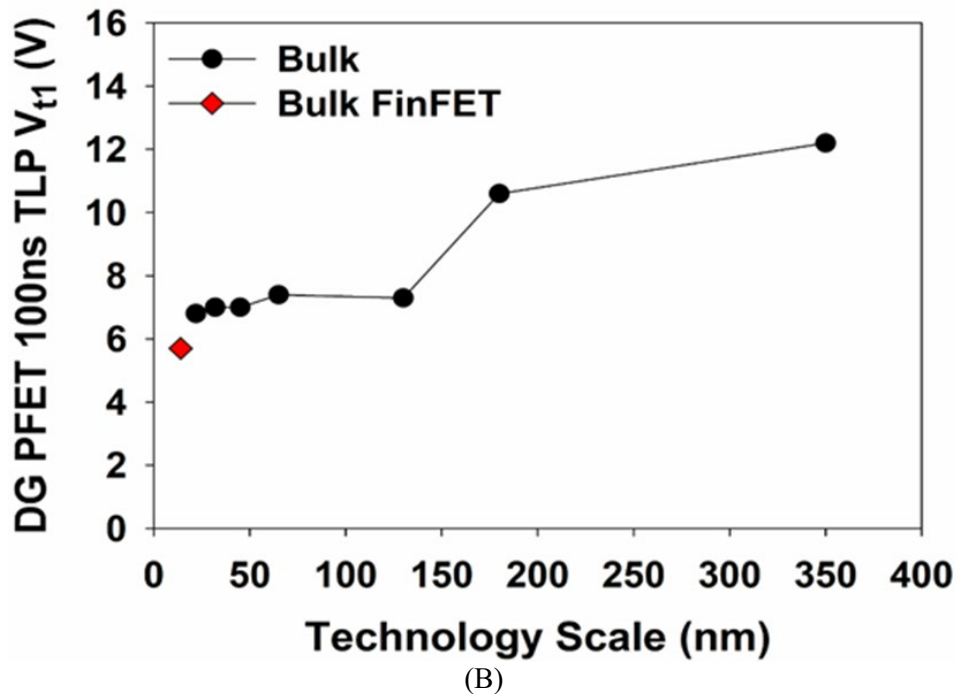


Figure 24 — A) Thin-oxide (SG) PFET trigger voltage V_{t1} vs. Technology Node B) Thick-oxide (DG) PFET trigger voltage vs. Technology Node

Figures 25A and 25B show the 100 ns TLP thin oxide and thick oxide NMOS breakdown voltages respectively under worst-case oxide breakdown gate biasing polarities. Figure 25A shows the thin-oxide (SG) NMOS 100 ns TLP breakdown voltages from 350 nm down to 7 nm is reduced from ~19 volts to ~2.8 volts. Figure 25B shows the same technology range but for the thick-oxide (DG) NMOS which reduces from ~22 volts down to ~6 volts.

5.9.2 ESD Design Window Scaling as Technologies Scale (cont'd)

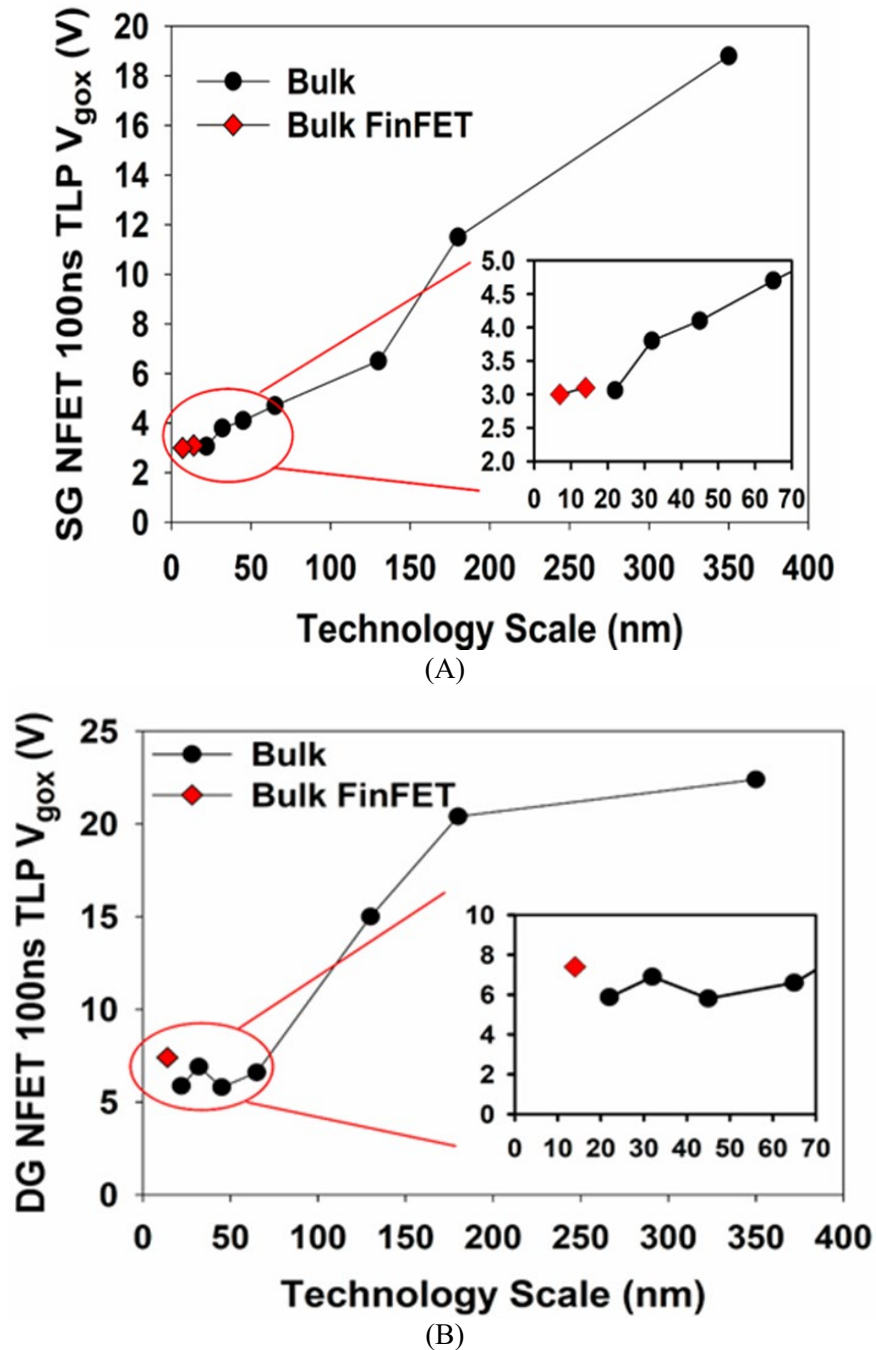


Figure 25 — A) Thin oxide (SG) NFET 100 ns TLP Oxide Failure Voltage (V_{gox}) vs. Technology Node B) Thick oxide (DG) NFET 100 ns TLP Oxide Failure Voltage (V_{gox}) vs. Technology Node

5.9.3 Estimation of What CDM Targets Designs Can Handle for High-Speed Interfaces in 7 nm and beyond

The worst-case scenario is a large package IC using thin-oxide I/Os where the high-speed performance doesn't allow for series resistors and secondary ESD protection. In a simple diode-based and RC-Clamp ESD architecture and assuming a bussing resistance of $0.1\ \Omega$ (very aggressive) we can come up with a rough estimation of the amount of current during a CDM event these I/O interfaces can withstand without reaching failure. Consider the CDM current path depicted in Figure 26.

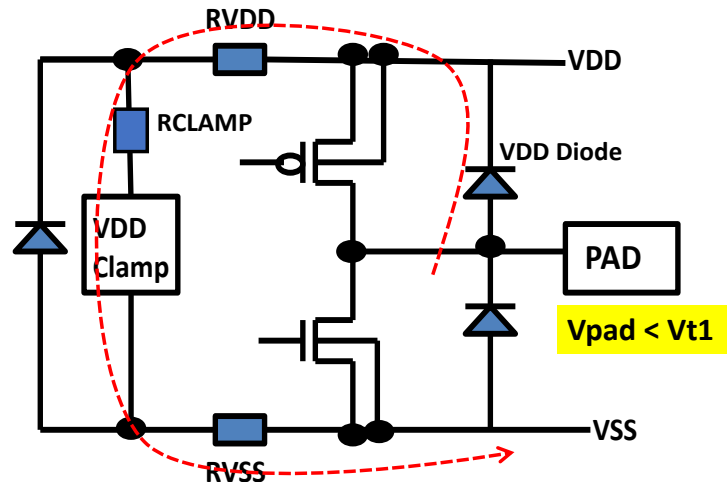


Figure 26 — Rail clamp design where for a given CDM discharge current the voltage buildup at the pad (V_{pad}) must be lower than V_{t1} to protect the output buffer device.

Assumptions (worst-case 7 nm design):

$V_{diode_on} = 1.0\ \text{volt}$

$R_{diode_on} = 0.2\ \Omega$

$RV_{dd_buss} = 0.1\ \Omega$

$RV_{ss_buss} = 0.1\ \Omega$

$V_{rcclamp_on} = 0.5\ \text{volts}$

$R_{rcclamp_on} = 0.1\ \Omega$

$R_{series_IO} = 0\ \Omega$

$V_{t1_thinox_7\ \text{nm}} = 3.2\ \text{volts}$ (note: device fails at the trigger point of V_{t1})

Large package giving CDM current of 2 amperes / 100 volts

- $V_{pad} = V_{diode_on} + (R_{diode_on} * I_{cdm}) + ((RV_{dd_buss} + RV_{ss_buss}) * I_{cdm}) + V_{rcclamp_on} + (R_{rcclamp_on} * I_{cdm})$ where V_{pad} in this example must be $\leq 3.2\ \text{volts}$
- $3.2\ \text{volts} = 1.0\ \text{volt} + (0.2\ \Omega * I_{cdm}) + (0.2\ \Omega * I_{cdm}) + 0.5\ \text{volts} + (0.1\ \Omega * I_{cdm})$.
- $I_{cdm} = 3.4\ \text{amperes}$ which leads to $V_{cdm} = (3.4\ \text{amperes} / 2\ \text{amperes}) * 100\ \text{volts} = 170\ \text{volts}$ (best case)

Based on a large package that gives 2 amperes per 100 volts of CDM voltage, using very aggressive on-resistances for RC_clamp, RV_{dd_buss} , and RV_{ss_buss} which are all at $0.1\ \Omega$ (the best-case scenario), the best we can achieve is a 170 volt CDM target level. Given that we should include some margin ($\sim 10\%$), a realistic CDM target is 125-150 volts for high speed/RF interfaces in 7 nm and lower technology nodes.

6 CDM Related ESD Control in Assembly Lines

6.1 Motivation

The ESD robustness of semiconductor devices against discharges according to the human body model (HBM) and against discharges of isolated conductors is continuously trending to lower values [2]. There is a general concern by many companies that they cannot handle these sensitive devices. However, if ESD-protective measures in the assembly lines are set up according to international standards such as ANSI/ESD S20.20 [4], IEC 61340-5-1 [5], or JEDEC JESD625 [6], these devices can be handled without any adverse effects from HBM (see also [1]). The current editions of both standards are reasonably well aligned and provide rules for the safe handling of “electrical or electronic parts, assemblies and equipment susceptible to damage by electrostatic discharges greater than or equal to 100 volt human body model and 35 volts on isolated conductors” (taken from ANSI/ESD S20.20).

The Industry Council on ESD Target Levels recommends HBM target levels of 1000 volts for products [1]. Typically, this HBM target is met if a certain level of charged device model (CDM) robustness is designed into the product. Therefore, one does not have to expect ESD failures related to the human body and isolated conductors if an ESD program is implemented that follows one of the above referenced international standards.

However, these hazards are only two of the risks that can be found on an assembly line. It is also necessary to prevent the charging by triboelectricity or induction and subsequent “hard” grounding of electrostatic discharge sensitive (ESDS) items, resulting in a CDM-type ESD event. For integrated circuits, ANSI/ESD S20.20 and IEC 61340-5-1 require a CDM-robustness of 200 volts or greater to allow safe handling, leaving little margin to the recommended target of 250 volts as recommended in the earlier version of JEP157 [35].

The EOS/ESD Association’s Technology Roadmap for Semiconductors provides a trend chart for CDM robustness [2]. There are more and more products for which the CDM robustness will fall below the 200-volt limit and, hence, will require additional ESD control measures.

What do international standards require to avoid CDM-like ESD hazards? Many of the basic ESD protection measures for HBM protection also protect against CDM-related problems, although they would not be called special CDM protection measures. Examples of these are wrist straps or dissipative table mats. If an operator is not grounded, he can induce a charge on a device or PCB without directly damaging it by a discharge when contacting the ESDS item. But when the device or PCB in the electrostatic field of the charged operator is placed on a metal surface, it could be damaged by a CDM-type discharge. On the other side, a grounded dissipative table mat avoids dangerous potential differences between various items in the production area, and, thus, reduces the risk of damage in the case of a hard discharge of the charged ESDS item. It is therefore also a CDM protection measure.

Many examples like these can be found. The situation is summarized in Figure 27, which shows that basic CDM protection is already part of the basic ESD protection process that is in place in most EPAs worldwide.

6.1 Motivation (cont'd)

Additional to the “inherent” CDM protection measures which primarily address HBM risks, international standards require the removal of non-essential insulators that can become highly charged and require a strategy on how to handle process required insulators as a CDM-specific ESD control measure. The limits set for electrostatic fields of the charged insulator at the location where the ESDS item is handled or the surface potential of the process required insulators are said to allow safe handling of ESDS devices with a CDM robustness of 200 volts or greater [4, 5].

However, with a continuously increasing number of devices with at least some pins falling below this limit, following the requirements of both ESD control standards might not be enough to prevent ESD damage. Detailed process analysis must be conducted to assess the ESD risk in the process and determine the most efficient mitigation techniques. Such an ESD process risk assessment requires personnel with advanced knowledge and experience with electrostatic measurements and advanced measurement technologies. Assessment of any risk induced by a charged ESDS item or electrostatic field is briefly explained in this document in the following sections by some examples. Sub-clause 6.2 describes the ESD process assessment flow based on the basic ideas of charging and hard discharges. Several successful approaches to CDM-like process risk assessment and risk mitigation have been published and will be discussed in Sub-clause 6.2.2 after a brief introduction to the systematic approach of the basic ESD assessment flow. Sub-clause 6.3 discusses the approach of process capability and transition analysis. The case studies give the end-user good examples and ideas of a systematic approach. This includes how to analyze a CDM-like risk or the process capability of the respective production line and how a process can be analyzed to avoid CDM-like failures. Sub-clause 6.4 describes the approach for an ESD process assessment based on ANSI/ESD SP17.1 [3])

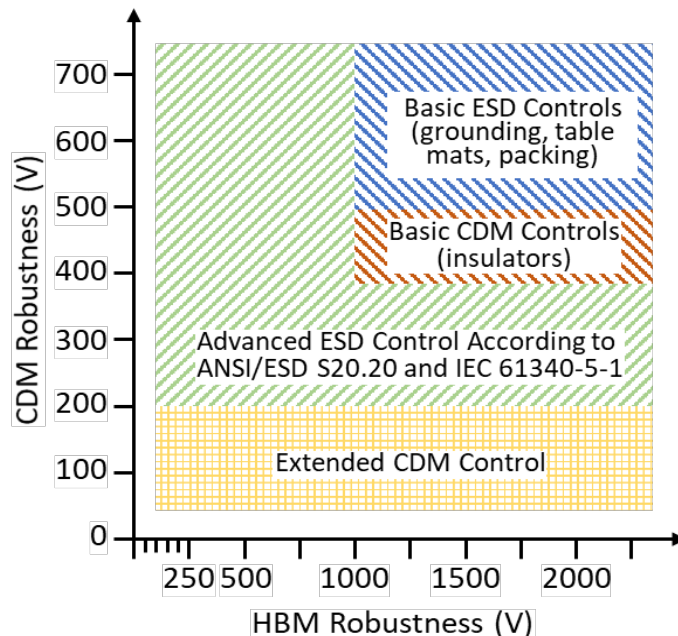


Figure 27 — Relationship Between General ESD Control and CDM Specific Control

Note: Robustness levels are for rough guidance only

6.2 Basic Idea of CDM Protection and Process Related Risk Analysis

Many processes, particularly in assembly and test, cause charging of the ESDS item to take place, either by triboelectric charging of the ESDS item or by charging by induction of the ESDS item in an electrostatic field of a near-by process required insulator. However, charging the ESDS item itself is not critical as it will not result in damage to the ESDS item. In many process steps, charging either by a triboelectric effect or induction cannot be avoided. “Hard” discharges of the ESDS item must be avoided in each process step. A hard discharge is a discharge through a low ohmic contact; it is the most severe discharge as compared to a discharge through a higher resistance contact (see definition in ANSI/ESD SP17.1 [3]).

There are several possible ways to analyze a CDM-like risk (see, for example [36-38]). The very basic idea of this approach is shown in Figure 28.

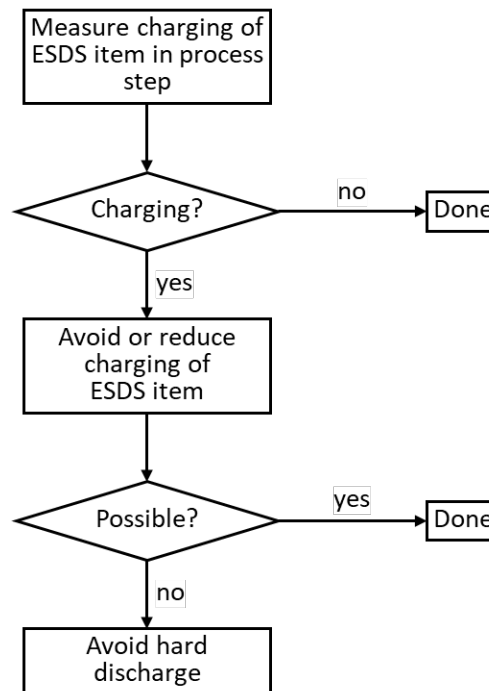


Figure 28 — Basic ESD Assessment Flow for CDM-like Risks

6.2.1 Systematic Approach

While investigating device and PCB charging, it must also be considered whether these charging values are dangerous for the ESDS item. That means, it must be determined whether the charged ESDS item experiences a low ohmic contact to ground or contacts another conductive object at a different potential. Both scenarios are a hard discharge that can cause a dangerous CDM-type event. If that is not the case, the charging will normally not cause any damage to the object – electrostatic problems like the attraction of particles by charged objects will not be discussed here.

6.2.1 Systematic Approach (cont'd)

These considerations result in an analysis of every single process step by asking the following questions:

- Is there charging of the object being processed?
- Is there a chance for a hard discharge in this or the next process step?

If there is no charging, there is consequently no possibility for a hard discharge. If there is no hard discharge, there is normally no possibility of CDM damage.

6.2.2 Theoretical approach

The approach will be explained in some simple examples that can happen in a typical PCB assembly line [36]:

- 1) An uncharged PCB is transported on a conveyor belt from process step A to process step B in a closed tunnel. In order to be able to view inside the tunnel, the cover is made of a transparent material. To keep costs low the cover is made of insulative, highly chargeable Plexiglas. While the (initially neutral) PCB is running underneath the highly charged Plexiglas, the electrostatic field of the Plexiglas results in a charge separation on the conductors of the PCB. This is by itself not damaging the PCB! If the PCB exits out of the charged transport tunnel without having experienced a metallic contact (or an arc to a nearby piece of metal), the charges recombine, and a neutral undamaged PCB arrives at the next process step.

NOTE The use of a grounded, dissipative cover prevents the charging of the cover and therefore avoids the field-induced charge separation on the PCB. This makes the risk analysis much easier but is not absolutely necessary.

- 2) The same uncharged PCB now comes to a process step where it becomes charged. A possible example is when a charged barcode label is attached to the PCB, or when the PCB is held in place by a bar or stop at the end of a conveyor while the conveyor belt continues to run and charges up the PCB by rubbing (tribocharging). Such processes can charge the PCB to several hundred volts. If the metal parts of the PCB, for example, connectors or metal lines, are not contacted by or are not coming close to a grounded conductive object, there is no risk for a hard discharge or arc and the process step can be considered “safe”, independent of the charging. Additionally, it is necessary to determine what happens to the PCB in the follow-on process steps. If the PCB comes to a process step where it discharges slowly and in a controlled way, for example, by the temperature at reflow soldering or by the relative humidity while stored in a magazine, no further risk mitigation measures are necessary. If the charged PCB is going directly to a process where it contacts another conductor (for example, at testing), the charge must be drained off before the first contact happens, by using ionization for example.
- 3) The same uncharged PCB now comes to a process step, where it is charged during the process and contacted immediately afterward. It is possible that a hard discharge can happen immediately after the charging event. In this case, there is a clear risk for a CDM-like ESD event. A typical example of this is the in-circuit test (ICT). The PCB is pressed down by plastic pins, made very often of highly chargeable material. This charging is transferred to the PCB by induction. During the electrical measurement, the PCB is contacted with metallic pogo-pins and a hard discharge from the PCB into the tester can occur.

NOTE Very critical during such “closed” process steps is the fact that the problem can be overlooked very easily since the PCB is not charged before and after the process but can nevertheless be damaged during the process.