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3D Chip Stack with Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions

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Introduction

To increase device bandwidth, reduce power and shrink form factor, microelectronics manufacturers are implementing three dimensional (3D) chip stacking using through silicon vias (TSVs). Chip stacking with TSVs combines silicon and packaging technologies. As a result, these new structures have unique reliability requirements. This document is a guideline that describes how to evaluate the reliability of 3D TSV silicon assemblies.

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3D CHIP STACK WITH THROUGH-SILICON VIAS (TSVS): IDENTIFYING, EVALUATING AND UNDERSTANDING RELIABILITY INTERACTIONS

(From JEDEC Board Ballot JCB-09-64, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication references a set of frequently recommended and accepted JEDEC reliability stress tests. These tests provide guidance for qualifying new and modified technology/process/product families, as well as individual solid state surface-mount products. This publication is intended as a guideline to describe the extension of the standard tests to three-dimensional (3D) chip structures that contain stacks of two or more chips that use through-silicon vias to connect from the front side to the back side of each chip. The main element of this extension is the addition of appropriate test structures to evaluate the reliability of the TSVs and other new features introduced in the fabrication of 3D products. This publication applies to vias-first process (TSV formation before completion of the silicon device fabrication), vias-middle (TSV formed in the BEOL or prior to the BEOL process), and a vias-last process (TSV formation after completion of the silicon device fabrication). Although 3D TSV test structures may not be a prerequisite for silicon chip qualification, they are necessary if those chips are intended for use in 3D products. If the effects of 3D TSVs on a device technology placed in a specific packaging scheme are not known, there could be reliability concerns for that component (packaged part) that are not evident with standard component level test structures. Therefore, it is recommended to include 3D TSV test structures and associated testing and failure analysis to determine if there are any adverse effects on the assembly due to packaging.

This publication covers only interaction between the 3D TSV component, the semiconductor package, and the semiconductor device. Interactions between the assembled component and a second level assembly are not covered. See JEP150 for information regarding assembled component reliability.

The reliability stress tests referred to in this document have been found capable of stimulating and precipitating failures in components in an accelerated manner, but they should not be used indiscriminately. Failures from each test should be examined for:

- a) potentially new and unique failure mechanisms
- b) situations where these tests/conditions may induce invalid or overstress failures.

In either case, the set of reliability requirements, tests, and/or conditions should be appropriately modified to properly include the new failure mechanisms and modes.

This document does not relieve the supplier of the responsibility to meet internal or customer-specified qualification programs.

2 Terms and Definitions

3D chip stack: Two or more chips vertically connected to form a unified electrical structure in a single package.

assembled state (of a component): The state of a component that has been attached to a second-level assembly.

back-end-of-line (BEOL) (adj): Pertaining to the portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

back end of line (BEOL) (noun): The portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

bond and assembly process (B&A): A process associated with connecting chips (dice) to other package elements and assembling semiconductor-device packages.

chip stack: A group of interconnected silicon chips stacked vertically to make a 3D structure.

chip-to-chip interconnect; level D interconnect: The structure that connects one chip in a 3D stack to another chip in that 3D stack.

NOTE Examples of this structure include, but are not limited to, solder bumps and copper pads.

chip-to-package interaction (CPI): For the purpose of this document, the interaction between stresses induced by the semiconductor package and the semiconductor chip whether alone or within the semiconductor 3D chip stack.

chip-to-substrate-interconnect; level 1 (L1) interconnect: The structure that connects a chip to a substrate.

NOTE 1 For the purpose of this document a “chip-to-substrate-interconnect” is referred to as an “interconnect”.

NOTE 2 Examples of this structure include, but are not limited to, solder bumps and copper columns.

NOTE 3 Level 1 (L1) interconnect is not associated with JP 001 Foundry Level 1 Qualification (L1).

dice: Plural of die.

distance to neutral point (DNP): The physical distance from the stress-neutral point to the point of interest on the die, chip stack, or interposer.