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## **Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity**

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# PROCEDURE FOR THE EVALUATION OF LOW-K/METAL INTER/INTRA-LEVEL DIELECTRIC INTEGRITY

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## Foreword

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This document is intended for use in the semiconductor IC manufacturing industry and provides reliability characterization techniques for low- $k$  inter/intra level dielectrics (ILD) for the evaluation and control of ILD processes. It describes procedures developed for estimating the general integrity of back-end-of-line (BEOL) ILD. Two basic test procedures are described, the Voltage-Ramp Dielectric Breakdown (VRDB) test, and the Constant Voltage Time-Dependent Dielectric Breakdown stress (CVS). Each test is designed for different reliability and process evaluation purposes. This document also describes robust techniques to detect breakdown and TDDB data analysis.

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## Introduction

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Two test procedures are described within this document: a fast VRDB test, and a constant voltage TDDB test (CVS). Each of these procedures is designed for different evaluation purposes and can be implemented separately or complementally.

The VRDB test starts at zero voltage or  $V_{use}$  and ramps linearly until dielectric breakdown occurs and can be conducted at either room temperature or at higher temperatures to accelerate the occurrence of the degradation mechanism to failure. VRDB tests are important to characterize the defects at lower electric fields and the dielectric breakdown strength of dielectric for a given process. The CVS test starts at a fixed voltage and is kept at this fixed voltage until dielectric breakdown occurs. The test can also be performed at higher temperatures to accelerate failure. TDDB tests are important to characterize the long-term dielectric acceleration parameters and to calculate the ILD based fraction of the failure rate or lifetime of a product.

## PROCEDURE FOR THE EVALUATION OF LOW-K/METAL INTER/INTRA-LEVEL DIELECTRIC INTEGRITY

(From JEDEC Board Ballot JCB-15-23, formulated under the cognizance of JC-14.2 Subcommittee on Wafer Level Reliability.)

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### 1 Scope

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The continued scaling of advanced VLSI circuits, particularly of high performance logic circuits, is driving the need for low- $k$  materials and copper metallization in back end of the line (BEOL) interconnect systems to reduce the resistance-capacitance (RC) delay, cross talk noise, and power dissipation. With the wide applications of low- $k$  and ultra-low- $k$  dielectric materials at the 90nm technology node and beyond, the long-term reliability of such materials is rapidly becoming one of the most critical challenges for technology qualification. Low- $k$  time dependent dielectric breakdown (TDDB) is commonly considered as an important reliability issue because low- $k$  materials generally have weaker intrinsic breakdown strength than traditional SiO<sub>2</sub> dielectrics. This problem is further exacerbated by the aggressive shrinking of the interconnect pitch size due to continuous technology scaling.

The procedures outlined herein were developed to estimate the electrical breakdown performance of low- $k$  ILD and as a tool for driving constant improvement in the low- $k$  ILD process. The test procedure described within this document should be used as common methodology for low- $k$  ILD process control and improvement and could be used as a guideline to predict the effect of ILD TDDB on product lifetime or failure rate. In actual practice the ILD TDDB reliability of a semiconductor product is a complicated function of the interconnect critical area, power duty cycles, transient voltage variation, and series resistance. These parameters are not considered within this document.

The purpose of this document is to describe test procedures for characterizing the reliability of inter/intra level dielectrics. It does not specify acceptance or rejection criteria for any of the described procedures.

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## 2 Terms and definitions

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The following abbreviations and symbols are used in this document. They have been listed alphabetically for the convenience of the reader.

### 2.1 Abbreviations

**BEOL:** Back end of line

**CVS:** Constant voltage stress

**DUT:** Device under test

**ILD:** Intralevel and/or interlevel dielectric

**MLE:** Maximum likelihood estimation

**Tddb:** Time dependent dielectric breakdown

**VRDB:** Voltage ramp dielectric breakdown

### 2.2 Symbols

**$A_{ILD}$  ( $cm^2$ ):** Total active area of dielectric.

**$E_{ILD}$  (V/cm):** The ILD electric field. The general formula for E is:

$$E_{ILD} = V_{ILD} / S_{ILD}, \quad (1)$$

where  $V_{ILD}$  is the ILD voltage and  $S_{ILD}$  is the physical ILD spacing between two metal lines.  $S_{ILD}$  must be determined by a consistent, documented method. The method of determining  $S_{ILD}$  or a reference to the documented standard must be included in the data report.

**$E_{bd}$  (V/cm):** The estimated ILD electric field just before ILD breakdown.

**$I_{bd}$  (A):** ILD current measured just before ILD breakdown.

**$I_{comp}$  (A):** The maximum current of the voltage forcing equipment. Often the user can specify a compliance limit for a particular test.

**$I_{init}$  (A):** ILD failure current when  $V_{use}$  is applied. This value is determined as a deviation from typical current vs. voltage characteristics measured from good devices. For maximum sensitivity the value should be well above the worst case ILD leakage current of a “good” ILD and at least 10 times greater than the noise floor of the test systems. A recommended value is 50 times the measured value for a good structure. Or a pre-defined absolute leakage level such as 100nA, which could critically affect chip performance and cause chip operation failure, could be used as failure criterion.

**$I_{meas}$  (A):** The measured ILD current.

## 2.2 Symbols (cont'd)

**$I_{\text{use}}$  (A):** The typical measured current through the ILD at the normal use voltage.

**$I_{\text{stress}}$  (A):** The ILD current measured during the CVS test.

**$I_{\text{previous}}$  (A):** The previously measured ILD current.

**$I_{\text{stress-t0}}$  (A):** The initial dielectric current measured at  $V_{\text{stress}}$  during the CVS test.

**$t_{\text{bd}}$  (s):** The recorded time at ILD failure.

**$t_{\text{int}}$  (s):** The time interval to sense ILD current during the CVS test. This value should be <1% of the anticipated  $t_{\text{bd}}$  and should be decided for each stress condition

**$t_{\text{meas}}$  (s):** The time interval for measuring the stress current ( $I_{\text{stress}}$ ) during the constant voltage test.

**$t_{\text{record}}$  (s):** The time interval for recording current measurements ( $I_{\text{meas}}$ ) during the constant voltage test.

**$t_{\text{step}}$  (s):** The voltage ramp step time is determined from the ramp-rate and  $V_{\text{step}}$ . The step time should be less than or equal to 100 ms.

**$S_{\text{ILD}}$  (nm):** Physical space of remaining ILD between metal interconnects.

**$V_{\text{bd63}}$  (V):** The scale parameter of the  $V_{\text{bd}}$  Weibull distribution

**$V_{\text{post}}$  (V):** The voltage measured when  $I_{\text{init}}$  is forced into an ILD that been detected as broken down but does not exhibit excessive leakage current during the post-VRDB or CVS test. This situation results when the interconnect metal electrode is evaporated off during the high temperature transient during breakdown.

**$V_{\text{stress}}$  (V):** The ILD stress voltage.

**$V_{\text{use}}$  (V):** The test voltage that is applied during pre- and post-test to determine device validity. This voltage is usually the power supply voltage or use voltage of the technology.