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LONG-TERM STORAGE GUIDELINES FOR ELECTRONIC SOLID-STATE WAFERS, DICE, AND DEVICES

Introduction

Age does not adversely affect solid-state electrical performance provided no degradation in materials occurs. This publication provides the industry with the best practices and recommendations for packing and storing solid-state electronics for long-term storage (LTS).

For the purposes of this document, LTS is defined as continuous storage where J-STD-033 does not apply.

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LONG-TERM STORAGE GUIDELINES FOR ELECTRONIC SOLID-STATE WAFERS, DICE, AND DEVICES

(From JEDEC Board Ballot JCB-22-36, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication examines the LTS requirements of wafers, dice, and packaged solid-state devices. (Note: Packaging may include encapsulation, under-fill, over-mold, or other techniques to attach a die to the next level of assembly.) The user should evaluate and choose the best practices to ensure their product will maintain as-received device integrity and minimize age- and storage-related degradation effects. Major degradation concerns can be driven by moisture-induced corrosion, contamination, electrostatic fields, temperature effects, and outgassing. Please refer to J-STD-033 for non-LTS criteria as well as requirements for moisture sensitivity levels, environmental conditions, dry bag requirements, handling, shipping, and desiccant calculations.

Wafers and dice that are in process or finished may require LTS depending upon program needs. Environmental factors should be evaluated to avoid electrostatic discharge (ESD) damage and to protect the wafer and die bond pads and the device terminal leads against corrosion and damage until any die is packaged or otherwise attached in its next level of assembly. Specific ESD requirements and procedures can be found in ANSI/ESD S20.20, EOS/ESD S8.1, and JESD625 as applicable.

Solid-state devices may be constructed from either organic or ceramic materials. Many organic packaged solid-state devices are designed to attach the semiconductor die to copper die bond pads or heat spreaders or stiffeners. These packages utilize organic resins and other carbon-based materials which can absorb and retain moisture, leading to failure mechanisms such as delamination, corrosion, and warpage. Ceramic solid-state devices are constructed from inorganic materials such as alumina or glass frit. Ceramic devices can develop corrosion from moisture exposure. Ceramic devices can be damaged from handling.

Effective use of this publication is intended to prevent environmental damage to and maintain reliability of wafers, dice and unassembled solid-state devices during LTS. Product destined for LTS should be free from any initial storage concerns, including contamination from process chemicals, fluxes, handling damage, etc. LTS product should be inspected prior to use to ensure no detrimental effects. Metallic whiskers (such as tin, silver, copper) could develop depending upon moisture and temperature environmental conditions. This document does not relieve the supplier of the responsibility to meet internal or customer specified requirements or qualification programs.

2 Terms and Definitions

critical moisture limit: The maximum safe equilibrium moisture content for a specific encapsulated device at reflow assembly or rework.

interlevel dielectric (ILD): The dielectric material used to electrically separate closely spaced interconnect lines arranged in several levels (multilevel metallization) in an advanced integrated circuit

long-term storage (LTS) : Uninterrupted storage where the conditions and requirements of J-STD-033 do not otherwise apply; e.g., safe storage, shelf life, floor life.

NOTE Allowable storage durations will vary by form factor (e.g., packing materials, shape) and storage conditions. In general, long-term storage is greater than one year.

LTS packaged hardware: The wafers, dice, or encapsulated devices that have additional packaging for storage to protect from moisture and mechanical impact and for ease of identification and handling.

LTS storeroom: An area containing wafers, dice, or packaged devices that have additional packaging for storage to protect from moisture or from mechanical impact or for ease of identification or handling.

moisture-sensitive device (MSD): Any device that exhibits moisture absorption or moisture retention and whose quality or reliability is affected by moisture.

next-level assembly: The attachment of a die or packaged device to the next level of assembly packaging.

printed circuit board (PCB): A substrate used to mechanically support and electrically connect electronic components using conductive pathways or signal traces by printing or etching tracks of a conductor such as copper on one or both sides of an insulating substrate.

NOTE A PCB is also called a printed wiring board (PWB) or etched wiring board.

under-bump metallization (UBM): A patterned, thin-film stack of material that provides 1) an electrical connection from the silicon die to a solder bump; 2) a barrier function to limit unwanted diffusion from the bump to the silicon die; and 3) a mechanical interconnection of the solder bump to the die through adhesion to the die passivation and attachment to a solder bump pad.

under-bump metallurgy (UBM): The metal layers located between the solder bump and the die.

3 References and Other Useful Resources

3.1 IPC¹ / JEDEC²

IPC-T-50, *Terms and Definitions for Interconnecting and Packaging Electronic Circuits.*

JESD88, *Dictionary of Terms for Solid State Technology.*

IPC/JEDEC J-STD-033, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.*

JESD201, *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes.*

JESD625, *Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices.*

IPC/JEDEC J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

IPC-1601, *Printed Board Handling and Storage Guidelines.*

JESD22-B118, *Semiconductor Wafer and Die Backside External Visual Inspection.*

JESD22-B116, *Wire Bond Shear Test Method.*

J-STD-002, *Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.*

JEP122, *Failure Mechanisms and Models for Semiconductor Devices.*

3.2 ANSI³

ANSI/ESD S20.20, *Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices).*

ANSI/ESD STM11.11 *Surface Resistance Measurement of Static Dissipative Planar Materials.*

ANSI/ESD STM11.12 *Volume Resistance Measurement of Static Dissipative Planar Materials.*

ANSI/ESD STM11.13 *Two-Point Resistance Measurement of Static Dissipative Materials*

3.3 Electrostatic Discharge Association (ESD)⁴

EOS/ESD S8.1, *Protection of Electrostatic Discharge Susceptible Items - Symbols - ESD Awareness.*

3.4 Military Standards⁵

MIL-PRF-81705, *Performance Specification Barrier Materials, Flexible, Electrostatic Protective.*

MIL-PRF-131H, *Barrier Materials.*

3.5 ISO⁶

ISO 14644, *Cleanrooms and Associated Controlled Environments.*