JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163A

(Revision of JEP163 dated September 2015)

DECEMBER 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2022
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

This page intentionally left blank

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

SELECTION OF BURN-IN/LIFE TEST CONDITIONS AND CRITICAL PARAMETERS FOR QML MICROCIRCUITS

Contents

		Page
1	**Scope**	**1**
2	**References**	**1**
3	**Terms and Definitions**	**1**
4	**Wafer Fabrication and Design Considerations**	**4**
5	**Burn-In Stress and Electrical Test Conditions Development**	**4**
5.1	Considerations for Burn-In Stress Conditions	**4**
5.2	Electrical Test and Data Analysis for Burn-In	**7**
6	**Life Test Stress and Electrical Test Conditions Development**	**8**
6.1	Considerations for Life Test Stress Conditions	**8**
6.2	Electrical Test and Data Analysis for Life Test	**10**
Annex A	**(Informative) Example Burn-In Condition Evaluations**	**12**
Annex B	**(Informative) Burn-In and Electrical Measurement Requirements**	**17**
Annex C	**(Informative) Burn-In Alternatives**	**20**

Figures	**Page**
Figure 1 — Burn-In Schematic	**13**
Figure 2 — SRAM Burn-In Example	**15**

Tables	**Page**
Table 1 — Burn-In Mechanisms	**6**
Table 2 — Life Test Wearout Mechanisms	**9**
Table 3 — Dynamic Burn-In Pin Listing	**14**
Table 4 — Static Burn-In Pin Listing	**14**
Table 5 — Burn-In and Electrical Measurement Requirements	**17**

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

Foreword

This publication was developed as a guideline to assist manufacturers of integrated circuits (microcircuits) in defining the conditions for burn-in and life test of their products to meet the quality and reliability performance requirements of MIL-PRF-38535 and the applicable Standard Military Drawing. Documentation of the manufacturer's technical rationale in accordance with this guideline will also facilitate customer understanding and acceptance of the manufacturer's Quality Management (QM) plan.

Introduction

MIL-PRF-38535, in conjunction with MIL-STD-883, defines the basic screening requirements for compliant microcircuits. MIL-STD-883 Test Method 5004 specifies two independent burn-in conditions for Class Level S devices. A dynamic burn-in is performed for 240 hours at 125°C. A static or reverse bias burn-in is performed for 72 hours at 150°C. Per Test Method 5004 the reverse bias burn-in is a requirement only when specified in the applicable device specification (i.e. Standard Military Drawing) and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern.

These requirements have been part of the military standards for decades and originated at a time when design rules and wafer fabrication processes were much less advanced than current state-of-the art technologies. With the advent of improved wafer fabrication processes, Statistical Process Controls (SPC), Wafer Level Reliability (WLR), Circuit Design Tools, Design-For-Test (DFT) techniques, and modern simulation and characterization techniques, the presence of certain failure modes have been reduced and/or eliminated for certain wafer fabrication processes. However, deep submicron and System On A Chip wafer fabrication processes have potentially greater transistor to transistor process variations; hence, they may have a greater need for burn-in and life test to evaluate and screen infant life mortality. Due to the current variation in geometry sizes and different levels of technology maturity and circuit designs, the establishment of the appropriate burn-in/life test stress and test conditions must be evaluated in relation to each product's wafer fabrication process and circuit design techniques. The stress conditions must demonstrate adequate Early Failure detection and Intrinsic Failure Rate (IFR) performance that meets customer failure rate requirements. For example, a typical space application has a goal of 10 to 15 years operating life.

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

SELECTION OF BURN-IN/LIFE TEST CONDITIONS AND CRITICAL PARAMETERS FOR QML MICROCIRCUITS

(From JEDEC Board Ballot JCB-22-50, formulated under the cognizance of JC-13 Committee: Government Liaison.)

1 Scope

This publication is intended as a guideline to develop and establish conditions for burn-in and life test of MIL-PRF-38535 QML integrated circuits. These guidelines are intended to provide manufacturers with a consistent means of defining burn-in and life test stress and electrical test requirements acceptable to user organizations and for the development of Standard Military Drawings.

The guidelines cover the entire design, wafer fabrication and manufacturing flows, including design and process awareness. Without design awareness (critical circuit blocks/functionality, etc.), burn-in/life test of an integrated circuit might be compromised, or it might dramatically shorten the device's life prior to system use.

2 References

EEE-INST-002, *Instructions for EEE Parts Selection, Screening, Qualification, and Derating (NASA Goddard Space Flight Center)*

JEP122, *Failure Mechanisms and Models for Semiconductor Devices*

JESD85, *Methods for Calculating Failure Rates in Units of FITs*

MIL-HDBK-1331, *Handbook for Parameters to be Controlled for the Specification of Microcircuits (DLA Land and Maritime)*

MIL-PRF-38535, *General Specification for Integrated Circuits (Microcircuits) Manufacturing (DLA Land and Maritime)*

MIL-STD-883, *Test Method Standard Microcircuits (DLA Land and Maritime)*

3 Terms and Definitions

For the purposes of this publication, the terms and definitions given in the above references and the following apply:

absolute maximum rated junction temperature: The maximum junction temperature of an operating device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

Documents
Document Sharing Hub

Full document details: JEDEC JEP163A 2022

3 Terms and Definitions (cont'd)

absolute maximum rated voltage: The maximum voltage that may be applied to a device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

acceleration factor (A, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of 1/kT, the reciprocal of the product of Boltzmann's constant in electron-volts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electron-volts.

NOTE 4 The abbreviation AF is often used in place of the symbol A.

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature.

NOTE 1 This is the acceleration factor most often referenced. The Arrhenius equation for reliability is commonly used to calculate the acceleration factor that applies to the acceleration of time-to-failure distributions for microcircuits and other semiconductor devices:

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp[(-E_{aa}/k)(1/T_1 - 1/T_2)]$$

Where:

E_{aa} is the apparent activation energy (eV);

k is Boltzmann's constant (8.62×10^{-5} eV/K);

T_1 is the absolute temperature of test 1 (K);

T_2 is the absolute temperature of test 2 (K);

λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});

λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1}).

NOTE 2 The best-fit linear slope of a plot of the natural log of the time-to-failure as a function of 1/kT, the reciprocal of the product of Boltzmann's constant in electron-volts per kelvin and the absolute temperature in kelvins, is equal to the apparent activation energy in electron-volts.

NOTE 3 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s.

Documents
Document Sharing Hub
Full document details: JEDEC JEP163A 2022

3 Terms and Definitions (cont'd)

activation energy (E_a): The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur.

NOTE The activation energy is used in the Arrhenius equation for the thermal acceleration of physical reactions. The term "activation energy" is not applicable when describing thermal acceleration of time-to-failure distributions, e.g., in the Arrhenius equation for reliability; hence the need for the term "apparent activation energy."

apparent activation energy (E_{aa}): An energy value, analogous to activation energy, that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions.

NOTE 1 An apparent activation energy should be associated with a specific failure mechanism and an observed time-to-failure distribution to calculate the acceleration factor for converting the observed failure rate to the quoted failure rate at a different temperature.

NOTE 2 An activation energy is a measure of the heat energy needed to establish the rate of reaction for a specific failure mechanism. The reaction rate and other contributing factors, e.g., radiation, voltage, humidity, magnetic fields, determine the unique time-to-failure distribution for the modeled failure mechanism.

NOTE 3 The apparent activation energy is empirically determined from the change in an observed time- to-failure distribution with temperature.

failures in time (FITs): The number of failures per 10^9 device hours.

high-temperature forward-bias (HTFB) test: A static test configured to forward-bias at least a majority of the solid-state junctions of the devices operating at, or near, absolute maximum rated junction temperature and voltages.

high-temperature reverse-bias (HTRB) test: A static test configured to reverse-bias at least a majority of the solid-state junctions of the devices operating at, or near, absolute maximum rated junction temperature and voltages.

NOTE For some CMOS circuits, any static state will reverse-bias approximately half the junctions (others are zero-biased).

recommended operating conditions: The operating conditions, such as supply voltage and junction temperature, at which a device is specified to operate in compliance with the applicable device specification or data sheet.

NOTE 1 Maximum and minimum values are applicable; these adjectives refer to the magnitudes.

NOTE 2 The maximum recommended operating supply voltage is not the absolute maximum rated voltage, i.e., the voltage beyond which, damage is likely.

toggle coverage: The percentage of signals in a device that are toggled (transitioned Low to High and from High to Low) during one complete cycle (an entire sequence of applied signals).

Documents
Document Sharing Hub
Full document details: JEDEC JEP163A 2022