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System Level ESD Part III: Review of ESD Testing and Impact on System-Efficient ESD Design (SEED)

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SYSTEM LEVEL ESD

Part III: Review of ESD Testing and Impact on System-Efficient ESD Design (SEED)

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Foreword

This document is the third of the Industry Council white papers dealing with System Level Electrostatic Discharge (ESD). The previous two white papers addressing system level ESD are the Industry Council's JEP161 and JEP162.

In JEP161, the misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified, and a novel ESD component / system co-design approach called system efficient ESD design (SEED) was described. The SEED approach is a comprehensive ESD design strategy for system interfaces to prevent hard (permanent) failures. In JEP162 this comprehensive analysis of system ESD understanding to categorize all known system ESD failure types was expanded, and described new detection techniques, models, and improvements in design for system robustness. JEP162 also expands this SEED co-design approach to include additional hard / soft failure cases internal to the system.

This third document on system level ESD takes this further while focusing on system testing of ports and the shortcomings of air discharge testing.

Part A of the document highlights the need of a consistent and standardized specification of IO Port contact discharge which is widely used in industry. This is supported by real world discharge scenarios like cable discharge. A well specified testing procedure and the related target levels for IO port direct pin injection are the base for a SEED simulation and co-design approach which can commonly be executed by IC suppliers and system customers.

Part B addresses air discharge testing, which is most relevant for field fails, while its specification in IEC 61000-4-2 and its practical application suffers from both missing repeatability and reproducibility. In the first part, the arguments of maintaining air discharge as a relevant, mandatory test method are explained. Various scenarios leading to real world discharge events which correlate to IEC 61000-4-2 testing are analyzed in more detail. They can lead to soft and hard fails reproducible by system ESD testing. Secondly, in this document new considerations to better calibrate the air discharge test and reliably perform a repeatable air discharge test are given

Introduction

The Industry Council previously published two white paper documents describing the nature of component level electrostatic discharge (ESD) versus system level ESD, and the methods to ensure efficient system level ESD robustness. JEP 161 established that there is no correlation between component and system level robustness and introduced the concept of *system-efficient ESD design*, known as SEED, while JEP 162 expands on the concept of SEED, which utilizes simulations to achieve desired system ESD robustness with minimal impact on system performance.

We present here JEP164 that addresses real-world system level ESD testing and suggests improvements to the existing International Electrotechnical Commission (IEC) 61000-4-2 standard widely used to test for ESD reliability of electronic systems. Before presenting a summary of this new white paper, highlights of the two previous white papers are reviewed to place the challenges of system level ESD in a full perspective.

I.1 Review of JEP161 document highlights

- The misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified.
- A novel ESD component / system co-design approach called system efficient ESD design (SEED) was described.

I.2 Review of JEP162 document highlights

- Comprehensive analysis of system ESD understanding to categorize all known system ESD failure types and describe new detection techniques, models, and improvements in design for system robustness.
- Discussed system ESD stress application methods and introduces new system diagnosis methods to detect weak ESD failure areas leading to hard or soft failures.
- Outlined present-day state-of-the-art electromagnetic compatibility (EMC)/electromagnetic interference (EMI) design prevention methods that have been developed to prevent system level ESD failure.

I.3 Introductory Note for JEP164

While the two previous documents have set the stage for approaching system level ESD in a more realistic manner, the nature of testing for the well-established IEC 61000-4-2 test method has not adequately addressed all the challenges of testing from an increasing variety of modern electronic systems. This third document on system level ESD is intended to be a comprehensive review of more effective test procedures and recommends them for consideration as part of an overall improved IEC 61000-4-2 test method.

I.4 Overview of the Document

As an important note, compilation of this document involved contributions from university and industry experts and includes a survey of the most salient findings from published academic research papers. The main goal is to derive the most important information and to leverage this to formulate recommendations to an overall improved system level ESD test method.

I.5 What is the real motivation here?

All electronic systems, from mobile phones to large computers, need to be tested for robustness from damage or upset from electrostatic discharge. System ESD testing is done using an ESD pulse generator, often called an ESD gun. The vast majority of system level ESD testing follows the test procedures and ESD pulse generator specifications defined in IEC 61000-4-2. Unfortunately, even when carefully following the procedures in IEC 61000-4-2, there is a high level of uncertainty in the test results, and successfully passing the test requirements is often not a complete prediction of ESD robustness in the field.

The uncertainty in system level ESD test results is often attributed to the large differences in the calibration current waveforms which can exist between ESD guns from different manufacturers, even when all the ESD guns meet the specifications in IEC 61000-4-2. But this is only a part of the problem.

The reason the Industry Council has addressed this topic is regarding the need for a more relevant and reproducible system ESD test procedure to better correlate integrated circuit (IC) and board co-design approaches as discussed in WP3 Part 1 and Part 2. The Industry Council provides recommendations based on technical data in this document which can be used for further discussion in standardization committees which are chartered with system level ESD test methods.

I.5 What is the real motivation here? (cont'd)

This White Paper explores the reasons for the high level of uncertainty in the test results, proposing test procedure modifications to improve repeatability, reproducibility, and predictability in field performance. Modeling methods are also discussed which can give insight into system level ESD testing and the design of ESD robust systems.

I.6 Organization of the Document

The document is divided into two main parts: Part A describes direct pin discharge, and Part B considers discharge to chassis and display, also known as air discharge. Specifically, Part A presents real world scenarios such as cable discharge events (CDE) to introduce an extension to the IEC 61000-4-2 standard on direct port discharging. To further facilitate this, reference circuit models are described so that SEED, as introduced in JEP161, can be used more effectively. Whereas Part B describes the shortcomings of the currently practiced air discharge method and recommends improvements for calibration and test measurements.

Synopsis of Part A: For shielded connectors, the IEC 61000-4-2 standard does not specify direct pin stress, but this is important for system qualification involving uncertain results, variations in individual set ups, and repeatability of the results. This section promotes an industry wide alignment for the IEC 61000-4-2 standard to include direct pin discharge. For printed circuit board (PCB) designs to address this issue, standard models for SEED are described.

In Part A of this document, the approach is first to describe the real-world events ([Clause 4](#)) that must be understood, then detailing the direct-injection method ([Clause 5](#)) and concluding with information on the important target levels for these tests ([Clause 6](#)). For these issues on direct pin testing to be viewed in an analytical perspective, the ESD gun model details ([Clause 7](#)) and the techniques of SEED simulations ([Clause 8](#)) are also presented. An alternate characterization method using 50-ns TLP is also introduced that can be directly applied to the IC as a way of characterizing the external pin high current I-V response. One very important outcome of the investigations is that for universal serial bus (USB) cables meeting standard shielding requirements a 2 kV stress is enough.

Synopsis of Part B: After studying the air discharge test method, it is concluded that both a lack of precise test methods and specifications led to extreme variability and uncertainty in qualification results. Removing this method altogether is not an option since in the real-world events discharges to chassis do occur. Details of this inadequacy and the subsequent improved recommendations are given.

In Part B, the document focuses on improved test methods for displays using the air discharge method. This includes a review of the challenges associated with the IEC 61000-4-2 test methods and the test results' uncertainties ([Clause 9](#)). Improvements to the calibration of the ESD simulators for both contact-mode discharge and air discharge are suggested ([Clause 10](#)). With the extensive background of the test methods and the description of corresponding various opportunities for improved applications of these methods, the document recommends useful test improvements ([Clause 11](#)). Supporting technical details of the work presented in this document are given in the appendices at the end.

I.7 Nuances of System Level ESD Testing

The most important points of this document can be understood only after the real issues of system level ESD robustness are clearly stated and defined. This will also give a better understanding of why the test method improvements recommended here are important to the industry.

System level ESD testing is performed using a combination of stresses to each system while in a powered, functional state. Contact discharge is applied to conductive surfaces by placing a pointed tip of the ESD gun against the system and initiating an ESD pulse. Air discharge is performed on insulative surfaces, with emphasis on locations frequently touched by the user, such as keyboards and touch screen displays, and locations where ESD can enter the system, such as seams, vent holes, etc. In this test a rounded tip on the ESD gun is charged to a high voltage and the gun is moved toward the system under test until an air discharge occurs or the surface of the system is touched. In the next test discharges are made to horizontal and vertical coupling planes near the device under test to see if the fields generated by these stresses can upset the system. It is important to note that test results from system level ESD testing can have a variety of results:

- System suffers no ill effects from the testing
- Soft failure
 - System is upset but returns to normal operation without user intervention
 - System is upset but returns to normal operation after user intervention which may require a reboot of the system
- Hard failure in which there is permanent physical damage requiring repair.

The causes of testing uncertainty and failure to predict field reliability covered in this white paper are numerous and will be summarized here in bullet form.

- Important for both contact and air discharge
 - IEC 61000-4-2 compliant ESD guns have substantial variability in current waveforms and power distribution in the RF spectrum between models and manufacturers.
 - Number of stresses per discharge point (10) is insufficient to adequately predict soft failures, which can depend on precise timing between the stress and system timing.
 - Test results can depend on a previous stress if charge is not removed before the next stress - this phenomenon can lead to **secondary discharge**.
 - Transient electromagnetic fields from ESD guns are not specified or limited. This leads to an uncertainty of soft failure testing with different guns. Pulse to pulse variation of the same gun can be eliminated by multi-zap testing.
- Contact discharge
 - Contact discharge is generally more repeatable than air discharge but does not represent the real world which is typically air discharge
 - Discharge current waveform is only verified for a low resistance load:
- Air discharge
 - There is no calibration procedure for ESD guns in air discharge
 - Test severity depends on arc length which is sensitive to a number of factors
 - Humidity
 - Approach speed
 - Geometry
 - Materials on each side of arc

I.7 Nuances of System Level ESD Testing (cont'd)

- Discharge to coupling planes
 - Geometries specified in IEC 61000-4-2 are sometimes unrealistic for modern form factors
- Expanding the scope of IEC 61000-4-2
 - Cable discharge event (CDE) is not included
 - There are a number of forms of cable discharge event (CDE)
 - Cable quality can affect CDE
 - Tests conditions are not realistic for wearable devices, which could not have been realistically anticipated in the earlier IEC 61000-4-2 specification creation. These include items such as smart watches or mobile phones held in a case attached to a belt.

I.8 Important Recommendations from This Work

Some important recommendations are summarized here for both contact discharge and air discharge tests.

- Direct discharge:
 - Establish industry wide alignment for direct discharge to ports
 - Consider alternate 50-ns TLP test with 2 ampere goal applied to IC pins
 - Consider 2 kV contact discharge as a standard spec for USB pins meeting cable shielding requirements
- Air discharge; Consider recommendations to improve the testing at a chosen discharge point that include:
 - Maintain air discharge as a field relevant stress method, but improve its reproducibility by:
 - Improved gun calibration for air discharges
 - Controlled arc length using
 - A well-controlled humidity environment
 - Introduction of ionization
 - Controlled approach conditions by use of robotics
 - Increased number of discharges per test point
 - Controlling secondary discharge
 - Measurement of radiated gun emission
 - Address cable discharge as a relevant system level ESD event

I.9 Test Reproducibility Recommendations

The white paper presents data to support an understanding of state-of-the-art system ESD testing and makes suggestions for improving the repeatability and reproducibility of system level ESD testing. The following bullet list summarizes the improved understanding and suggestions for improving future testing.

- ESD gun calibration
 - Contact discharge waveform verification with loads other than a low impedance resistive load
 - Introduction to a method for ESD gun calibration in air discharge mode without the uncertainties of air discharge
 - Measurement of radiated emissions, including the RF spower spectrum
- Methods to improve air discharge arc repeatability
 - Ionization to stabilize arc length
 - Different air discharge tip materials

I.9 Test Reproducibility Recommendations (cont'd)

- Improvements in temperature and humidity control
- Charge removal techniques
- Robotic testing to improve control of approach speeds
- Improvements in test procedures
 - Recommendations on increasing the number of stresses at each test location to improve capture of weaknesses due to soft failures
 - Improved understanding of ESD discharge voltage as a function of humidity
 - Robotics to improve test repeatability
 - Improvements in documentation of test procedures used, including video recording

Finally, the white paper also presents modeling methods which can both improve the understanding of system level ESD testing and help in the design of ESD robust systems.

- Simulation program with integrated circuit emphasis (SPICE) level models of ESD guns
- System Efficient ESD Design (SEED) for simulating systems when ESD stressed
- 3D models of ESD guns and systems

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SYSTEM LEVEL ESD**Part III: Review of ESD Testing and Impact on System-Efficient ESD Design (SEED)**

(From JEDEC BoD Ballot JCB-22-31, formulated under the cognizance of the JC-14.3 Subcommittee on Wafer-Level Reliability.)

1 Scope

This white paper presents the recent knowledge of system ESD field events and air discharge testing methods. Testing experience with the IEC 61000-4-2 (2008) and the ISO 10605 ESD standards has shown a range of differing interpretations of the test method and its scope. This often results in misapplication of the test method and a high test result uncertainty. This white paper aims to explain the problems observed and to suggest improvements to the ESD test standard and to enable a correlation with a SEED IC/PCB co-design methodology. This white paper is divided into a part on direct pin stressing (Part A) and IEC 61000-4-2 testing of chassis and display which is typically a type of air discharge (Part B). Part A discusses the necessary industry alignments and standardization to support a unified SEED design procedure. Part B provides the input to improve the calibration and test reliability of IEC 61000-4-2 in the air discharge mode.

2 Normative references

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated herein. For undated references, the latest edition of the normative document referred to applies.

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3 Terms and definitions

AC	alternating current
ADS	Advanced Design System
ASIC	application specific integrated circuit
CAN	controller area network
CAT	category
CDE	cable discharge event
CDM	charged device model
CST	Computer Simulation Technology
DAC	direct attach copper
DC	direct current
DNA	deoxyribonucleic acid
DUP	device under protection
DUT	device under test
DVI	digital visual interface
EOS	electrical overstress
ESD	electrostatic discharge
EUT	equipment under test
FDTD	finite-difference time-domain
FIT	finite integration technique
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
HBM	human body model
HCP	horizontal coupling plane
HDMI	high definition multimedia interface
H-M	human-metal
IBIS	input/output buffer information specification
IC	integrated circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IO	input/output
ISO	International Organization of Standards
IV	current-voltage
LAN	local area network
LCD	liquid crystal display
PC	personal computer
PCB	printed circuit board
PHY	physical layer interface
PIFA	planar inverted F antenna
PoE	power over Ethernet
RC	resistor capacitor network
RF	radio frequency
RH	relative humidity
RLC	resistor inductor capacitor network
SEED	system efficient ESD design
SFP	small form-factor pluggable
SPICE	simulation program with integrated circuit emphasis
TLM	transmission line matrix
TVS	transient voltage suppression

3 Terms and definitions (cont'd)

USB	universal serial bus
UTP	unshielded twisted pair
UV	ultraviolet
WB	wet bulb
VCP	vertical coupling plane

EMC: electromagnetic compatibility – The condition which prevails when telecommunications (communication-electronic) equipment is collectively performing its individual designed functions in a common electromagnetic environment without causing or suffering unacceptable degradation due to electromagnetic interference to or from other equipment/systems in the same environment (MIL-STD-463A).

SEED: system-efficient ESD design - Co-design methodology of on-board and on-chip ESD protection to achieve system level ESD robustness.

Soft Failure: Failure of a system, not due to physical damage, in which the system can be returned to a functional state without the repair or replacement of a component. Return to a functional state may or may not require operator intervention. Operator intervention may include rebooting or power cycling. Soft Failures can involve software issues and software fixes but in the context of this document they are primarily due to ESD events injecting unwanted signals into the system which place the system into a state in which it does not function as intended.

Part A: Direct Pin Discharge

4 Real World Stress to Port Pins

The IEC 61000-4-2 test uses the discharge of a human via a handheld metal object as its reference ESD event. However, a variety of other ESD events occur which are not within the scope of the test standard. Many attempts have been made to use the IEC 61000-4-2 test generator to perform testing which will ensure robustness against other ESD events.

4.1 Human-Metal Discharge

The IEC 61000-4-2 standard uses the discharge of a human via a small metal part as its reference event [Chu2004]. The waveform shown in the IEC 61000-4-2 standard is similar to the discharge waveform of a human via a small handheld metal part at about 5 kV at an arc length of 0.8 mm. Due to the nonlinear behavior of the arc, human-metal ESD discharges at shorter arc length will have faster rise times and longer arc lengths will have slower rise times. The reference event covers only one situation. Its current derivative is in the range of 4 A/ns, which is at the lower end of the current derivatives observed for human-metal ESD, over a large range of voltages and arc lengths.

4.2 Human Skin ESD

A human skin ESD has much longer rise times (in the range of 1-10 ns for < 8 kV) and lower peak current values compared to a human-metal discharge. However, in the case of multiple discharge pulses, the subsequent pulses will have much faster rise times even if the amplitudes are lower.

4.3 Cables and Cable Discharge Events

In system level testing, discharges to connector pins should be included if the connector geometry allows for such discharges. This requires understanding of the threat levels. Directly applying IEC 61000-4-2 testing at system level voltage settings (e.g., 8 kV) can lead to over testing and unnecessary additional costs. The situations which lead to connector currents need to be identified and the stress levels, as seen by the sensitive data wires, need to be determined and used as guidance for setting test levels.

If a charged cable is inserted into a device under test (DUT), a current will flow onto the connector. Typically, events which cause connector currents are:

- Discharge to a DUT which is connected to ground in a system from a charged source such as a USB cable
- Discharge to another DUT, when both DUTs are connected to each other by a cable.
- Attaching a charged DUT to a grounded cable or a docking station.

The present system level IEC 61000-4-2 standard does not consider a cable discharge event, often referred to in industry as cable discharge event (CDE). However, the IEC 61000-4-2 standard does give some guidance as to which part of a connector should be exposed to a direct ESD discharge.

4.3 Cables and Cable Discharge Events (cont'd)

Protection design and an appropriate testing of system input/outputs (IOs) is certainly a critical topic. Multiple companies have reported field failures on ports such as USB or local area network (LAN). The assumption that a discharge will be safe because the cable is properly shielded, and a ground contact will be made first due to connector design, is often not true. The analysis of cables bought from a wide range of cable suppliers has shown that about 30% of the USB2 cables did not have any shield connection. Missing shield connections have also been found on USB 3.1 cables [Mar2017c, Stad2017].

Due to faster IO speeds, and influenced by reduced human body model (HBM) and charged device model (CDM) robustness levels, more emphasis must be placed on the trade-off between PCB and IC level protection. This is covered by the SEED concept. To enable a SEED based design there must be an understanding of the amplitude and the waveform of the cable discharge. Real world conditions for cable discharges of LAN and USB cables are discussed in the following.

For Ethernet, one needs to distinguish between Ethernet ports that use a transformer, often referred to simply as "magnetics" at the port, and those which have a direct connection to the circuit. The transformer provides a high voltage isolation barrier of at least 1500 V, and for short term, nanosecond long pulses probably > 5000 V. It also provides a common mode return path via the Bob Smith termination circuit, and via ferrites for power over Ethernet (PoE) devices. Further, the transformer will saturate at rather low currents. This saturation will reduce the coupling between the primary and secondary side; thus, it reduces the coupling of the physical layer interface (PHY) IC. This section analyzes LAN interfaces, such as unshielded twisted pair (UTP), which uses a transformer.

In contrast, small form-factor pluggable (SFP) + direct attach copper (DAC) cables directly provide an entry path, without magnetics to the physical layer interface IC. These cables are shielded, have a shielded connector that mates at the shield first. However, direct discharges to the pins are, although not likely, possible. The ESD performance of such cables has not been investigated yet.

4.3 Cables and Cable Discharge Events (cont'd)

Cables have been found which allow discharges to the signal wires of a USB, as they contain ungrounded decorative metal parts above the unshielded signal wires and connector pins. The cable shown in Figure 1 had a decorative metal that is not connected to the shield or the connector. The decorative metal is above the signal wires which connect to a PCB which is within the connector. The signal wires are not shielded underneath the metal part, as the foil and braid are only connected to an unshielded PCB on one side. This allows sparking between the unconnected, decorative metal and the signal wires of the cable and the PCB.

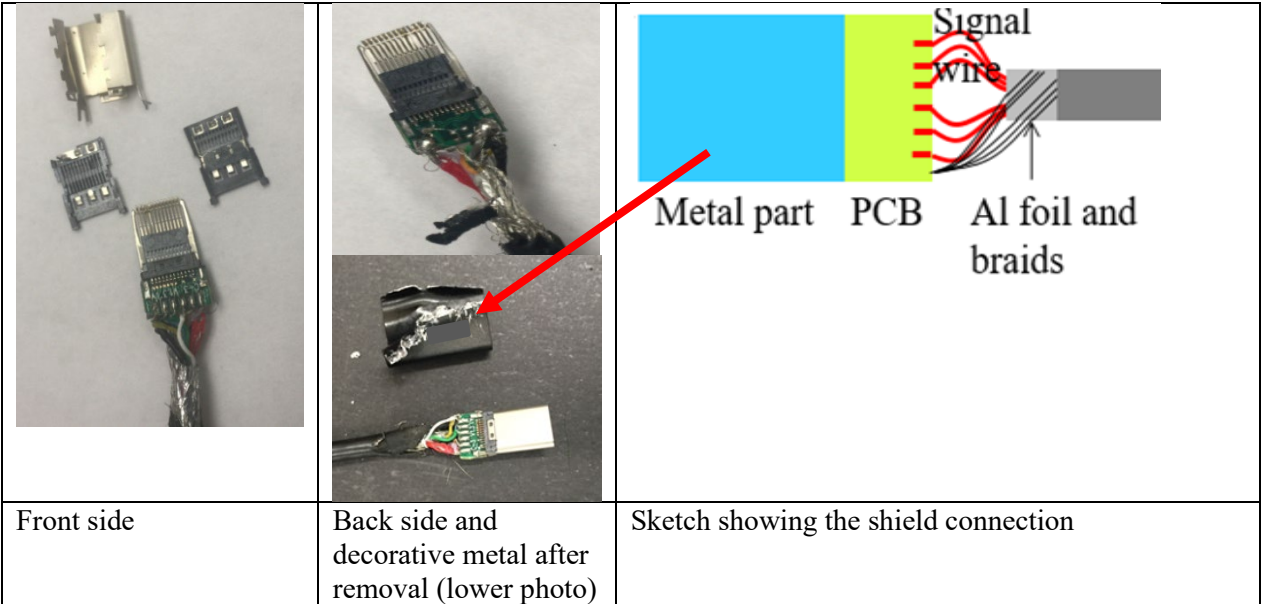


Figure 1 — Shield Structure of a Badly Shielded USB 3.1 Cable

In general, CDE discharges are a rather complex process. The effect of CDE depends on:

- The charge voltage of the cable.
- The charge mode (most cables will charge in common mode: All wires and the shield are at the same potential). A cable may also be polarized by a charge on the jacket. This charge will cause polarization of the metal structure, but no net charge on the metal structure. No matter whether the cable carries a net charge or if it is polarized, sparking can occur if the cable is inserted into a grounded connector.
- The type of shield structure: No shield, such as UTP; shield present but not connected; foil shield; foil + braid shield; connection of the shield to the connector from pigtail to 360° shield.
- The contact sequencing will vary from an undefined sequence, as every pin has the same chance to mate first, to a typical sequence observed in a good USB cable: Shell first, then GND or 5 V, then data.
- Exposure of pins: Some connectors will not allow an ESD to a pin as the ESD will be diverted to the shell. However, other cables may not have a shell, or may not connect the shell and may allow direct ESD to pins.
- Probability of ESD: Connections like USB are inserted rather often, other connections, such as a video interface will be inserted into most devices less often.
- Form factor and chassis material: For example, some USB memory sticks often have no shield, no shell and may allow discharges via the plastic into the circuit.

4.3 Cables and Cable Discharge Events (cont'd)

To highlight the essential aspects, a brief analysis is provided for two interfaces; LAN and UTP. The details can be found in the cited literature and see 1.4 (for LAN).

4.3.1 Charging and Discharging of USB Cables

Electronic systems must tolerate electrostatic discharges in a typical user environment. The existence of badly shielded cables and poor contact between the shield and the connector requires studying real world waveforms for USB cable discharge events [Mar2017c, Stad2017]. Charged cable events have been investigated by charging a cable to a known voltage and then inserting the cable into a connector to measure the currents. However, environmental conditions and materials can change the charge level and related electrostatic charge voltage. But, for many practical cases, the voltages that a cable can reach via triboelectric charging are not well known. To address this concern, a set of experiments were conducted where the total accumulated charge was measured.

High charging voltages have been observed for:

- People sitting up from a chair.
- People removing a garment, such as a fleece jacket.
- Handling of plastic sheet material.

The voltages reached by walking on a carpet are usually much lower than the voltages reached by the situations described above.

An experiment was conducted measuring the voltages on cables that were rubbed against various clothing materials. The aim of this study by Rezaei et al. was to enhance the understanding of cable charging behavior under different humidity conditions, with a variety of rubbing materials [Rez2017]. The voltage levels and various dependencies for such cable charging were investigated. The charge levels translate into a voltage if the capacitance of the cable to ground is considered. The insertion of a charged cable into a USB connector may lead to a CDE. Throughout this section the act of plugging in a cable is called a “plug-in event”. The USB cable connected devices are potential sources of a CDE. A CDE occurs because of the USB cable being charged and then discharging to the USB connector of the connected device. Typical examples include discharge scenarios such as an ESD to USB drive with no shield, a USB cable connected to cellphone inserted into a grounded device such as a personal computer (PC), a USB HUB connecting multiple electronic devices together via USB cables, etc. The goal of the work by Mardiguian et al. and Stadler et al. was to understand the range of stress levels seen by the USB 2.0 A/B (type A and type B connectors) cable connected devices due to various USB cable discharges as a function of the charging scenario, cable shield quality, and cable connections [Mar2017c, Stad2017].

4.3.2 Overview of Charging Scenario

Investigation on the effect of relative humidity and materials on triboelectric charging of USB cables was performed experimentally. The measurement setup involved the use of different sweater materials to rub on the outer jacket of various cables. This action of rubbing of different sweaters on cables led to the charging of cables by a triboelectric charging process. Figure 2 depicts one of the sweaters and one of the cables used in the study.

4.3.2 Overview of Charging Scenario (cont'd)



Figure 2 — Rubbing of the Sweater on the Cable Leads to a Charge Developed on the Cable

4.3.3 Overview of Discharge Scenarios

Various USB discharge scenarios are possible. For example, the direct ESD discharge to a USB drive, or a charged human holding a cable and plugging it into a USB connector. The focuses of the study were the discharge into a USB connected device and a discharge into a USB connector during a plug-in event. They are illustrated in Figure 3 and Figure 4, respectively.

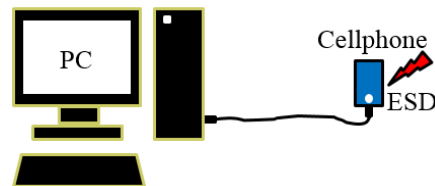


Figure 3 — Discharge into a USB Connected Device Scenario

In Figure 3 a cellphone is connected to a grounded device such as a personal computer (PC) by a USB 2.0 cable. A charged human can discharge into the cellphone and the ESD discharge source point is at the cellphone. The current flows via the USB cable to the grounded PC.

In Figure 4, a charged cable is inserted into the PC. The other end of the cable is connected to a USB device (a cell phone is depicted) which leads to a plug-in event.

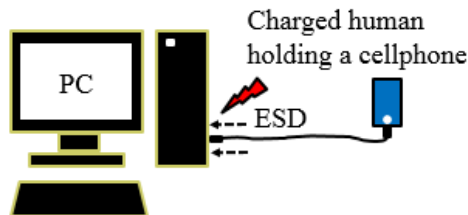


Figure 4 — Discharge into a USB Connector During a Plug-in Event

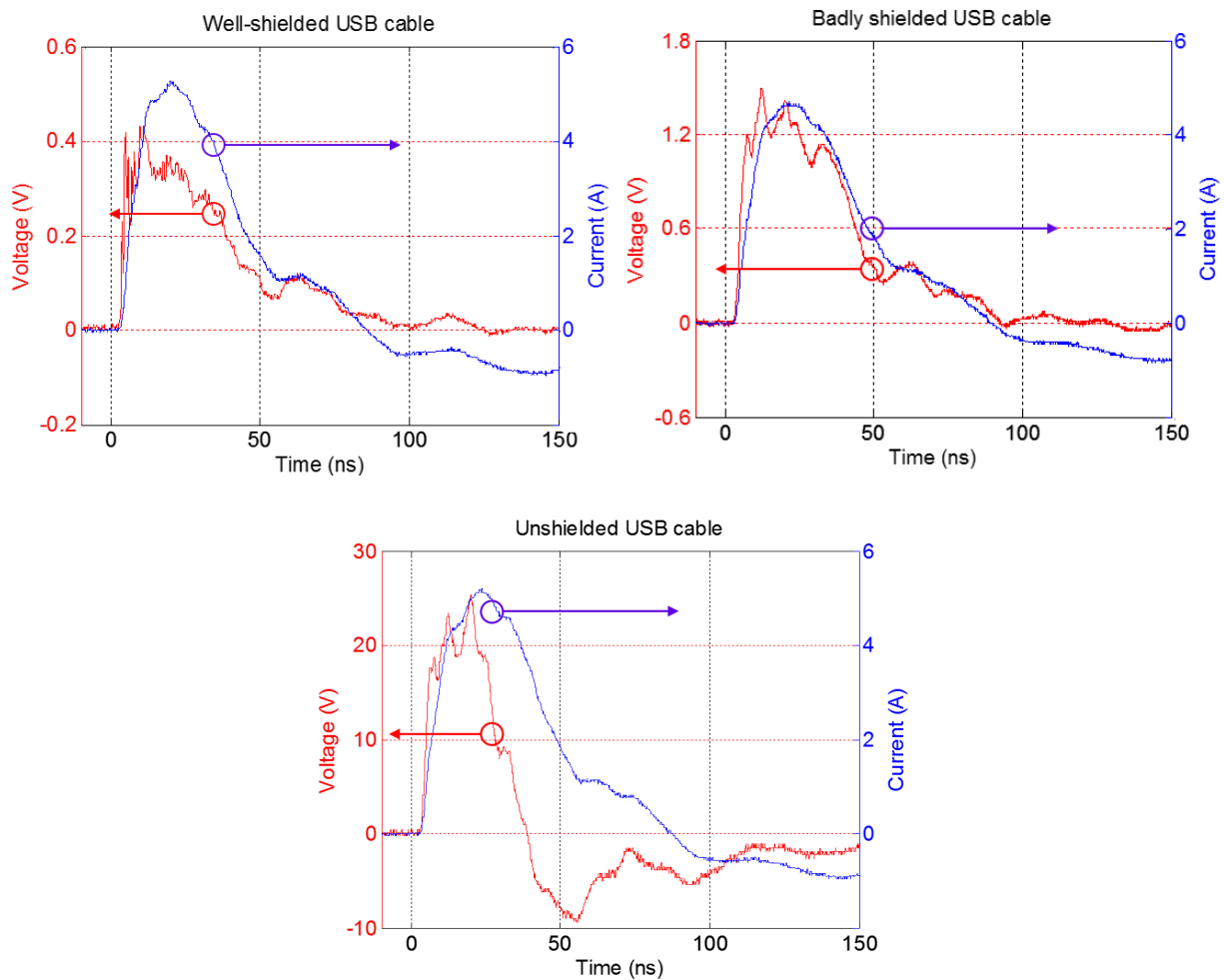
In this study, randomly purchased USB 2.0 A/B cables (USB 2.0 type B to type A) are classified into three different types based on their cable shield quality. A resistor inductor capacitor network (RLC) meter was used to measure the USB connector shell to shell DC resistance of the cable. This gives a first impression on the shield's properties. If the resistance is within several hundred milli Ω and does not change much when the cable is twisted, the cable is classified as a well-shielded cable. If the resistance is in the range of 1-80 Ω s and it changes during twisting, the cable is classified as a badly shielded cable. A few of the USB 2.0 cables purchased had no shields. In addition, the shields of a few USB cables were cut for experimental purpose. Cables with a cut shield or no shield are classified as an unshielded cable.

A block diagram for this series of tests is shown in Figure 5. 2 kV contact mode ESD was injected into the conductive enclosure of the DUT box, resembling a situation in which an ESD occurs to a USB connected device (such as a USB drive) connected to a PC. For such a situation, data traffic can be active, while there cannot be data traffic during a plug-in event.



The graphs in Figure 6 show the common-mode current on the USB cable as captured by the F-65 monitoring probe clamped close to the scope box and the voltage induced between D+ and ground on the scope box side. The measured waveforms for the well-shielded, badly shielded, and unshielded USB cable types are shown in Figure 6.

4.3.5 Discharge into a USB Connected Device (cont'd)



NOTE Data is shown for well-shielded, badly shielded, and unshielded type USB cables. The ESD gun is discharged at 2 kV in contact mode. The negative current readings are a measurement artifact of the F-65 current probe. Common-mode current and voltage induced between D+ and ground for a discharge into a USB connected device scenario.

Figure 6 — Common-Mode Current and Voltage

At a 2 kV contact mode discharge, a noise voltage of 0.4 V is measured for the well-shielded cable, 1.2 V is measured for the badly shielded cable, and approximately 20 V are measured for the unshielded cable (without taking the reaction of ESD protection into account). In contact mode the ESD gun discharge current has a linear relationship to the ESD gun voltage setting. If the same measurement is performed at a higher ESD gun voltage, the amplitude of the measured waveform is expected to increase linearly.

At 2 kV for an unshielded cable the peak current occurs at 20 ns and the amplitude is approximately 5 A as shown in Figure 6. The initial peak current would be 2×3.75 A, but it returns via the DUT box to ground capacitance and is therefore not visible in the F-65 current clamp data. The designer is often interested in a realistic worst-case specification. Although possible in some rare situations, direct discharges into pins were disregarded and the discharge into a USB connected device for the case of an unshielded USB cable was considered the realistic worst case.

4.3.5 Discharge into a USB Connected Device (cont'd)

If the ESD gun had been set at 8 kV, a current amplitude of 20 A would be expected. It should be noted that the current measured using the F-65 current clamp is the common-mode current and it is not a function of the type of USB cable used. In the case of a badly shielded or unshielded cable it is reasonable that the common-mode current splits equally over the four wires of the USB 2.0 cable. Approximately a 5-A current will flow on each of the four wires, GND, Vbus, D+, and D-. This assumption is based on the fact that all wires are connected via low impedances to ground. The 5 V (Vbus) is usually connected via a large value capacitor, and D+ and D- have ESD protection diodes either on the board or in the IC. A current of 5 A with pulse widths of 10's of nanoseconds on the IO lines (D+ and D-) can cause hard failures. Here the pulse width is not determined by the cable length, but by the source.

4.3.6 Discharge into a USB Connector during a Plug-in Event

When a charged person holds a cellphone connected to a USB cable, the charge will be distributed on the USB cable via polarization and/or charge migration. When the person inserts the USB cable into a grounded PC, ESD occurs. Figure 7 illustrates the test setup used to investigate plug-in events.

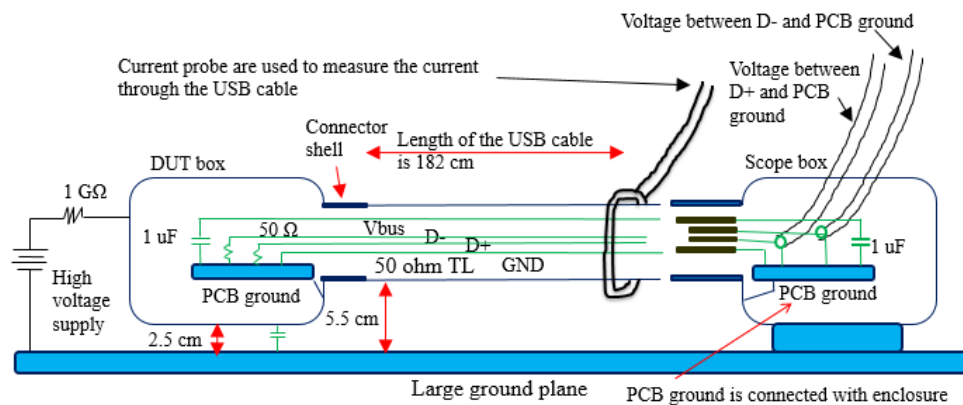


Figure 7 — Discharge into a USB Connector During a Plug-in Event

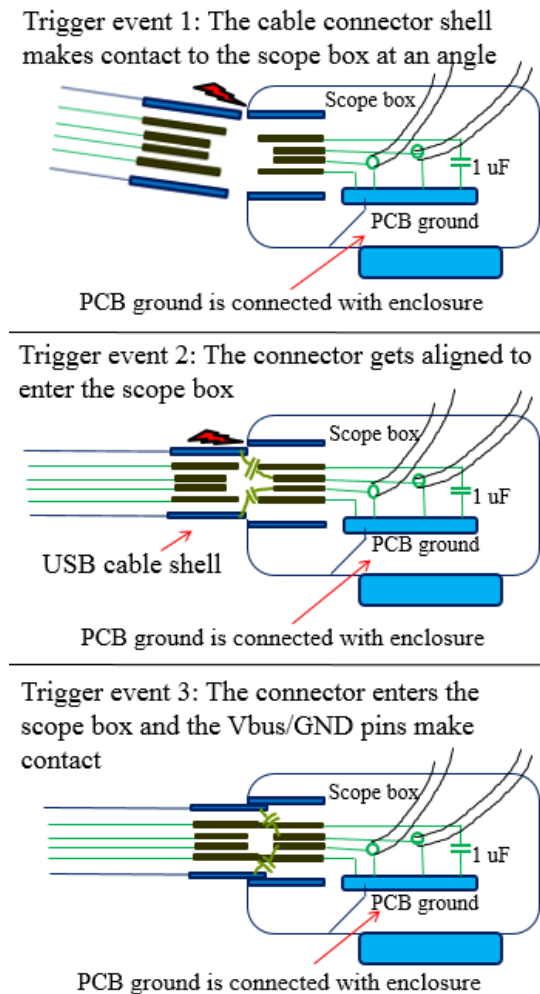
Because of the design of the USB connectors, the shell will contact first, then the GND/Vbus pin follows, and finally D+/D- will contact. Even if the cable is unshielded, GND/Vbus will contact first.

4.3.6.1 Plug-in Event Sequencing

During the plug-in measurements the cable was charged via 1 GΩ. The unconnected end of the USB cable was held by hand using insulated gloves, then the operator inserted the cable into the scope box. Multiple pulses can occur during the insertion process. To be able to capture pulses that occur with microsecond delay times, a fast re-trigger mode was selected. Another application of the fast retrigger mode or sequence mode acquisition is shown in [Mar2017b], and [Mar2018], which explains the use of the fast re-trigger mode in capturing multiple pulses. The measurement was performed using ultra-segmentation (Rohde & Schwarz) or sequence mode acquisition (Teledyne LeCroy) activated on the oscilloscope. The oscilloscope can be triggered on the channel connected to the F-65 current clamp or the D+ signal.

4.3.6.1 Plug-in Event Sequencing (cont'd)

The USB cable connector may not always enter the scope box in parallel to the connector. It may hit the scope box at an angle to be aligned for entering the scope box connector. This action leads to multiple triggers for a single plug-in event measurement. A possible sequence is illustrated in Figure 8.



NOTE It should be noted that multiple triggered events can occur in a plug-in measurement.

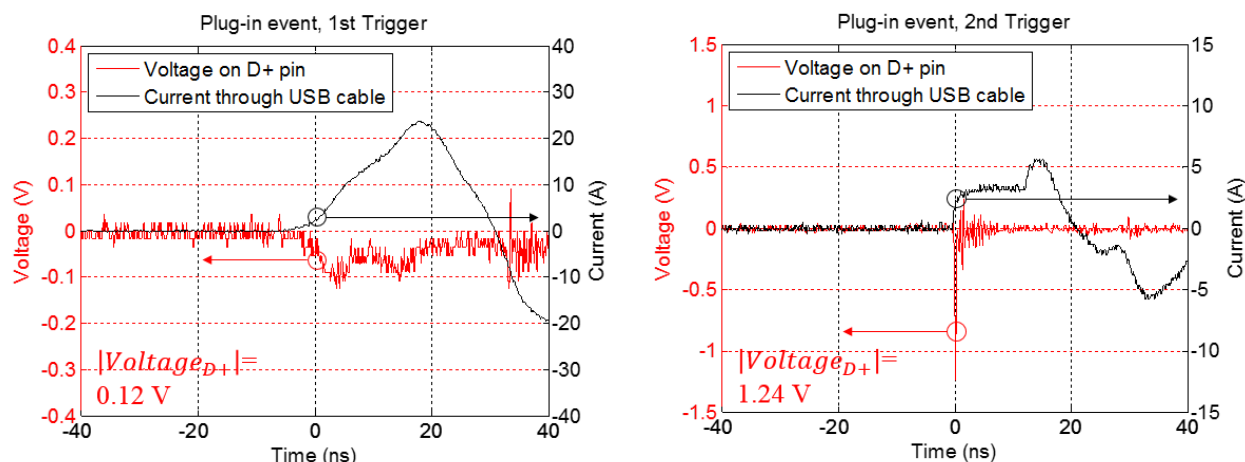
Figure 8 — Plug-in Event Sequence Explained Using Three Triggered events

4.3.6.2 Plug-in Event Measurement Results

A set of measured typical waveforms during a plug-in event is shown in Figure 9. They are based on charging the DUT box to 8 kV and using a well-shielded cable. In this setup the USB cable behaves as a transmission line (wire above the ground plane) having an impedance approximately equal to 266 Ω (1 kV/3.75 A). In this measurement setup, the USB cable GND wire was directly connected to the scope box PCB ground. The USB cable Vbus wire was terminated with a 1 uF capacitor on the PCB inside the scope box. Neither of these wires were monitored during the plug-in event measurements. However, emphasis was placed on the IO lines (D+ and D-) of the USB 2.0 cable. The waveforms induced on the D+ and the D- IO signal lines due to the plug-in event were comparable.

4.3.6.2 Plug-in Event Measurement Results (cont'd)

The F-65 current clamp, D+, and D- channels can be used to trigger the oscilloscope. In this case the oscilloscope was triggered on the D+ channel and the ultra-segmentation/sequence mode was enabled. It should be noted that the oscilloscope is triggered on the D+ channel to observe the waveforms induced on the IO signal lines due to the plug-in event. This leads to a few of the initial current waveforms through the USB cable not being acquired by the oscilloscope.



NOTE Measured waveforms for the first and second triggered event are shown.

Figure 9 — Discharge into a USB Connector During a Plug-in Event.

During the plug-in sequencing, the first event caused lower ESD-induced voltage (0.12 V) on the D+ pin because most of the current flowed between the USB shell and the scope box. The second plug-in triggered event had a higher ESD-induced voltage on the D+ pin (1.24 V).

4.3.7 Summary of USB Risks

A triboelectric charging scenario was investigated for various types of cables [Rez2017]. Two USB 2.0 cable discharge scenarios were investigated [Mar2017c, Stad2017]. The first scenario investigated ESD on a USB cable connected system. The second scenario investigated a plug-in event of a connected USB cable.

In the measured waveforms for the first discharge scenario, the discharge into a USB connected device shows pulse widths on D+ (IO signal) of 20-40 ns and 2-10 ns rise times at 2 kV contact mode ESD to the USB connected device. If 8 kV is set as the expected reliability level for the user environment, then the ESD protection needs to be able to handle 5 A for tens of nanoseconds on the D+ and D- at the same time. Here, damage, as well as latch-up or soft failures may need to be considered. The plug-in of an already device-connected cable has a lower chance of causing damage. The voltages induced in D+ by a discharge between a USB cable and a grounded connector during the insertion show less than 5 V at 8 kV for the well-shielded and the badly shielded cables. For the case in which the USB cable has no shield, a voltage of approximately 12 V has been induced at 8 kV. This translates to a current of 0.24 A (oscilloscope channel impedance of 50 Ω) on the D+ IO line. It should be noted that even though this voltage amplitude may look significant, the duration of the pulse width is less than 10 ns as shown in Figure 9. Soft failures may still be possible if a cable is inserted into a USB HUB servicing multiple USB connections. Here, other active connections could be interrupted by the insertion of a charged USB cable even if the voltage is rather small.

4.3.7 Summary of USB Risks (cont'd)

The system designer must account for the fact that a large portion of the USB 2.0 cables on the market have no shield. About 1/3 of the thirty USB 2.0 cables randomly selected for this study had no shield or no shield to USB connector shell connection. ESD protection circuits should be designed to protect electronic device from CDE stress levels up to as much as 5 A for tens of nanoseconds on the D+/D- IO lines for an 8 kV device stress level.

4.4 Cable Discharge of LAN Cables

One needs to distinguish between Ethernet ports that use a transformer, often called magnetics at the port, and those which have a direct connection to the circuit. The transformer provides a high voltage isolation barrier of at least 1500 V, and in the short term, nanosecond long pulses probably > 5000 V. It also provides a common mode return path via the Bob Smith circuit, and via ferrites for PoE devices. Further, the transformer will saturate at rather low currents. This saturation will reduce the coupling between the primary and secondary side, thus, reducing the coupling of the physical layer interface IC. This section analyzes LAN interfaces, such as UTP, which use a transformer.

In contrast SFP + DAC cables (small form-factor pluggable + direct attach copper) directly provide an entry path, without magnetics, to the physical layer interface IC. These cables are shielded, having a shielded connector that mates at the shield first. However, direct discharges to the pins are, although not likely, possible. The ESD performance of such cables has not been investigated yet.

The protection strategies for an electronic system against ESD are mainly developed based on the type of ESD source, the discharge mechanism, and the likelihood of its occurrence. An IC located internal to an electronics system is at a lesser risk to an ESD event when compared to an IC having an interface that is exposed to the external world. For example, Ethernet physical layer (PHY) transceivers may be subjected to CDE, which is not the case for on board interfaces between ICs such as DDR interfaces.

When a charged LAN cable is plugged into an Ethernet connector [Gan2016], a cable discharge event will occur. The discharge voltage and subsequent current can damage the transformer, the common mode chokes, and especially the Ethernet PHY IC transceivers.

Over the past few years, researchers have understood that CDE needs to be treated separately from other types of ESD tests due to vast differences between the effects caused by CDE. LAN cable discharge pulses can be quite long and have the potential to stress the IO more than those discharges described by an HBM or IEC 61000-4-2 discharge model. Additionally, the LAN cable discharges lead to shorter rise times compared to the 0.8 ns rise time of the IEC 61000-4-2 standard. These shorter rise times may require faster turn on performance of the electrostatic discharge protection circuit.

4.4.1 Cable Discharge of LAN Cables Introduction (cont'd)

Some of the important differences are listed in the Table 1.

Table 1 — Comparison between Different ESD Models

Parameter	HBM	CDM	IEC 61000-4-2	CDE
Rise time	2 to 10 ns	100 to 500 ps	~ 0.8 ns	100 to 300 ps
Pulse duration	150 ns	~ 2 ns	~ 80 ns	up to several milliseconds (depends on the cable length)
Peak current	0.7 A/kV	1- 16 A (depends on the size of IC)	3.75 A/kV	Peak: ~5 A/kV Plateau: ~3 A/kV

The effects of LAN cable discharges leading to malfunction or even damage is presently not covered by any of the ESD immunity test methods. IEC 61000-4-2 is used to verify the ESD withstand capabilities, i.e. immunity of equipment, directly at its enclosure port and the metal shells of connector ports (excluding direct discharges to the pins). Complying with the system level IEC 61000-4-2 standard may not ensure enough robustness of the Ethernet system against LAN cable discharge. Several semiconductor manufacturers dealing with these communication interfaces have developed their own in-house CDE testers to qualify their ICs. However, the need for standardizing the test procedure is ever growing.

4.4.1 LAN Cable Charging Scenario

When a LAN cable is pulled over a surface, the cable may get charged due to a triboelectric effect. A LAN CDE can also occur if a person, who carries a laptop and is charged, inserts a LAN cable which is at ground potential. Other LAN CDE sources may be a charged device close to a cable which polarizes the cable.

The voltages of a LAN cable can appear between: (1) All twisted pairs and ground (common mode); (2) Wires of a single pair (differential mode); (3) Different pairs in the cable (mixed mode). The LAN cables can be charged in common mode and, although with a smaller likelihood, in differential mode. However, during the discharge sequence (pin sequencing) a cable which is charged in common mode can become charged in differential mode.

In [Gre2009], the average surface charge density on a short cable was experimentally measured by pulling it through an inline tribo-electrification charger consisting of a sleeve fabricated from numerous different plastic materials, including PTFE and aluminum, to provide friction against the cable jacket. The surface charge was measured using an electrometer. Examples of the surface charge measured densities are:

- 1) For a PTFE charging sleeve: $\sigma = 0.1 \cdot 10^{-8} \text{ C.cm}^{-2}$;
- 2) For aluminum charging sleeve: $\sigma = -0.15 \cdot 10^{-8} \text{ C.cm}^{-2}$.

4.4.1 LAN Cable Charging Scenario (cont'd)

In another study [Wan2013a], a similar experiment has been performed where a spooled category (CAT) 6 cable is unwound over flooring materials like a high-pressure laminate, a typical surface material for a raised floor system. An example of the measured voltage (1.1 kV) is shown in Figure 10 and Figure 11.

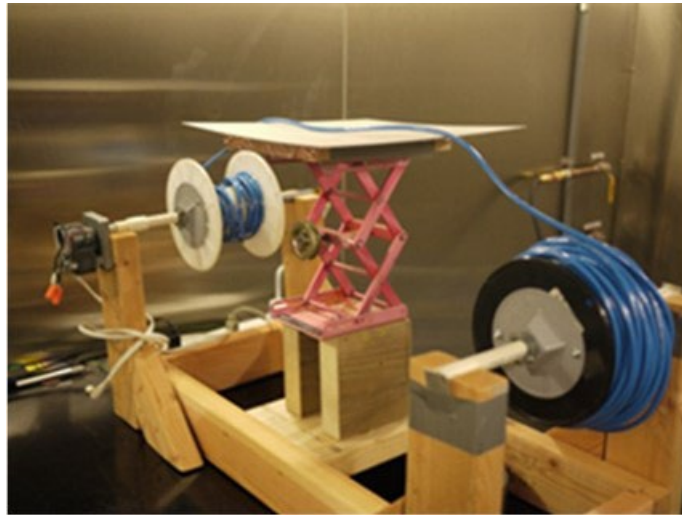
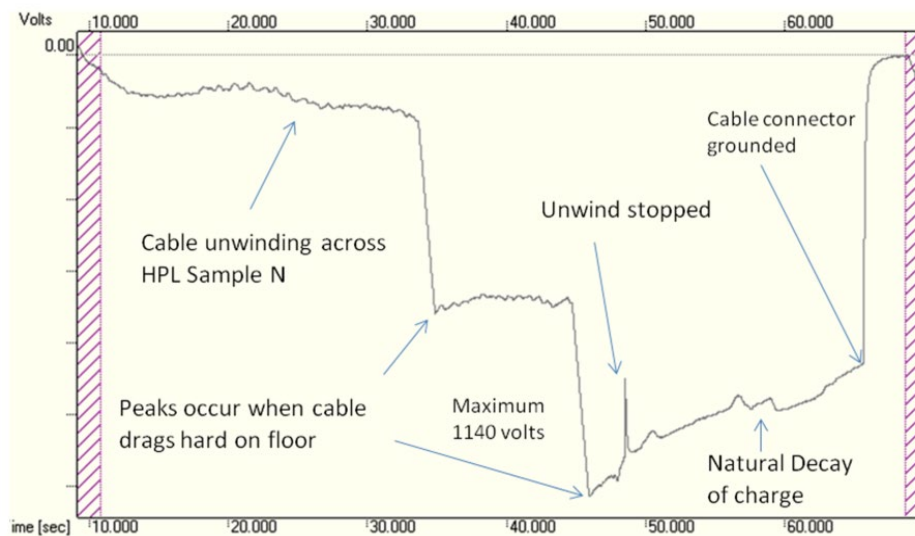


Figure 10 — CAT 6 Cable Unwind Test Set up

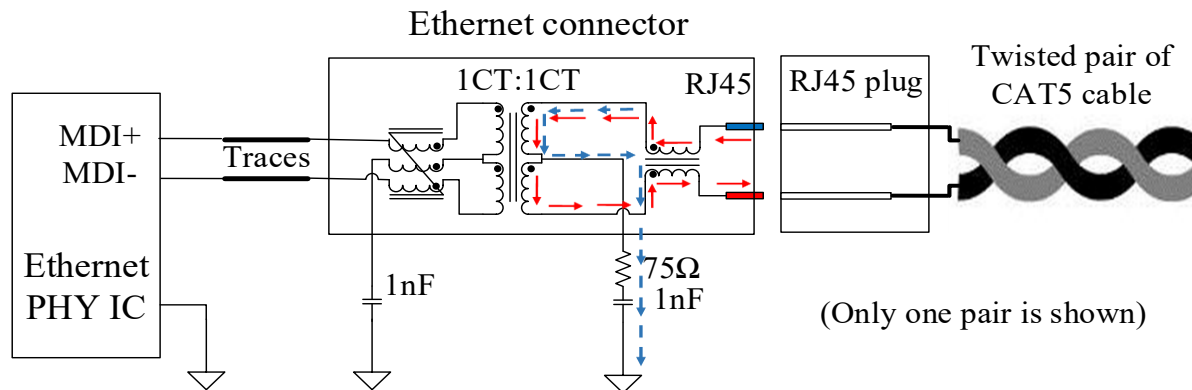


NOTE Voltage on the inner conductor of a CAT 6 cable during unwinding across a high-pressure laminate floor.

Figure 11 — Voltage on the Inner Conductor of a CAT 6 Cable

4.4.2 Typical LAN Cable Discharging Scenario

As shown in Figure 12, a typical LAN cable discharge situation includes: (1) Charged cable; (2) transformer possibly having common mode chokes included in an Ethernet connector; (3) PHY IC transceiver interface pins. The primary-side center tap of the magnetics is usually connected to a Bob Smith termination circuit which consists of a resistor and a high voltage capacitor. During a LAN CDE, the discharge sequence, the Bob Smith circuit, the magnetic group and the PHY IC pin dynamic impedance will all affect the discharging scenario.



NOTE The system contains four pairs, here, only one pair is shown.

Figure 12 — Schematic Diagram of the LAN Cable Discharge Situation

When a charged LAN cable is plugged into an Ethernet LAN connector, not all pins make contact at the same time. One of the pins will spark over first. The first pin that contacts initiates a current flow between that wire and the LAN connector. Then, at least two different modes can be initiated by the second pin that mates. The second pin can either be from the same twisted pair, or from another twisted pair.

The assumption is that the LAN cable is charged in common mode. In other words, all 8 wires of the cable have the same potential with respect to a reference plane. When the first pin contacts, the discharge current flows via the common mode choke, and one half of the transformer primary winding to the Bob Smith termination circuit. The first pin discharge current path is illustrated by the blue arrows in Figure 12. This is referred to as a differential mode discharge, and the current magnitude mainly depends on the Bob Smith termination type, the common mode impedance the cable forms with respect to reference ground, and the charge voltage. Typical values for the resistor and the capacitor in the Bob Smith circuit are $75\ \Omega$ and $1\ \text{nF}$ respectively, but other realizations are possible. For example, if power over Ethernet is provided, the capacitor value may be much larger. Furthermore, many center taps from different pairs or even cables may connect together and share the same termination circuit. This makes the first pin discharge current path become more complicated as multiple PHYs may be affected by one discharge.

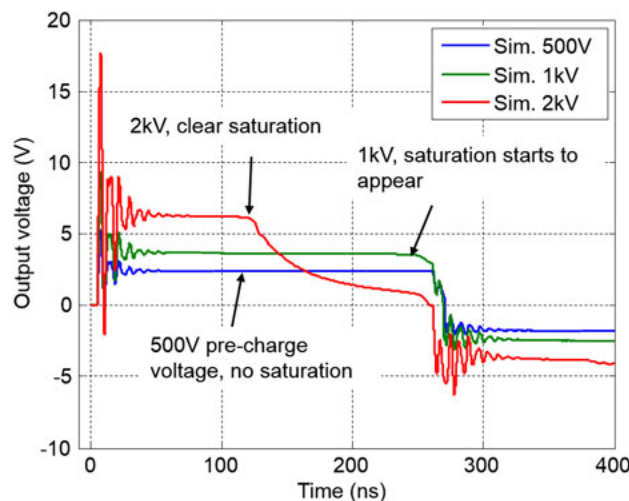
If the second pin that mates is from the same twisted pair, the second pin discharge current path is illustrated by the red arrows in Figure 12. In this case, the current will flow through the transformer primary winding, and the first pin will be the main current return path. This is also referred to as a differential mode current.

4.4.2 Typical LAN Cable Discharging Scenario (cont'd)

As the discharge currents are in differential mode, the common mode chokes in the magnetic group cannot suppress the CDE currents. Differential mode discharge situations can occur under two circumstances:

- First contact causes a current flow from a pin, via the transformer, to the Bob Smith circuit, and
- If the first discharge caused a differential voltage on a pair (the analysis of this requires knowing the capacitance distribution between the wires, pairs and to ground) and the second pin that contacts is from the same pair, then a differential current will flow.

Most discharge currents will transfer to the PHY IC pins through the magnetics. The failure level of the PHY IC will depend on the magnetic module which are manufactured in several different configurations. Due to the large currents during an ESD event, nonlinear effects such as core saturation must be considered. The saturation of the magnetic cores can limit the amount of energy which is coupled into the transceiver circuit. In [Gan2016], the LAN CDE second pin discharge simulation result shows that the long pulses or high current levels will saturate the transformer, and this effectively reduces the PHY IC current, protecting the IC (see Figure 13).



NOTE Voltage at the PHY IC pin side for a 25m long cable at different charge voltages [Gan2016]

Figure 13 — Voltage at the PHY IC Pin Side

4.5 Protecting Radio Frequency (RF) Antennas

With the increase of mobile and wireless applications, protection of the RF antenna ports from ESD becomes both critical and challenging. Antenna reception and signal integrity are important figures of merit for these products and virtually anything that is added to the circuit to protect it from ESD will impact its performance. Thus, considerable effort must be focused on either making the antenna self-protecting or minimizing the impact of the ESD protection elements.

4.5 Protecting Radio Frequency (RF) Antennas (cont'd)

One of the most common antennas in use for wireless applications is the planar inverted F antenna (PIFA). This antenna has a ground leg and thus can be inherently self-protecting. An example of a tunable PIFA antenna is shown in Figure 14.

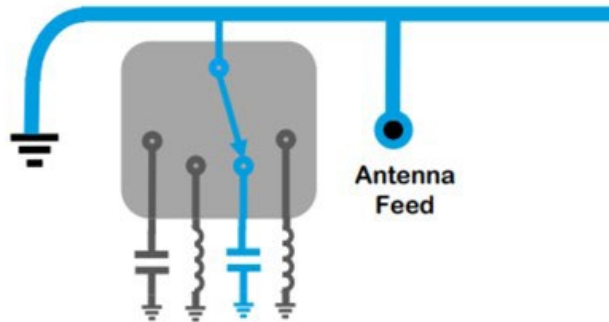


Figure 14 — Tunable PIFA Antennae

While the PIFA antenna is indeed grounded, care must be taken in designing the actual ground network. An antenna connected to a noisy analog ground will impact performance and can dramatically lower the antenna's performance. Thus, there is a tendency to design a DC ground that also provides some RF isolation. This is typically done by adding inductance in series with the ground connection. But this can defeat the purpose of an effective ESD ground. The Fourier transform of the initial peak in the IEC 61000-4-2 contact discharge pulse contains significant contribution from frequencies as large as 1 GHz. Furthermore, there are additional high frequency components in the typical ESD gun pulse. Any inductance to ground in the PIFA antenna ground net will degrade the grounding of the high frequency components in the system level ESD pulse. Effective grounding of the antenna will require designing a ground net that provides some level of RF isolation as well as an effective ESD ground.

The second type of antenna in common use is the monopole antenna. This antenna tends to be higher performance than the PIFA antenna, but it is much more difficult to protect. An example of a tunable monopole antenna is shown in Figure 15. Since the antenna has no ground of its own, ESD protection design becomes critical.

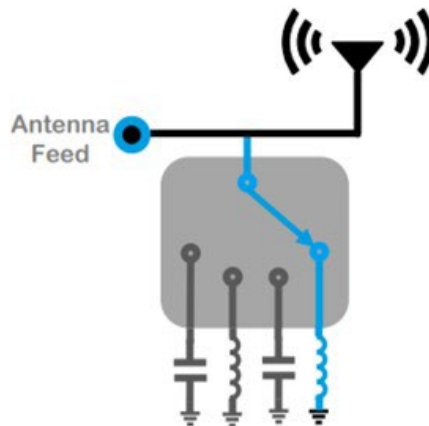


Figure 15 — Tunable Monopole Antennae

4.5 Protecting Radio Frequency (RF) Antennas (cont'd)

There is a tendency by companies that find the ESD protection of the antenna system challenging to push the requirements for ESD protection back on their component suppliers. This will lead to inefficient ESD designs since all the components connected to the antenna such as antenna switches, tuners, multiplexers, or other components must have their own protection. This not only duplicates ESD protection in the individual components, but it limits the ability of the system engineers from developing the most effective ESD protection that also minimally impacts performance. Ideally, the ESD protection of the antenna circuitry should be done at the system level so that there can be an efficient co-design of the ESD protection and RF performance circuit elements. With the development of ESD simulations at the system level through such approaches as SEED, the design of the RF antenna protection can be done much more intelligently.

Antenna ports that are external to the electronic component must, of course, be tested using the system level IEC 61000-4-2 test. For most wireless applications, including mobile phones, the device must pass Level 4 testing. Consequently, if the antenna is exposed, it will need to withstand 8 kV contact discharge testing. For antennas that are not exposed, they need only be protected sufficiently to withstand the 15 kV air discharge testing that is applied to the non-conductive exterior of the electronic device.

5 Direct Pin Injection

5.1 Purpose of Direct Pin Injection of IEC 61000-4-2 Pulse

In real world stress situations IC pins are usually well shielded from ESD discharges. This includes mechanical design measures like pre-mate contacts of cable connectors, grounded shield metal of the connector and the chassis and electrical protection by filtering components on the PCB which mitigate the transient pulse on the PCB line towards the IC pin. Nevertheless, a partial stress, typically referred to as a residual pulse on the PCB line, can reach the IC component and cause damage or a malfunction. Also, an electromagnetic coupling can occur between the direct discharge path and nearby sensitive PCB paths.

Currently the direct discharge of an IEC 61000-4-2 pulse to a connector pin is excluded from IEC 61000-4-2 if a grounded shield is provided by the connector. However, as system design needs to consider the aspect of a residual pulse, it is industry practice that IEC 61000-4-2 pulses are applied to the connector pins even though IEC 61000-4-2 excludes this test. Since there is no specification of this test, performing this stress and the target values are largely differing. Primarily IEC 61000-4-2 ESD gun simulators are used due to the wide availability of the test equipment. Even if the waveform of the IEC 61000-4-2 spec does not match the waveform of the cable discharge, the practical experience of many generations of systems designs produced in high volume has shown that it provides a relevant test of the robustness in the field. This can be explained in that typically IEC 61000-4-2 failure mechanisms are dependent on the power or energy of the stress pulse and not on the details of the waveform. With increasing speed and downscaling of technologies a well-defined IC/PCB co-design is important to satisfy performance as well as robustness requirements. The essential base is the common understanding of the type of stress and the targeted stress levels by the IC and system design. This requires a clear specification of the direct pin discharge to the connector pins. The purpose of the clause is to recommend a relevant and practical direct pin injection test at the system level.

5.2 Applying IEC 61000-4-2 Gun Pulses to IO Lines

Applying an IEC 61000-4-2 pulse to a connector pin using the commercially available ESD simulators poses various difficulties. To ensure a reproducible and well-defined discharge, a contact discharge to the pin under investigation should be performed. Due to the geometry of the connector pins with small distances and the large tip of the gun it can be difficult to impossible to contact a single pin (see Figure 16). In addition, the pins are often situated deeply inside the connector. A viable solution is a fan-out board with test pads of each line under test where the gun tip can reliably be contacted (see Figure 17). The board needs to have an appropriate jack to the connector and the board parasitics should be minimized.



Figure 16 — Comparison of a USB-C Connector Size and the Tip of an IEC 61000-4-2 Gun

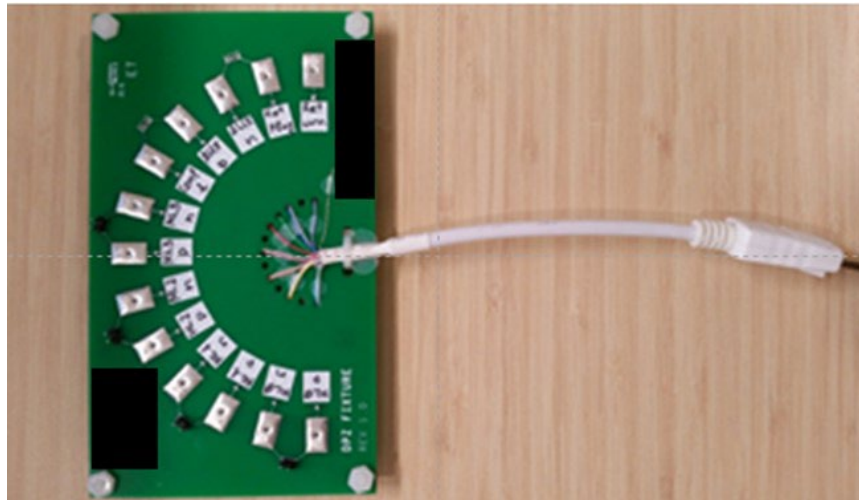


Figure 17 — Example Fan-out Board Used for Direct Pin Injection

As the PCB trace between the device pin and transient voltage suppression (TVS) diode acts as an inductor with efficient high frequency filtering in case of a low impedance state of the TVS diode, a 2-3 cm length of the PCB line between the branch point of the TVS diode and the IC pin landing pad is sufficient to block any overshoots related to fast transients in the first 5-10 ns of the residual pulse. Longer traces help to divert more current into the TVS path over the full pulse length.