

JEDEC PUBLICATION

GDDR5 Measurement Procedures

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GDDR5 MEASUREMENT PROCEDURES

(From JEDEC Board Ballot JCB-13-55, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 Scope

This publication is to inform all industry participants of a unified procedure to enable consistent measurement across the industry. This document contains the measurement procedures for testing GDDR5.

This document provides the test methodology details on:

1. CK and WCK Timings: t_{CK} , t_{WCK} , t_{CH}/t_{CL} , t_{WCKH}/t_{WCKL} , CK TJ/RJrms, CK and WCK Jitter
2. CK and WCK Input Operating Conditions: VIXCK, VIXWCK, VIDCK(ac), VIDWCK(ac), VIDCK(dc), VIDWCK(dc), CKslew, and WCKslew
3. Data Input Timings: t_{DIVW} , t_{DIPW}

NOTE The procedures described in this document are intended to provide information about the tests that will be used in JEDEC GDDR5 recommended measurement parameter. This testing is not a replacement for an exhaustive test validation plan.

2 CK and WCK Timings

2.1 Test Setup

1. Probe differential at the {W}CK and {W}CK_c to the oscilloscope input channels. Connect one channel ve+ to {W}CK and ve- to {W}CK_c.

NOTE Specs are defined “at the pin”; however this is difficult when implemented in a design and require probing at vias or probe points at some distance from the pin. An analysis needs to be done to determine best probe distance from the pin. It is recommended that probe points, termination and so forth be noted with the measurement results.

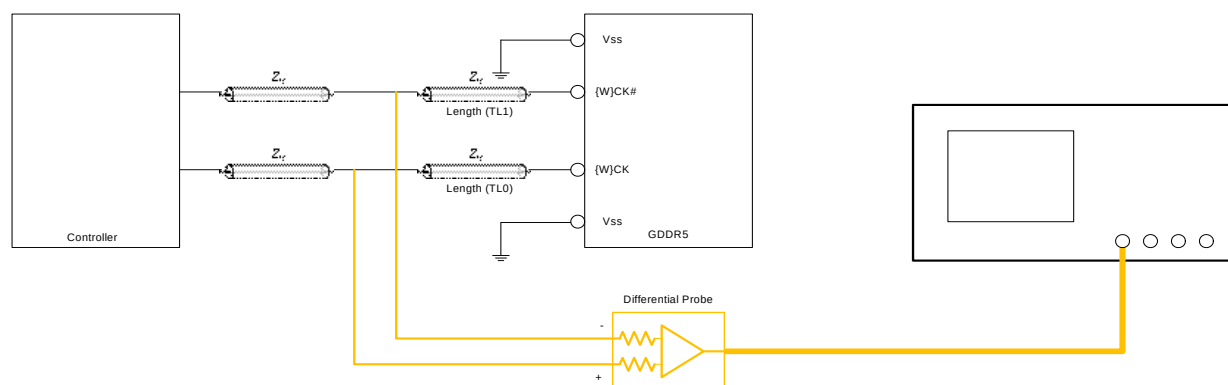


Figure 1 — CK and WCK Timings Measurement Setup – differential

2.2 tCK and tWCK Measurement Procedure

tCK and tWCK are calculated as the average clock period across any consecutive N_{top} cycle window, where each clock period is calculated from rising edge to rising edge.

NOTE A single cycle can be less than $t\{W\}CK(avg)min. spec.$ and greater than $t\{W\}CK(avg)max. spec.$ Allowable jitter is a partner to these specifications.

$$t\{W\}CK = \left(\sum_{j=1}^N t\{W\}CK_j \right) / N$$

where $N=N_{top}$

2.2.1 Test Procedure $t\{W\}CK$

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to $\{W\}CK$ and $\{W\}CK_c$.
3. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.
4. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
 - a. Recall factory setup on the scope.
 - b. Set sample rate.
 - c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
5. Measure from rising edge at 0V to next rising edge at 0V across N_{top} cycles.

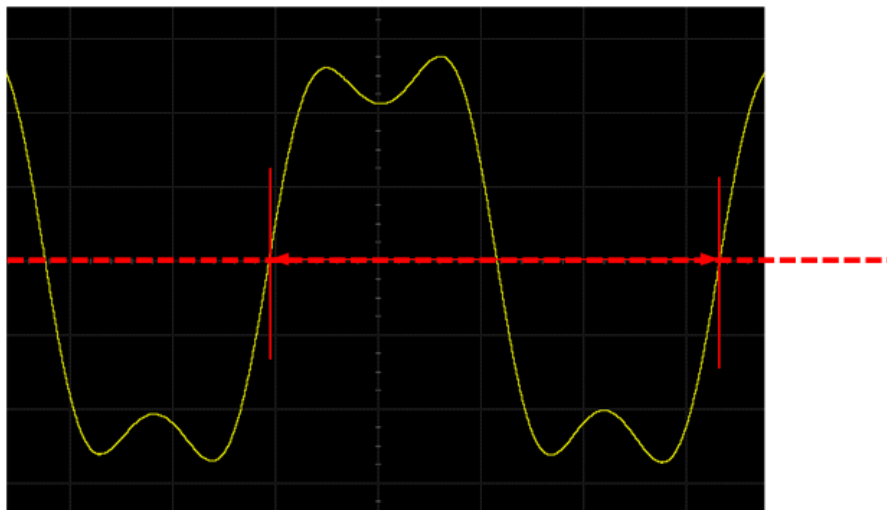


Figure 2 — $t\{W\}CK$ Measurement Example

2.2.1 Test Procedure t{W}CK (cont'd)

6. Calculate t{W}CK.

$$t\{W\}CK = \left(\sum_{j=1}^N t\{W\}CK_j \right) / N$$

where $N = N_{top}$

7. Record values and conditions and compare against specification.

Vdd/Vddq ¹	Temperature ²	Probe point TL0/TL1 ³	Termination ODT enable, disable, or external ⁴	Termination value ⁵	ZQ	Measured value ⁶

NOTE 1 Vdd/Vddq – Supply voltage used in measurement.

NOTE 2 Temperature – Ambient, or set temperature used in measurement.

NOTE 3 Probe point TL0/TL1 – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/location and characteristics of trace for {W}CK_c.

NOTE 4 Termination – ODT enable, disable, or external – Designate the type of termination used.

NOTE 5 Termination value – termination resistance.

NOTE 6 Measured Value – Value measured as per procedure.

2.3 tCH/tCL and tWCKH/tWCKL Measurement Procedure

tCH and tWCKH are defined as the average high pulse width, as calculated across any consecutive N_{top} high pulses. tCL and tWCKL are defined as the average low pulse width, as calculated across any consecutive N_{top} low pulse.

$$tCH = \left(\sum_{j=1}^N tCH_j \right) / (N * tCK(ave)) \quad tWCKH = \left(\sum_{j=1}^N tWCKH_j \right) / (N * tCK(ave))$$

where $N = N_{top}$

$$tCL = \left(\sum_{j=1}^N tCL_j \right) / (N * tCK(ave)) \quad tWCKL = \left(\sum_{j=1}^N tWCKL_j \right) / (N * tCK(ave))$$

where $N = N_{top}$

2.3.1 Test Procedure tCK/tCL and tWCKH/tWCKL

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to {W}CK and another to {W}CK_c.
3. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.
4. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
 - a. Recall factory setup on the scope.
 - b. Set sample rate.
 - c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
5. Measure from rising edge to falling edge at 0V for tCH and from falling edge to rising edge at 0V for tCL across N_{top} cycles.

2.3.1 Test Procedure tCK/tCL and tWCKH/tWCKL (cont'd)

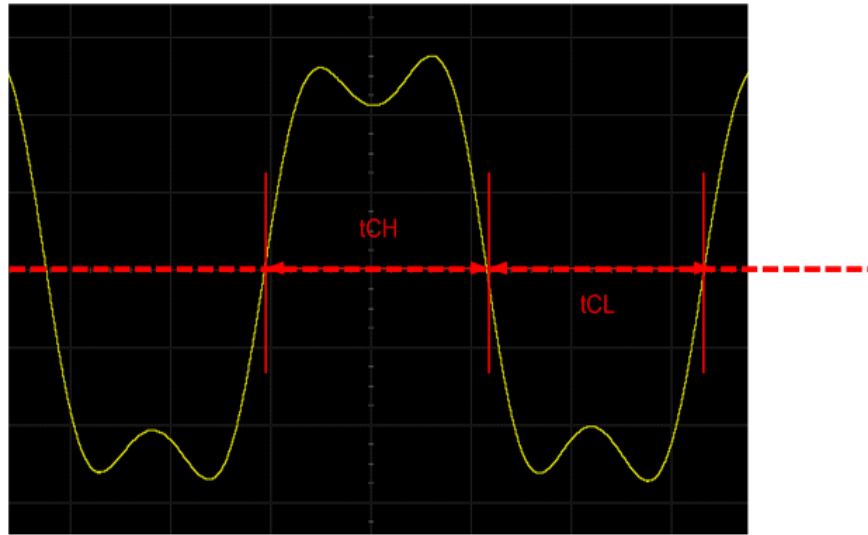


Figure 3 — tCH/tCL Measurement Example

6. Calculate tCH/tWCKH and tCL/tWCKL.

$$tCH = \left(\sum_{j=1}^N tCH_j \right) / (N * tCK(avg)) \quad tWCKH = \left(\sum_{j=1}^N tWCKH_j \right) / (N * tCK(avg))$$

where N=N_{top}

$$tCL = \left(\sum_{j=1}^N tCL_j \right) / (N * tCK(avg)) \quad tWCKL = \left(\sum_{j=1}^N tWCKL_j \right) / (N * tCK(avg))$$

where N=N_{top}

7. Record values and compare to specification.

Vdd/Vddq ¹	Temperature ²	Probe point TL0/TL1 ³	Termination ODT enable, disable, or external ⁴	Termination value ⁵	ZQ	Measured Value ⁶

NOTE 1 Vdd/Vddq – Supply voltage used in measurement.

NOTE 2 Temperature – Ambient, or set temperature used in measurement.

NOTE 3 Probe point TL0/TL1 – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/location and characteristics of trace for {W}CK_c.

NOTE 4 Termination – ODT enable, disable, or external – Designate the type of termination used.

NOTE 5 Termination value – termination resistance.

NOTE 6 Measured Value – Value measured as per procedure.

2.4 CK and WCK Jitter Measurement Procedure

Jitter for WCK and CK clocks are defined for N-cycle half-period jitter. TIE is measured across M_{jtr} half-cycles. TJN and RJN(rms) are calculated for each N-cycle half-period up to N_{top} at the tested Bit Error Ratio (BER).

Table 1 — Key Jitter Characterization Parameter

Parameter	Symbol	Min	Max	Unit	Note
Number of half periods per Jitter Measurement	M_{jtr}	$1e^{-6}$			1
Number of half periods across which Cumulative Error is Measured with PLL Off	$N_{top-off}$	50			
Number of half periods across which Cumulative Error is Measured with PLL On	N_{top-on}				2
Bit Error Ratio	BER				3,4

1. A half period, in this context, is one half of one clock cycle.

2. Vendor specified value.

3. Vendor specified Bit Error Ratio.

4. Bit Error Ratio is the probability for a single bit to be received in error. It is recommended that this value not be less than $1e^{-12}$.

For CK and WCK clocks, the maximum allowable jitter information can be measured and reported for N-cycle Half Period jitter as shown in Table 2. Refer to vendor specified values for application speed and PLL on or off case. The conditions involving temperature, VDD, and VDDQ are all recommended to be determined and reported along with the jitter results.

**Table 2 — Maximum Allowable Clock Input Jitter for N-Cycle Half Period Jitter $t_{CK}/t_{WCK} = t_{bd}$ Ghz
Temp = tbd, VDD = tbd, VDDQ = tbd**

N	RJ^N_{RMS}	TJ^N
1		
2		
3		
4		
5		
...		
N_{top}		

2.4.1 Test Procedure {W}CK Jitter

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to {W}CK and {W}CK_c.
3. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.
4. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
 - a. Recall factory setup on the scope.
 - b. Set sample rate.
 - c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.

2.4.1 Test Procedure {W}CK Jitter (cont'd)

- Measure at 0V crossing point from actual edge vs ideal for each 0 to Mjtr half-cycles. Ideal half-period is defined as a measured average creating a TIE mean of zero. $F_k = t_k - t_{refk}$, $k = 0, \dots, Mjtr$.

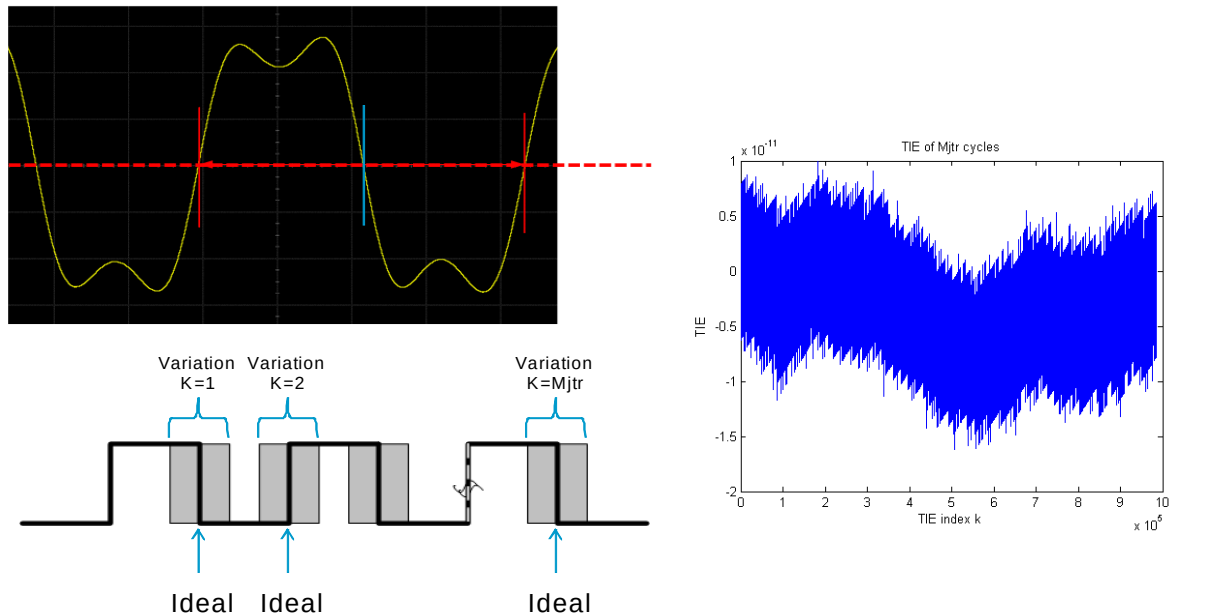


Figure 4 — Measure WCK and CK from Ideal

- Separate TIE sequence F into DJ and RJ sequences. After separation, each point in TIE can be represented as: $F_k = DJ_k + RJ_k$, $k=0, \dots, Mjtr$, see Figure 5.

NOTE There are several methods to separate RJ and DJ. Any method to separate RJ and DJ in to their index values is an acceptable method.)

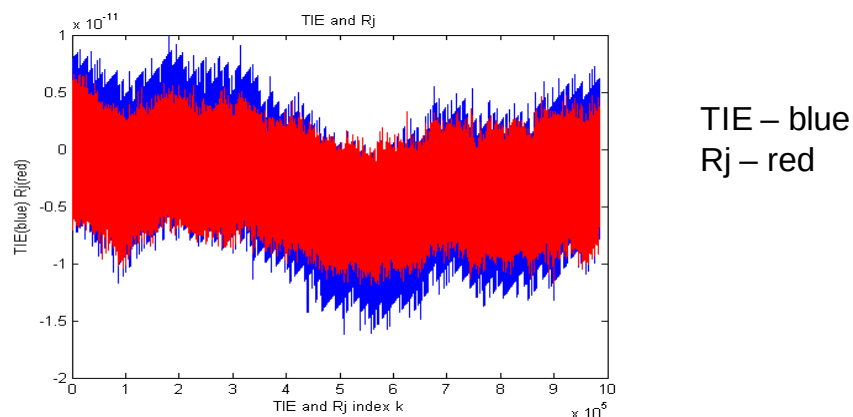


Figure 5 — Calculate Rj for each index k

- Calculate differences for F^N for TIE F and RJ^N for RJ for each N half-cycle. $F_k^N = F_k - F_{k-N}$ and $RJ_k^N = RJ_k - RJ_{k-N}$ where $k=N, \dots, Mjtr$; $N=1, \dots, Ntop$