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Understanding Electrical Overstress - EOS

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UNDERSTANDING ELECTRICAL OVERSTRESS - EOS

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Foreword

Damage signatures from Electrical Overstress (EOS) are the leading reported cause of returns in integrated circuits and systems that have failed during operation. Solutions to this problem are hindered by a prevailing misconception in the electronics industry that insufficient robustness to electrostatic discharge (ESD) is a primary cause of EOS. This document, White Paper 4, (WP) has been carefully compiled by the Industry Council on ESD Target Levels to foster a unified global understanding of what constitutes EOS and how EOS damage signatures can result from a wide variety of root causes.

The paper begins by outlining a brief history of EOS. It then presents the results of an industry-wide EOS survey. This survey gathered information on the types of EOS problems experienced by over 80 different companies, the relative importance of EOS to their overall business, and the methods assigned by these companies to address EOS issues. The survey provides a combined picture from which a more comprehensive definition of EOS can be made. The numerous categories and sub-categories of EOS root causes are explored in an attempt to understand how to create better specifications which will reduce their occurrence. In addition to the survey results, this paper studies many field returns with EOS damage signatures to establish the underlying root causes of damage and offers the respective identified solutions.

The survey and the case studies both show that successful failure analysis (FA) depends on careful communication between customer and supplier from the time a failure occurs until its cause has been discovered. Detailed investigation into manufacturing and handling processes is often necessary to accurately identify the root cause. This paper outlines a basic summary of the typical process flow for component electrical failure analysis.

The key point is that EOS issues can be mitigated when the proper understanding of IC design, factory and field environments, and system implementation is combined with effective communication across all these areas.

Introduction

In this introduction the Industry Council will address the most important electrical overstress (EOS) issues and conclusions of White Paper 4. Further details can be found in the various clauses of the document.

I.1 Purpose

This purpose of this white paper will be to introduce a new perspective about EOS to the electronics industry. As failures exhibiting EOS damage are commonly experienced in the industry, and these severe overstress events are a factor in the damage of many products, the intent of the white paper is to clarify what EOS really is and how it can be mitigated once it is properly comprehended. It is very clear that EOS is predominantly a matter of what customers do with devices, and in which applications the semiconductor specifications are exceeded causing destruction of the device. This white paper will describe those phenomena and explain the most important facts so that the involved partners in the industry have the opportunity to understand and recognize helpful steps for analysis and avoidance of EOS events.

I.1 Introduction (cont'd)

EOS is defined in terms of its impact inside applications. We focus on exceedance of specifications but not on how an exact specification was originally created. We focus instead on when and how the specifications are exceeded to cause EOS damage.

It is intended that this document be disseminated throughout the semiconductor industry for the benefit of those persons whose positions are concerned with the real nature of EOS. It is intended to serve as a foundational reference document for existing and future technologies.

I.2 Traditional Perceptions of EOS

Through the years, a high incidence of failures exhibiting EOS damage has been reported in most market segments of electronics and related industries, such as the automotive industry. This damage has often been mislabeled as “EOS Failure”, implying that these malfunctions are solely a result of a phenomenon or stress called EOS. Understanding EOS as a “stress” has led many customers to incorrectly assume a device experiencing EOS is “weak”. This misperception has led to requests to “improve” a device in regards to EOS.

Another incorrect assumption has been that EOS can be avoided by making devices more ESD robust to both the human body model (HBM) and the charged device model (CDM). This misconception has been addressed in JEDEC publications JEP155 [1], and JEP157 [2] where it is convincingly shown that the incidence of EOS is independent of the level of HBM and CDM robustness.

I.3 Industry Council Worldwide Survey

In preparation for this white paper, the Industry Council conducted a worldwide survey of the electronics industry concerning EOS. Results confirmed the long held view that EOS is consistently one of the “high bars” on product failure Pareto charts. Looking at the EOS survey, respondents reported greater than 20% of total failures being EOS-related or 30% of total electrical failures being EOS-related, making EOS the largest bar on the Pareto chart of that responder’s known causes of returns. One glaring revelation was the critical need for a better industry-wide understanding of EOS to address its issues.

Looking at the EOS survey further, misapplication (powered handling) stands out as the highest cause of EOS damage, with over 40% of respondents indicating EOS damage which occurred in the field as the most common location. Damage signatures associated with EOS often can involve package and silicon damage and are more extensive in a product than failure signatures resulting from events in the measurable ESD regimes. The main findings of the EOS Survey were:

- 1) **Powered Handling:** This stands out as the most widely reported root cause, involving a significant (over 20%) percentage of reported returns exhibiting EOS damage. Powered handling can include overvoltage, improper insertion, power supply sequencing, and incorrect biasing during use.
- 2) **Absolute Maximum Rating (AMR):** A number of returns exhibiting EOS damage were attributed to applied voltages exceeding the specified AMR voltage, indicating that incomplete or unclear maximum ratings may be an issue and that AMR characterization and improved AMR information on the datasheets is important to minimize the risk of EOS.
- 3) **ESD Related:** System level events, discharges from charged devices, and ESD controls in manufacturing which are not compliant with handling ESDS devices are additional root causes for EOS damage. Charged board events (CBE) and cable discharge events (CDE) also contribute.
- 4) **Miscellaneous Causes:** There were other miscellaneous causes reported that ranged from weak printed circuit board (PCB) designs to mishandling.

1.4 New Definition of EOS Incorporating AMR and EIPD

It became clear to the Council during analysis of the survey, as well as gathering data on customer–supplier experiences with resolving EOS-related returns that a new way of visualizing the relationship of AMR to EOS is sorely needed in the industry. The Council proposes that the relationship between EOS and AMR may be illustrated in the manner indicated in Figure 1. Definition of AMR and its relationship to device stress, reliability impact and long and short term damage potential allows semiconductor manufacturers to clearly provide the maximum voltage / current / power limits. This enables system manufacturers to incorporate devices into their systems safely and ensure an operational environment that does not exceed those maximum limits. This is based on the following EOS definition:

An electrical device suffers an electrical overstress event when a maximum limit for either the voltage across, the current through, or power dissipated in the device is exceeded and causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.

Critical to this definition is a clear understanding of what is meant by maximum limit. Clause 6 further expands this definition by providing a practical interpretation of EOS in terms of AMR. Insight into the electrical aspects of AMR can be gained by examining the voltage ranges illustrated in Figure 1.

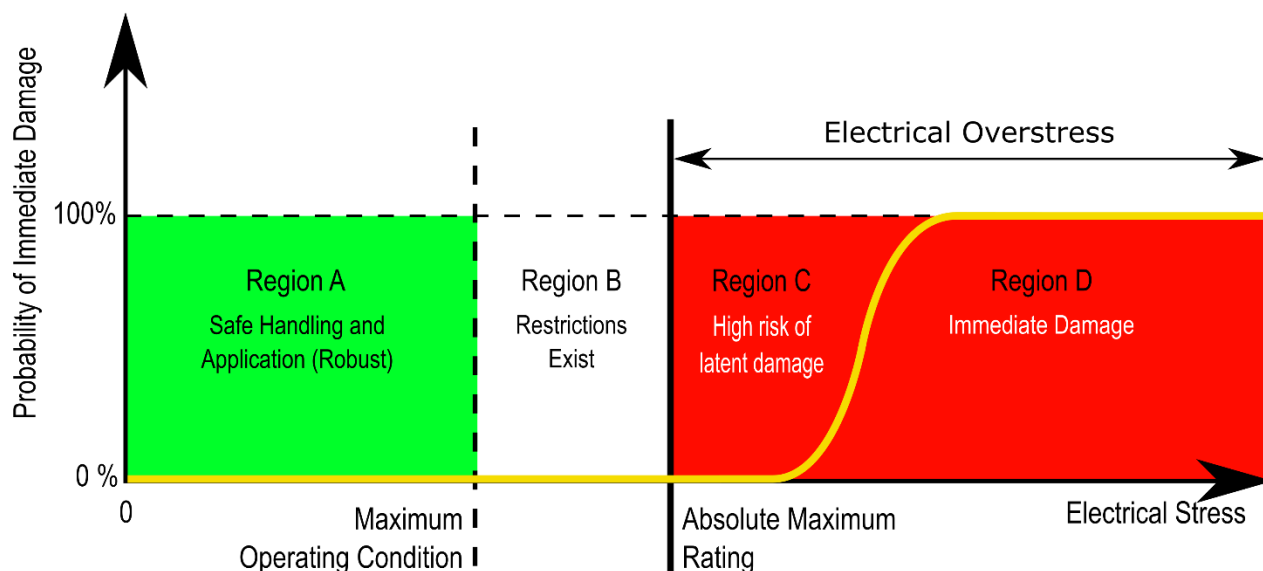


Figure 1 — A graphical depiction of how Absolute Maximum Ratings should be interpreted.
(The yellow line is the number of components suffering immediate, catastrophic EOS damage.)

First, there is the safe operating area, a region of robust operation (region A). This is the region in which the manufacturer designed the device to operate. This is followed by a region in which operating restrictions exist (region B). In region B, the device is not guaranteed to function as specified, however the device is not expected to be physically damaged. Operating the device in region B for extended periods of time may also result in reliability issues. The upper limit of region B is the AMR. At and beyond the AMR the user should expect problems. Beyond the AMR are two regions of *electrical overstress* with either latent (region C) or immediate (region D) damage as a result of exceeding AMR. Note that the transition between latent damage and immediate damage is subject to normal process variations as illustrated by the yellow S curve. In order to properly evaluate the product reliability and robustness, it is important to understand that some qualification stresses, such as device level ESD and latch-up, are *expected* to run evaluations that will exceed AMR. For example, in the case of latch-up, this may be necessary in order to get significant current injection to assess latch-up robustness.

1.4 New Definition of EOS Incorporating AMR and EIPD (cont'd)

There are different methods a device manufacturer may use to determine AMR values. The manufacturer may pick very conservative AMR values not based on physical properties of the product. This results in a wide region C before the onset of immediate damage. Alternatively, the manufacturer may define the AMR values based on detailed circuit and technology understanding resulting in a more accurate prediction of the damage threshold. This can result in the near elimination of region C. Regardless of the method chosen, the manufacturer is solely responsible for defining the AMR. Further, an AMR is a function of stress duration and any single documented value will have a fixed time association. Consequently, a clear understanding of the AMR by a system manufacturer is necessary to ensure that the operating environment of the system is within the specified conditions and that the limits defined in the AMR are never exceeded. This is particularly important when the system is using the semiconductor device in new or unique configurations. In these special cases, communication between the supplier and system manufacturer *is absolutely necessary*, particularly if the AMR does not appear to cover a mode of operation the system manufacturer expects their system to experience.

Beyond this discussion of regions of operation where the AMR describes maximum electrical and environmental values of operation, there is controversy about whether it should also refer to ESD limits. As noted above, while recognizing that this definition of EOS focuses attention on the AMR, placing greater significance and expectations on its limits than may have been given in the past, each supplier has their own approach to setting the AMR values. With respect to ESD, several different approaches have been observed:

- Some suppliers do not include ESD limits as part of their AMR because testing to establish the ESD limits often does not have similar statistical data collected as is required for setting more traditional items such as voltage.
- Some suppliers do place ESD limits in their AMR definition as it is felt that this is part of the overall agreement that must be met between supplier and customer.
- Other suppliers have placed ESD limits in an AMR section did so for no other reason than it was the only place that it made sense to them.

Regardless of the approach taken, the supplier is *solely* responsible for deciding what parameters and limits are included in their product's AMR. Since this discussion on AMR could be a new interpretation of existing documentation, system manufacturers should be communicating with their suppliers to verify that AMR information for any datasheet published prior to release of this white paper has appropriate meaning and that system manufacturers do not misinterpret the information as having a different meaning than the supplier originally intended.

This white paper also points out that failure analysis engineers are likely to assign, albeit some would say prematurely, the term EOS to any visible damage signature that appears to have been the result of excessive voltage or current. These assignments are often based on experience and may often be correct. However, after initial failure analysis, often times it is unclear as to whether a device has experienced EOS per this white paper's definition until further communication between supplier and customer has been carried out. The damage could be a violation of an AMR caused by incorrect biasing in the application, over voltage, induced latch-up conditions, extreme uncontrolled ESD, misorientation, or something else entirely. The damage may also have been due to a defect in an individual weak device, an improperly set AMR or an intrinsic weakness in the technology. To that extent, this white paper introduces the term "electrically induced physical damage" (EIPD) to represent the term that should be used by FA engineers when no clear communication has been completed with the customer as to possible root causes of the damage. The definition of EIPD is the following:

Damage to an integrated circuit due to electrical/thermal stress beyond the level which the materials could sustain. This would include melting of silicon, fusing of metal interconnects, thermal damage to package material, fusing of bond wires and other damage caused by excess current or voltage.

I.4 New Definition of EOS Incorporating AMR and EIPD (cont'd)

The term EIPD is used when it has not yet been determined if a unit experienced an EOS event by the definition of EOS above and elaborated on in Clause 6. That conclusion can only be determined after the supplier and customer have worked together to arrive at potential root causes.

I.5 EOS Root Causes

As shown in the fishbone diagram of Figure 2, there are many categories and sub-categories for EOS root causes. The three main categories where EOS damage can occur are:

- 1) **powered handling**
- 2) **unpowered handling**
- 3) **switching / alternating current (AC) applications**

Each category can be traced to a specific sub-category shown as branches in the fishbone diagram of Figure 2. The sub-categories of Figure 2 are not meant to be an exhaustive list of root causes but an overview of some of the more common root causes.

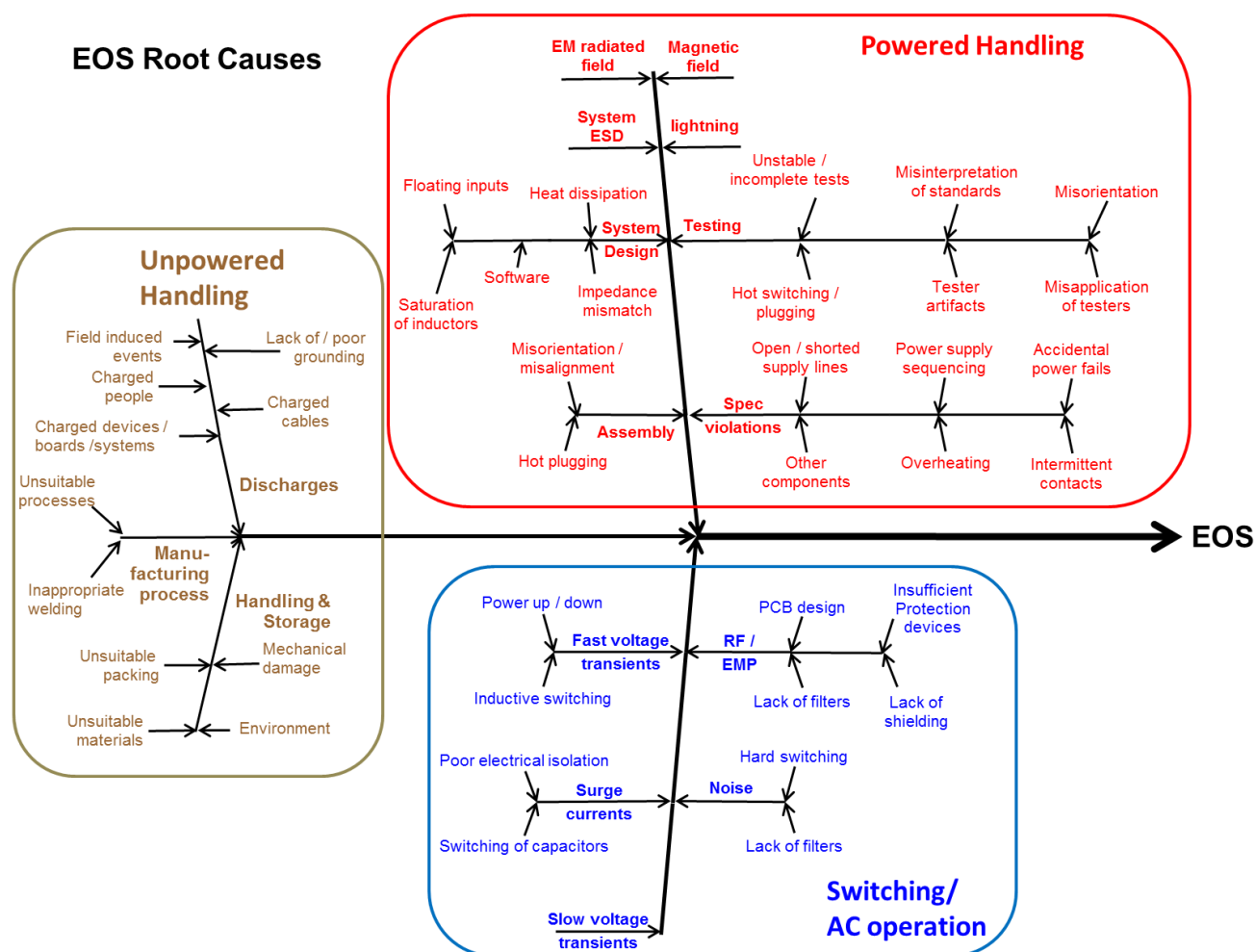


Figure 2 — Fishbone Diagram Representing Different Root Causes Leading to EOS

I.5 EOS Root Causes (cont'd)

Based on the EOS survey, the most common cause of EOS events is powered handling. Events may be related, for example, to overstress-induced phenomena when power is turned on, incorrect power supply sequencing, electromagnetic interference (EMI), or hot plugging. In addition, there are many system ESD events, especially during specification testing, which may result in unintended EOS damage. For responders showing a higher confidence level of finding a root cause of EOS damage (70 % to 100 %), a majority of those responders most often reported root causes which included hot plugging, overshoot / overvoltage, power surge, and misorientation being in their top 3, see Table 1 in Clause 5. Clearly powered handling is an area where more focus is needed to address EOS damage.

In the unpowered branch, possible root causes include: an external charged source discharging into or through the device; the charged device/system being discharged; or the device/system being in an electrostatic field when the discharge has occurred. It should be noted that the root causes in unpowered handling are ESD-like in nature but may not be specifically related to the HBM or CDM testing performed as part of a product qualification. In fact, as the survey responses suggest, ESD represents a very small percentage of what constitutes EOS damage. Many manufacturers spend significant time auditing factories for ESD, thinking this will resolve all EOS events, when in actuality, it will only address a small percentage of EOS related damage. Auditing a factory for EOS involves a much more in-depth look at power delivery systems and connection issues with significant focus on the powered handling root causes shown in Figure 2.

Typical root cause examples in the category of switching / AC operation are radio frequency (RF) coupling, spurious electromagnetic pulses (EMP) or poor PCB design, all of which may result in EOS damage. This category had the lowest reported incidence as root causes of EOS damage but this could be a result of the difficulty in properly assessing the environment for this category.

I.6 EOS Root Cause Diagnostics

When failed products are returned, proper failure analysis (FA) methods become crucial, but the success in determining *root cause* depends on the process flow used in this work. *Communication and cooperation* between customer and supplier *must* happen if the root cause is to be found. One challenge involves determining what can be classified as EOS and what should not be considered as EOS. The analysis itself can be lengthy as failure analysis times can range from days to months. Clause 9 discusses the factors that play a critical role in the analysis time. The analysis can also be complex, involving tools from optical microscopy to acoustic microscopy to assess the component and many other advanced techniques including analysis of the system board characteristics. But this may only identify a *cause*. Coupling the device failure analysis with the product return signature and the use environment is critical to finding the *root cause*. While proper training and the tools available to FA engineers described in this paper are necessary, an FA engineer can only find the *cause* of the device damage (such as the identification of the damage signature and probable polarity / path of transients resulting in the damage), not the root cause of what created the EOS event as shown in Figure 2. Therefore, there must be a cooperative effort between supplier and customer to find the *root cause*. It should be noted that in some cases, such as in a singular damaged unit or if the use environment in which the damage occurred is unknown, it may not be possible to determine root cause.

I.7 EOS Case Studies and IC Designs

There are many EOS damage scenarios that can be avoided if the product field return causes are understood. White Paper 4 discusses these in detail and establishes some important conclusions on A) **Product EOS Returns**, B) **IC Technology / Design Issues**, and C) **Field and Factory Events**.

A) Case studies of product returns with EOS damage signatures were analyzed to determine a root cause. This allowed a reduction of EOS occurrences and demonstrated how appropriate solutions can be identified to meet customer needs. Some important conclusions are:

1. Failure analysis only provides a damage signature and probable path and does not reveal the true root cause.
2. Incorrect testing limits during qualification can lead to failures being falsely identified as EOS.
3. An EOS damage signature could be due to a broad list of root causes including, but not limited to; hot-plugging, ground bounces, supply switching, EMI transient surges, and process / product / system assembly issues.

B) Technology scaling and IC protection designs can also have some impact on EOS returns. A summary of these investigations reveal:

1. Today's advanced process technologies have not shown any obvious increase in return rates for products exhibiting EOS damage when compared to older, more robust technologies [1, 2]. It should be cautioned that further technology advances, with thinner gate dielectrics and novel transistor process technologies, will reduce breakdown voltages and continue to shrink design windows. This reduction in breakdown voltage will reduce AMRs and may subsequently begin to influence returns which exhibit EOS damage. In all cases, it will become even more critical to adhere to the AMR boundaries and maintain clear communication between supplier and customer.
2. As previously established, lowering ESD target levels for compatibility with technology scaling and circuit performance have no impact on EOS return rates.
3. However, IC ESD protection design styles and implementations can have an impact on EOS if careful adherence to AMR values is not addressed. A summary of the design styles and their impacts are summarized in Clause 10.

C) Factory and field return analysis can provide lessons learned as listed below:

1. EOS damage can occur due to poor grounding methods and can easily be mitigated with established guidelines. A risk analysis often can avoid such problems.
2. Learning from field events is important. Many of the problems could be avoided if the supplier and the board designer communicate early in the product application development cycle having knowledge of possible root causes.
3. Automotive applications pose some of the most common risks. For example, hot plugging is a persistent problem in automotive electronics interconnection that can be mitigated by practicing the principle of first-mate-last-break.
4. EOS caused by ESD can be reduced by avoiding charging/discharging in manufacturing lines and implementing a balanced ESD protection approach.

I.8 EOS Mitigation and Communication

An important focus of this white paper is to convey the proper understanding of EOS, fostering communication between supplier and customer and reducing the number of returns exhibiting EOS damage in the industry. Useful customer communication methods are identified based on observed case studies and the expected influences from IC designs, production issues, field events, and application issues. Points to consider include:

- 1) Proper understanding of AMR
- 2) Realistic specifications of AMR and customer realization of its limits
- 3) Accurate determination of the location and possible causes of the damage and finding the true root cause event which created the damage
- 4) Understanding the use application and impacts to the IC's ESD protection design
- 5) Lessons learned from product returns from both manufacturing and the field

These are summarized to help the industry deal with returns exhibiting EOS damage.

I.9 Summary

This is the first known comprehensive document on EOS in electronics manufacturing and operations written to foster understanding of EOS, root cause determination for resolving EOS issues, and implementation of methods for EOS mitigation. A common language on EOS as documented here is the first significant step to help solve and mitigate EOS issues. IC suppliers, customers, applications engineers, and system builders alike should take part in understanding and solving EOS. Finally, customers and suppliers should treat all conditions for applications as a contract and agree that all unspecified conditions are not allowed. Education of these important aspects is the responsibility of all parties involved.

I.10 Outlook

For over four decades, EOS has been one of the top causes of returns for semiconductor devices and systems. The Industry Council has documented here an extensive study which enhances understanding of EOS and recommends many approaches to reduce EOS damage. This should be of great value in preventing EOS from becoming a catastrophic issue in the next generation of technologies involving even more consumer, medical, military, and automotive applications. It would be important to revisit the information presented here at a later date and conduct another industry wide survey to see how much impact this work has made. EOS is inherent in the application of electronic systems. Only through continuous learning and sharing of experiences can future risks be avoided.

UNDERSTANDING ELECTRICAL OVERSTRESS - EOS

(From JEDEC Board Ballot JCB-16-43, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

The scope of this white paper is damage to integrated circuits and systems caused by electrical stress, the terms and definitions associated with electrical stress to these integrated circuits and systems and the mitigation of this electrical stress event as it applies to integrated circuits and systems.

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3 Terms and Definitions

AC	alternating current
A/D	analog/digital
AEC	Automotive Electronics Council
AlCu	Aluminum Copper
AMR	absolute maximum rating
ANSI	American National Standards Institute
ASIC	application specific integrated circuit
ATE	automated test equipment
ATPG	automatic test program generation
BIST	built-in self-test
BJT	bipolar junction transistor
BTI	bias temperature instability
BV _{ii}	injection induced breakdown voltage
CAN	controller area network
CBE	charged board event
CBM	charged board model
CDE	cable discharge event
CDM	charged device model
CMOS	complimentary metal-oxide-semiconductor
CM	contract manufacturer
DC	direct current
DMOS	double-diffused metal-oxide-semiconductor
DSP	digital signal processing/processor
DRAM	dynamic random access memory
DUT	device under test
ECU	electronic control unit
ECL	emitter-coupled logic
EDX	energy dispersive X-ray
EIPD	electrically induced physical damage
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EMP	electromagnetic pulse
EOS	electrical overstress
ES	electrical stress
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association
ESREF	European Symposium on Reliability and Failure Analysis
FA	failure analysis
FAQ	frequently asked question
FEM	finite element model
FFR	failed failure rate
FIB	focused ion beam
FICDM	field induced charged device model
FICBE	field induced charged board event
FIT	failure-in-time
FMLB	first-mate-last-break
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
HBM	human body model

3 Terms and Definitions (cont'd)

HCI	hot carrier injection
HMM	human metal model
HTOL	high temperature operating life
IC	integrated circuit
ICT	in-circuit test
IO	input/output
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IPFA	International Symposium on the Physical and Failure Analysis of Integrated Circuits
IRPS	International Reliability Physics Symposium
ISTFA	International Symposium for Testing and Failure Analysis
ISO	International Organization of Standards
I-V	current/voltage
JEDEC	JEDEC Solid State Technology Association (formerly Joint Electronic Device Engineering Council)
JEITA	Japan Electronics and Information Technology Industries Association
JTAG	joint test action group
LC	inductor capacitor
LCT	liquid crystal thermography
LIN	local interconnect network
LIVA	light-induced voltage alteration
LSM	laser scanning microscopy
LU	latch-up
MCU	microprocessor control unit
MM	machine model
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
NBTI	negative biased temperature instability
NiCr	nickel-chromium
NMOS	N-channel metal-oxide-semiconductor
NPN	negative-positive-negative (transistor)
OBIRCH	optical beam induced resistance change
OEM	original equipment manufacturer
PBL	powered bipolar latching
PCB	printed circuit board
PCBA	printed circuit board assembly
PMOS	P-channel metal-oxide-semiconductor
PNP	positive-negative-positive (transistor)
PPM	parts per million
PQFP	plastic quad flat pack
RC	resistor capacitor network
RF	radio frequency
SCR	semiconductor controlled rectifier; silicon controlled rectifier
SEM	scanning electron microscopy
SMD	surface mount device
SOA	safe operating area
SoC	system-on-chip
STM	standard test method

3 Terms and Definitions (cont'd)

TC	timing circuit
TDDDB	time dependent dielectric breakdown
TDR	time domain reflectometry
TEM	transmission electron microscopy
TIVA	thermally induced voltage alteration
TLP	transmission line pulse
TTL	transistor-transistor logic
TVS	transient voltage suppression
USB	universal serial bus
VDD	positive voltage supply
VFTLP	very fast transmission line pulse
VLSI	very large scale integration
VSS	negative voltage supply
VSWR	voltage standing wave ratio
W-B	Wunsch-Bell
WP	white paper

electromagnetic interference (EMI): Electromagnetic emissions (radiated or conducted) that may cause harmful interference to communications services or other electronic devices.

ESD design window: The ESD protection design space for meeting a specific ESD target level while maintaining the required IO performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced technology node.

second-breakdown trigger current, (I_{t2}): The amount of current at the point in time when a transistor enters its second-breakdown region under ESD pulse conditions and is irreversibly damaged.

4 History of EOS

This is a general introduction to the historical references. In the 19th century, one of the first widespread applications of electro-mechanical systems with a well-known vulnerability to electrical overstress was the telegraph system. During storms, operators purposely ceased operations for fear of direct and indirect lightning strikes which could burn stations, melt wires and equipment and kill operators [3].

With the proliferation of vacuum tube communication equipment in the early 20th century, more complex component and system failure modes presented themselves. With the novelty of electronics in consumer applications, thermal and power supply robustness design issues competed with operator error and user repair problems. This formed the familiar basis for modern overload and overstress phenomenon.

Early radio repair (and kit construction) manuals of the 1920's and 30's included troubleshooting guides for finding melted grids and burned filaments on tubes, as well as procedures for determining failed open or shorted passive components when the hobbyist did not have even a voltmeter for debug.

4 History of EOS (cont'd)

The etymology of the term overstress implies a limit which is exceeded. This is synonymous with the term overload which was more generally used at the time to refer to any functional or permanent deviance from intended operation. Consider the following definitions from the Modern Dictionary of Electronics (1962) [4]:

*OVERLOAD - 1. A load greater than that which an amplifier, other component, or a whole transmission system is designed to carry. It is characterized by waveform distortion or overheating.
2. In electronics, it is that quantity of power from an amplifier or other component or from a whole transmission system which is sufficient to produce unwanted waveform distortion.*

OVERLOAD CAPACITY - The level of current, voltage, or power beyond which a device will be ruined. It is usually higher than the rated load capacity.

OVERLOAD LEVEL - The level at which a system, component, etc., ceases to operate satisfactorily and produces signal distortion, overheating, damage, etc.

At first glance, these would seem to be distinct from EOS, in that they pertain more to temporary functional failures or performance degradations. However, these passages elegantly define the resulting observations which are indicative of having exceeded maximum component limits. If we consider a burned filament in a tube, or a shorted P-N junction in an integrated circuit, we can assume that the device will forever fail to perform with acceptable operational functionality.

Partial damage, such as a semiconductor with leakage, might be detected by signal distortion of a reference test pulse or level, overheating under normal loads, or visible physical damage. Thus the concept of permanent damage due to EOS can be found in the early definitions of overload which may or may not have created permanent damage, depending on the performance requirements.

Absolute maximum ratings (AMR) first appeared routinely in solid state datasheets in the late 1960's and early 70's. These limits are due to the unique process technologies of early emitter-coupled logic (ECL), transistor-transistor logic (TTL), and N-channel metal-oxide-semiconductor (NMOS) which alerted the designers to power supply and interface level limits at a time when signaling voltages and polarities were not strictly defined and constrained by unique interface designs (such as RS-232, IEEE-488, etc.)

Generally, while input signals could cause problems in some circuitry, AMR's tended to convey a guarantee by the component supplier that if the thermal and voltage envelope limits were not exceeded, the component would never be permanently damaged or degraded and would remain completely within all other electrical performance specifications.

Exceeding the AMR for any period of time did not guarantee permanent damage, and indeed the ratings were often very conservative or "sandbagged" with wide guard bands because it was often difficult for designers to accurately gauge the robustness limits of a new technology.

4.1 Outline of History of Relevant Professional Societies

This historical note by Colvin [5] covers the origin of many EOS related professional societies:

"Published papers for Failure Analysis date back to 1954 for the Annual Symposium on Reliability and back to 1963 for the International Reliability Physics Symposium (IRPS). Another familiar resource to the failure analyst in the USA is the Symposium for Testing and Failure Analysis (ISTFA). ISTFA proceedings were originally known as ATFA (Advanced Techniques in Failure Analysis) and date back to 1974. The Microelectronic Failure Analysis Desk Reference (1996-2012) is an important companion to the ISTFA Workshops. IPFA (International Symposium on the Physical and Failure Analysis of Integrated Circuits) is another resource of information. The conference for IPFA has been held annually in Singapore for the last 6 years (*ED NOTE: since 1987*). ESREF is a European forum for reliability of electron devices, failure physics and analysis. ESREF held its first symposium in 1990. The annual EOS/ESD Symposium started in 1979 in the US. One of the goals being to elevate the awareness to the destructive nature of EOS and ESD to electronic components. Additional resources of information are the Journal of Electrostatics, an Elsevier publication, ESA (Electrostatics Society of America), and IEJ (Institute of Electrostatics Japan)".

4.2 EOS – A Brief History

Two of the earliest researchers were Wunsch-Bell [6], who did not mention EOS by name but whose physical modeling implied a path to melting at high temperatures for semiconductor components. The time dependent Wunsch-Bell equation generally defined as $P/A = f(t^x)$ also shows that the power per unit junction area varies with pulse width, and is actually a thermal diffusion equation which depends on thermal conductivity and the product of density and specific heat. This model characterizes a component's failure power threshold versus an input pulse duration (time dependent pulse width). A plot of the device behavior shows 3 regions: a short pulse width ($<0.1 \mu s$) ESD region, a longer pulse width ($0.01 - 20 \mu s$) Wunsch-Bell region, and a very long pulse width ($> 20 \mu s$) flat region. This is the region which leads to melting, because the thermal conductivity and the density-specific heat product are both temperature dependent properties of the semiconductor material, and so this flat pulse width region is directly related to EOS type failures, as a result of high heating with time in addition to pulse width.

Additionally, some early mentions of the word overstress appears to be in 1971 [7], when Smith and Shumka were analyzing complimentary metal-oxide-semiconductor (CMOS) microcircuits and silicon devices. They reported that up to 29 % failed due to external overstress; unfortunately a detailed FA of these failures was not included. In 1979 [8], Rutherford and several others reported on the electrical overstress of digital bipolar microcircuits and silicon devices claiming that 60-75 % were EOS damage. Some used charged capacitors (up to $0.01 \mu F$) as the input stress. Lee [9] attempted to interpret the EOS damage in power transistors and semiconductors. Melted bond wires, fused or alloyed metallization all fell under the category of EOS damage.

From 1983 to 1985, several authors, Lee [10], Middendorf [11], and May [12] reported the EOS damage from power circuits to power transistors. They used the terms *melted metal*, *dissolved metal*, *melt-through* and *burnt metal* in their description for EOS damage, but there was no mention of the bond wires. The use of the combined terms EOS/ESD is significant, where the combined term is used to mean EOS and/or ESD, i.e., EOS alone, ESD alone or both if the diagnosis is uncertain. However, the authors pointed out that the use of the shorter duration pulse distinguished between the ESD damage and the longer pulse EOS damage, in most cases.

4.2 EOS – A Brief History (cont'd)

In 1988 [13], Lee conducted simulation and characterization of EOS damage in metal-oxide-semiconductor field effect transistor (MOSFET) transistors and ICs by capacitive discharge. Here, Lee used much larger capacitors (200 μF to 4500 μF) to dump more energy into the device. Lee reported that the large metal melt-through also obliterated the ESD protection circuits. The wire bonds were also damaged. Using the lower capacitance (up to 200 pF) resulted instead in ESD damage between the source and drain in the ESD circuits. Hence, differentiating between EOS and ESD damage was of primary importance early on.

In 1989, Richardson Jr. [14] described an overvoltage stress test in TTL electronics, which resulted in melted metal, open metallization, melted input transistors, and damaged input protection diodes. A curve tracer was used as the voltage simulator, and all voltages were greater than the rated maximum voltages for the TTLs. The failures were referred to as electrical damage. The same year, Kiefer [15] studied the damage in high-speed CMOS gate arrays using the machine model (MM) as the simulator (in order to produce more power) and referring to the process as an EOS stress. This resulted in the usual fused/melted metal, all damage being visible with a low magnification microscope. At lower machine model (MM) voltages, the damage was not immediately visible, but on removal of topside glass/oxide and the metal below, the damage could be seen in the oxide below the drain-to-source contacts. These were referred to as ESD melt filaments failures. These authors simulated an EOS stress after first ESD stressing the devices. They called this an “ESD/EOS” stress, meaning ESD stress followed by an EOS stress. The damage seen was fused metal plus protrusions of polysilicon melt filaments in the contacts, and also between the contacts. These authors were attempting to show the difference between EOS damage and ESD damage.

Also in 1989, two authors (Willis [16] and Kitamura [17]) discussed locating EOS/ESD failures without explaining why they used the combined terms (EOS/ESD). They reported the following long list of failures: damaged/degraded junctions, blown open and punched through contacts, ruptured dielectrics, gate oxide pin holes, gate edge pinholes, aluminum melting, fused open aluminum metal, thermal damage of diffusion resistors, and melted silicon. They only used two electrical stress types, HBM and transmission line pulse (TLP), and labeled some figures EOS, and some ESD, with no clear discussion or clarification as to which failure belongs to the two different stresses.

Launer [18] related discoloration to EOS damage in 1990 when he presented EOS damage data after electrically overstressing passivated nickel-chromium (NiCr) resistors using two different pulse sources (a HBM 150 ns pulse width and a 200 ns to 120 μs square pulse). He referred to HBM as an alternating current (AC) source of adiabatic EOS, resulting in discolored NiCr resistors because there was no significant heat beyond the oxide. He referred to the square pulse as a direct current (DC) source with its long pulse width, which also caused EOS damage (including the discoloration) in the NiCr resistors. No explanation was given in the report as to why these two different events resulted in the same EOS type damage.

May, [19] in the same year (1990), presented and discussed the EOS discoloration concept, but applied it to the metallization using pulse widths of 10 μs , 120 μs , through to DC. The author concluded that the lateral thermal diffusivity occurs in the metallization, and therefore across the whole device.

Between 1991 and 1994, several authors, Wilson [20], Schani [21], Glacet [22], and Henry [23] demonstrated that EOS damage could be produced from either negative/positive step stress pulses, overvoltage/overcurrent stressing, from IC life test, and IC burn-in attributing one mechanism to the process-induced metal stress relief during the IC life test and/or burn-in test. This EOS simulation allowed the authors to speculate as to how to differentiate between EOS and ESD type damage. Then, in 1998, Henry and Mazur [24] in their paper “Basic Physics in Color-Coded EOS Failures” were able to do just that by applying some physics principles to the process. The visible EOS damage was the same as that seen by earlier authors: die surface burnt, fused metal, etc.

4.2 EOS – A Brief History (cont'd)

Most of the previously mentioned authors reported that EOS damage was optically visible at very low magnification - open metallization, fused metal, burnt/discolored metal, melted metal, fused open metal, package distortion/blistering, and melted sockets (on the board). One author used the non-destructive acoustic microscopy method to externally view the EOS damage inside the package. The package compound was shown to be thermally degraded. It showed internal delamination (die interface-die attach), voids, the aluminum wires were fused or burnt and had molding compound on them, die cracks, burnt/carbonized plastic, and package cracks under the die pad. They also reported the electrical signatures as shorts, opens, high leakage, and high resistance.

In 1995, Lisenker [25], working on a CMOS very large scale integration (VLSI) product, used the combined term ESD/EOS to mean ESD stress, followed by EOS stress to simulate the observed failures. He suggested that the metal burn-out occurred after the gate oxide punch-through (or juncture failure) occurred, creating a short which drew enough current in a powered device to melt the metal stripe. Hence the use of the combined term ESD/EOS. He used burn-in, a process of operating the device under certain electrical and thermal stress conditions which accelerates the life of the device and removes poor quality devices. Several other authors in the same year [26], 1995, showed EOS damage in insulated-gate bipolar transistor modules (each module contained several devices). The damage included burnt wires, melted wires, melting pits in bond pads, and melted material penetrated deep in the silicon chip. They used a square pulse frequency test (high voltage 50 Hz -12 kHz cycles 600 V-1300 V) through a charging capacitor and inductor.

In 1997, Milburn & Parekh [27] reported that the EOS damage (melted/open metal) was precipitated by excessive voltage or power generating a high current over a period of time, and in 1998 Vinson [28] studied the aluminum interconnect response to EOS, calling EOS the stress, instead of the failure, and reporting that EOS is the event causing the failure, and the aluminum film responded to the EOS event. They concluded that Joule heating caused failure as a result of excessive currents due to overvoltage from a power surge, inductive kickback from an inductive load, or application of a voltage to an output pin in the nanosecond to second range. They provided the following definition of EOS: “a class of failure from an applied stimulus condition exceeding the normal operation of the circuit”. Yet some authors referred to the failure as aluminum EOS, or EOS damage or EOS of aluminum lines—all interchangeably.

In 2001, Wang [29] described EOS damage as a result of over-current or over-voltage events ranging from microseconds to milliseconds. The author reported that EOS causes uncontrollable overheating (thermally induced failures) which leads to electromigration failure, intermetallic compound formation, and delamination on die surface. Vinson [30] also saw EOS damage, but the cause of the EOS was an excessive electrical stimulus (V or I) applied to the unit resulting in the damage. EOS then is an event that occurs at a point in time, triggering the failure. It is not a wearout mechanism that degrades with time, but the failure is quite visible, and in some cases the metal from the contact migrates into the silicon shorting out the junction (damaged junction).

In 2003, Korchnoy [31] showed that the silicon substrate and diffusion layers can be affected by ESD in such a way that the damage extends up through the interlayer dielectric to the metallization causing it to melt both at the contacts and the metallization because of the excessive current flow. He called these ESD/EOS failures, i.e., ESD induced EOS damage.

4.3 Transition to Present

In the period between the earliest, most elementary electrical circuitry overloads and the more recent academic and industrial analysis, the body of knowledge, terms and definitions have grown dramatically. EOS damage has been categorized by early researchers based on the physical results to try to determine the type of event, energy content, and duration of the event to help identify the source. Papers defining a method to characterize devices for EOS robustness were not always present. Also, most did not include physical modeling of EOS in the semiconductor devices, but there were some papers which attempted to describe how to improve the safe operating area (SOA) of transistors, SOA refers to the maximum voltage and current that a transistor can sustain without damage under specific conditions.

While the mechanisms may be related or even identical, often the definitions and terms used coherently within the scope of one paper or author may be confusing or even conflicting when compared to other sources. As Alfred Korzybski observed, it is important in any semantic system to index and date the terms used whenever the same word may be mapped by different authors and readers to different meanings at different times. The underlying physics of the phenomena may remain timeless and universal, but the labeling and classification may have been inconsistent.

The balance of this document investigates these issues in more detail and tries to add clarity to the use of the terms and definitions, aided with the benefit of the historical literature amassed so far.

For Further Historical Reading

While not explicitly referenced, references [32-106] have been included by the authors of this clause as historically significant, relevant and instructive milestones in the evolution and advancement of the definition, characterization and analysis of electrical overstress.

5 EOS Damage in the Factory and Field

This clause will first summarize the motivation for the EOS field returns analysis, conditions that could cause EOS damage in the factory and the field, how a determination of EOS can be made, and how these failures exhibiting EOS damage from EOS or other non-ESD root causes can be distinguished from EOS damage resulting from ESD events. Ways by which transients can couple into a system causing EOS damage is discussed in 5.2. The development and description of the industry EOS survey is given in 5.3. The results, both in graphical form and summary, of the different questions followed by notable comments from companies on their experiences with EOS damage, both within their company and with their customers, are described in 5.4. This will lead to a summary of the impact of EOS damage, both in terms of time and economics, to the electronics industry. The full EOS Survey that was sent out appears in Annex A.

5.1 Motivation for Field Returns Analysis of Failures Exhibiting EOS Damage

EOS is consistently one of the “high bars” on product failure Pareto charts in the electronics industry. EOS occurrences can be expensive to the entire supply chain (OEM, system supplier, module supplier, and IC supplier) in terms of time to resolve and opportunity cost. In most high reliability applications, if the failing devices in the board or product can be accessed, the devices are returned to the supplier and supplier resources are used to diagnose the failure and determine root causes of failure. Depending on the number of systems or devices returned the potential exists to affect long term reliability of an entire program unless the root cause(s) of the failure mechanism is found and an effective fix / solution is found and implemented. Delays in end product cycle time and mass production of systems often results.

As IC technologies scale and voltages decrease, and systems become more complex, the amount of energy transfer into systems necessary to produce EOS has been decreasing, and the damage can involve a larger area of the device.

5.1.1 Examples of Damage Resulting From Different Root Cause Mechanisms

Various root causes of EOS damage give rise to many different damage characteristics in ICs. Clauses 7, 8 and 9 present more information on this through various literature and case studies. Signatures associated with mishandling, signal / supply overshoots or misapplication often can involve package and IC material damage, and are more extensive in a product than failure signatures resulting from events in the measurable ESD regimes. High power transients from these root cause events can involve damage including metal burnout and significant electromigration (often in several locations), heating to the point of carbonized material on the surface of die, blown open bond wires, package melting, delamination, reflowed metal supply or ground buses, and blown holes in silicon / contact or substrate regions. Often the EOS damage signatures can be seen optically. There can be several regions of damage, involving several different failure mechanisms. Field induced events, charged person discharges or charged devices resulting in a discharge into or through a component (as a result of unpowered handling) often result in more localized damage areas involving less area and specific material changes (pinholes in one or more transistor gate oxides of a device, or junction damage in one or more devices in a current path).

5.1.2 What Information is Expected from these "Returns Exhibiting EOS Damage?"

Root cause diagnosis of EOS damage requires knowledge of the application at the time of the damage. This involves the following:

- where in the application or system the damage occurred
- environmental conditions at the time of the damage or during the test which revealed the damage, in terms of automotive, this would include the environment within the particular location of the car
- schematic / layout of board devices in the application
- details of the supply, ground and input/output (IO) connections and voltages at the time of damage
- details on the interconnection of devices on the board which could provide paths for the electrical stress
- any possible "precursors" to damage (on the supplier side, determination of IC process, IC assembly yield, test issues, or results of device analysis indicating a weakness; on the system manufacturer side, tester programming / hardware, or connection related issues in the application)

5.1.3 What is the Realistic Percentage of Devices that Customers do Return?

Many customers using products in non-high reliability applications would only provide a single return exhibiting EOS damage as a representative example and they may not report a rate of damage. The undisclosed devices would then be a hidden cost (customer would just buy a new one, or supplier would just supply a new device). However, customers supplying high reliability systems (such as automotive, non-space aerospace, pacemaker manufacturers, medical products) return every damaged device and expect failure analysis with results and root cause determination from an investigation on every single device, involving teams of design / product / FA from customer and supplier. So overall there is no "consistent" percentage across the electronics industry.

5.2 Transients

There are many ways a transient can enter into a system. Some may be from a directly applied source including, but not limited to:

- overvoltage spikes on supplies
- charging / discharging of large value capacitors directly into system pins
- long charged cables connecting directly into system pins
- a system being supplied with power before its connection to ground (connection of a board into a system plug contacts supply pins before ground pins)

Other more indirect ways could involve:

- Process induced – Such as those in assembly or IC misprocessing resulting in low breakdown, direct shorting, or unintended high current density path from device die to IC pin.
- Charged board – Sudden discharging of a charged board to a ground potential can result in discharge paths through the board's supply and ground tracks which directly route to or through components causing excessive current densities and component damage.
- Test induced – Excessive voltage transients resulting from incorrect power supply switching or incompatible switch control voltages, glitches on supplies, program induced misbiasing of supplies, incoming testing using charged multimeters.
- Coupling of external radiated energy into unprotected devices of a system – This can occur in those applications which generate or are in the range of this type of energy and which can also cause high voltages / currents that cause damage in systems and components.

5.2 Transients (cont'd)

Components and systems which have been compromised by insufficient ESD control may be prone to EOS damage upon application of a direct or indirect energy transfer as above.

These stimuli can immediately (or later during operation) produce damage signatures typical of EOS damage to components, including large area damage to the IC die, metal burnout, carbonized molding compound (for packaged components), wirebond thermal fusing/opens, etc. The thermal energy can spread to induce damage on the board itself and to other components of a board or system.

5.3 EOS Survey for Gathering Data on EOS Damage

5.3.1 Survey Form and Description - How was the Survey Conducted?

The Industry Council created an EOS survey for the purpose of collecting data from a broad set of people within the electronics industry. A list of electronics industry companies and associations, as well as institutions and conferences, etc. was identified and an email was sent to contacts (at their company address) within these associations. The contacts were invited to submit the EOS survey themselves for the company or forward the survey to the correct point of contact in their company for submittal. The survey was placed on the Industry Council web site so that people could request online to participate. To reach critical Asian companies, the survey was also translated into Chinese, Japanese and Korean. To access the survey, respondents gave their email address (similar to what AEC does), then they were allowed to download the survey (a PDF file allowing user entry). To ensure simple and anonymous feedback, no company specific or email address information was part of the collected survey data. The survey results (the returned pdf files) were extracted automatically and formatted into a .csv report file. For the checkbox or single item entries, charts with question titles were derived showing pictorial results that are summarized in 5.3.2. Additionally, questions requiring comments as answers were asked and the anonymous comments were collected. The EOS Survey is included in Annex A.

NOTE At the time the survey was done, many references to EOS were made in terms of “EOS failure”. The figures in 5.3.2 and subsequent comments, as well as the Survey itself in Annex A, keeps these references. But it must be clarified that the failed devices should not be referred to as “EOS failures” but rather “failures exhibiting EOS damage”. Root causes of EOS can come from many sources, and devices and systems are not designed to be immune to EOS. This distinction is maintained throughout the rest of WP4. It is expanded in Clause 7 and in the case studies of Clause 8.

5.3.2 EOS Survey Results

The remainder of this clause discusses results of the EOS survey. Results from single selection questions will be presented in graphical form followed by discussion of the results. The end of this section will feature notable written response answers to questions asking for comment response.

5.3.2.1 Demographics of Companies Reporting EOS Data

Eighty-one responses to the EOS survey were received from October 2012 to May 2013. Three questions were asked regarding company demographics. Figure 3 shows the market segments in which each company operates.

NOTE Respondents were allowed to select multiple segments, if applicable.

5.3.2.1 Demographics of Companies Reporting EOS Data (cont'd)

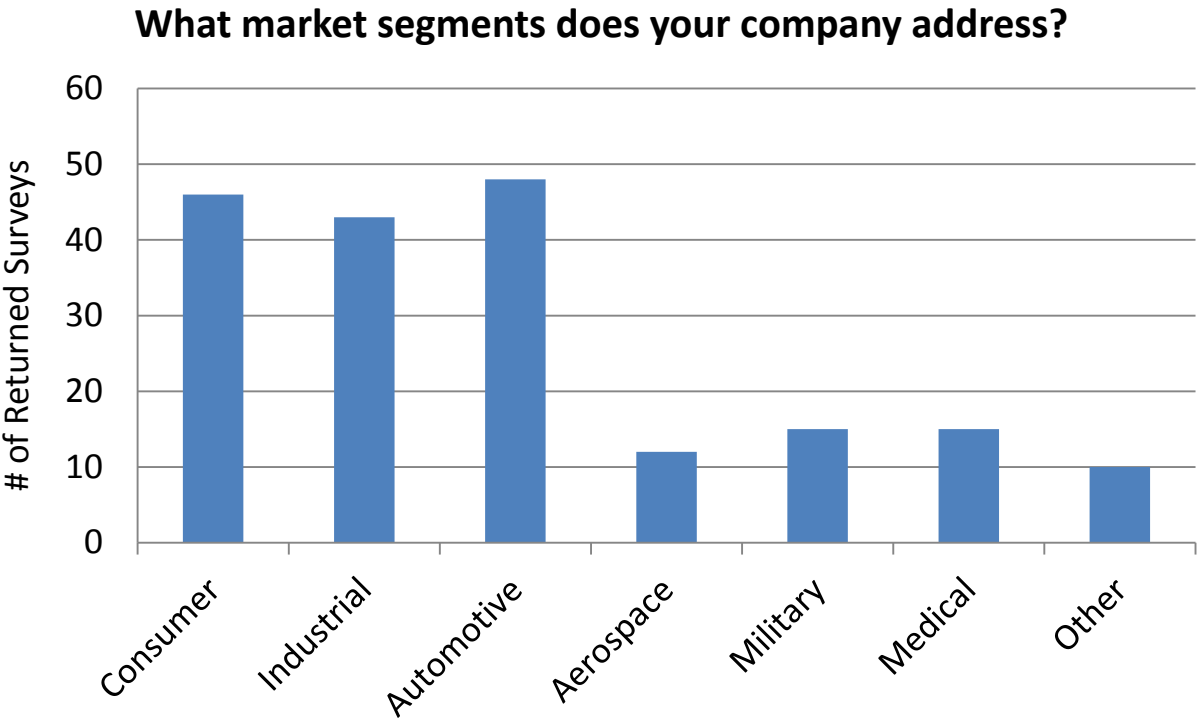


Figure 3 — EOS Survey Question 1a

The majority of respondents serve the consumer, industrial and automotive markets with each returning over 40 responses. The aerospace, military and medical markets were also well represented, but with about a third as many responses as the prior groups.

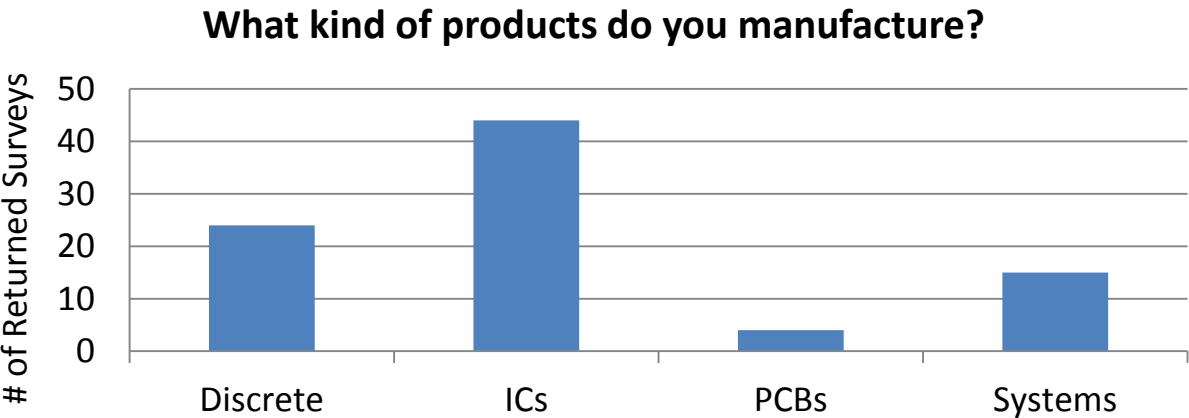


Figure 4 — EOS Survey Question 1b

Figure 4 illustrates that most of the respondents work for companies which sell discrete components or integrated circuits. Printed circuit board manufacturers were least represented, with only 4 responses. However 15 final system manufacturers (OEMs) participated in the survey.

5.3.2.1 Demographics of Companies Reporting EOS Data (cont'd)

How many electronic devices do you ship / assemble per year?

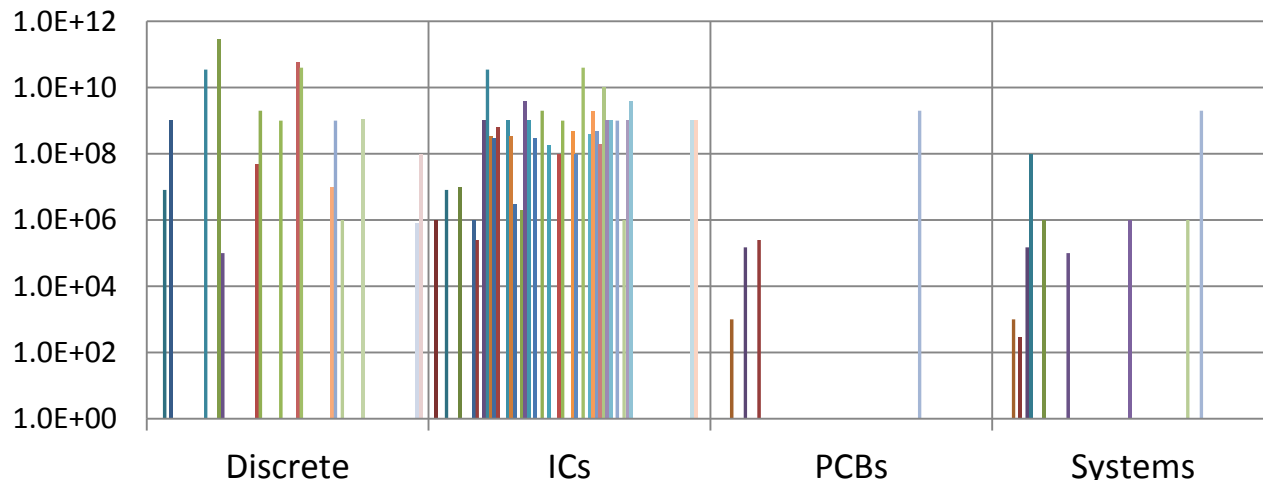


Figure 5 — EOS Survey Question 1c

The final demographics related question referred to the number of electronic devices each company assembled and shipped per year. You can see in Figure 5 that the “number of units shipped” responses varied from a few hundred to several billion across the discrete, IC, PCB and system space. Clearly the majority of the companies ship large volumes of product.

5.3.2.2 Industry Data on EOS Classification

How do you classify a failure as "EOS"?

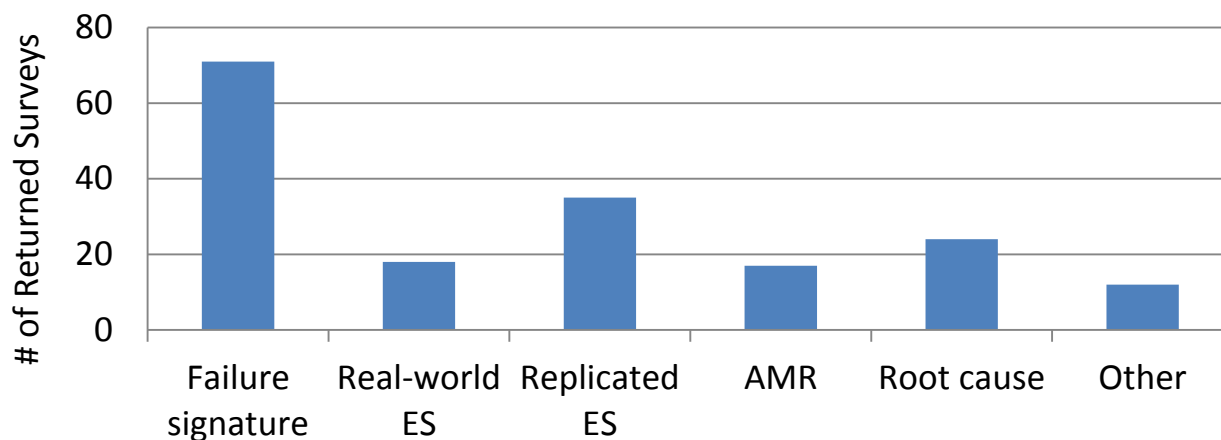


Figure 6 — EOS Survey Question 2a

Figure 6 shows 71 of 81 respondents classify EOS based on a failure signature (exhibiting EOS damage), indicating obvious severe damage as a key criteria of failure. Additionally, 35 of 81 respondents determine if they can replicate the damage with an electrical stress as a criteria for classifying as EOS

NOTE ES in the above graph is electrical stress.

5.3.2.2 Industry Data on EOS Classification (cont'd)

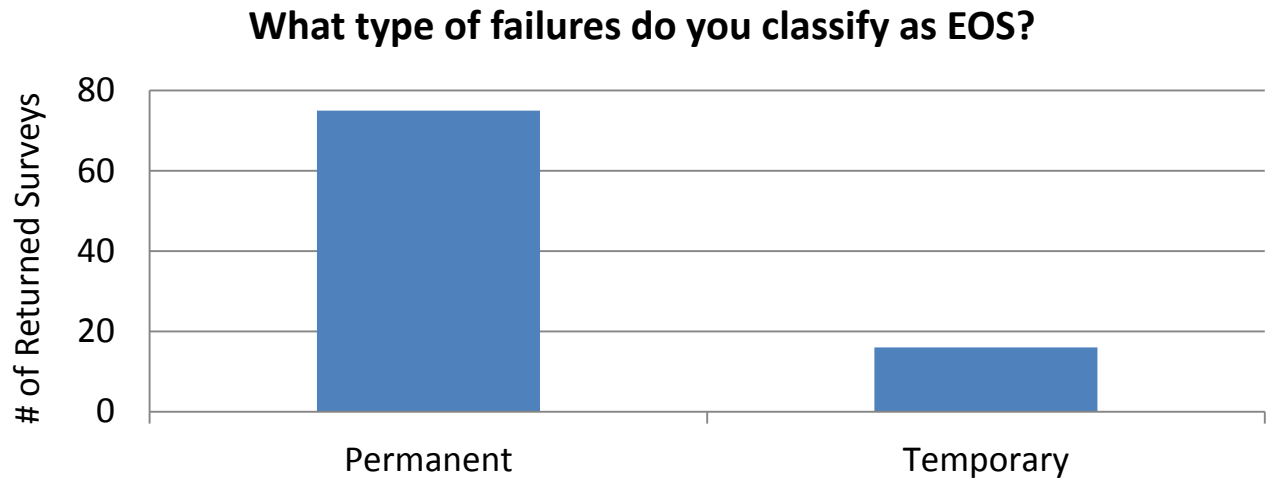


Figure 7 — EOS Survey Question 2b

Figure 7 shows 75 of 81 respondents would classify permanent damage as EOS damage. Only 16 of 81 would also classify non-permanent (intermittent or resettable) as an EOS damage mode.

5.3.2.3 Failure Rates, Main Causes, and Origin of Failures

The following graphs show reported EOS failure rates (as percentages of both total and electrical failures), reported causes of failures, and at what stage of the product life the failures occurred.

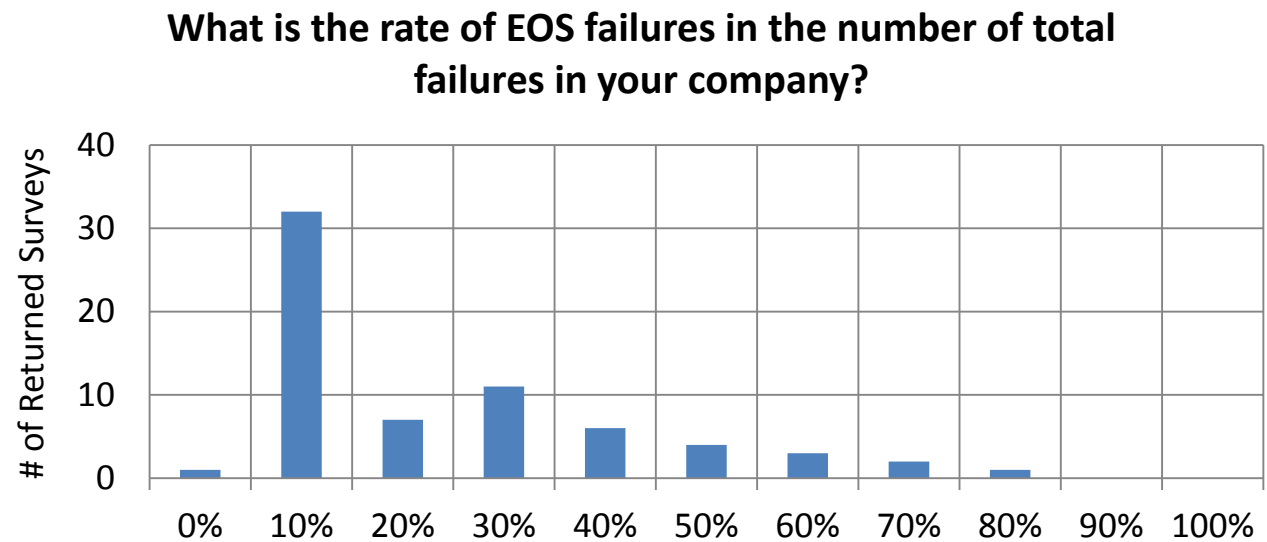


Figure 8 — EOS Survey Question 3a

Figure 8 shows nearly every respondent reported a non-zero EOS failure rate (in terms of percentage of total failures). The average percentage of EOS failures out of total failures was about 25%. One respondent reported a zero percent rate; nine reported EOS failures as being equal to or greater than 50% of their total failures.

5.3.2.3 Failure Rates, Main Causes, and Origin of Failures

What is the rate of EOS in the number of electrical failures in your company?

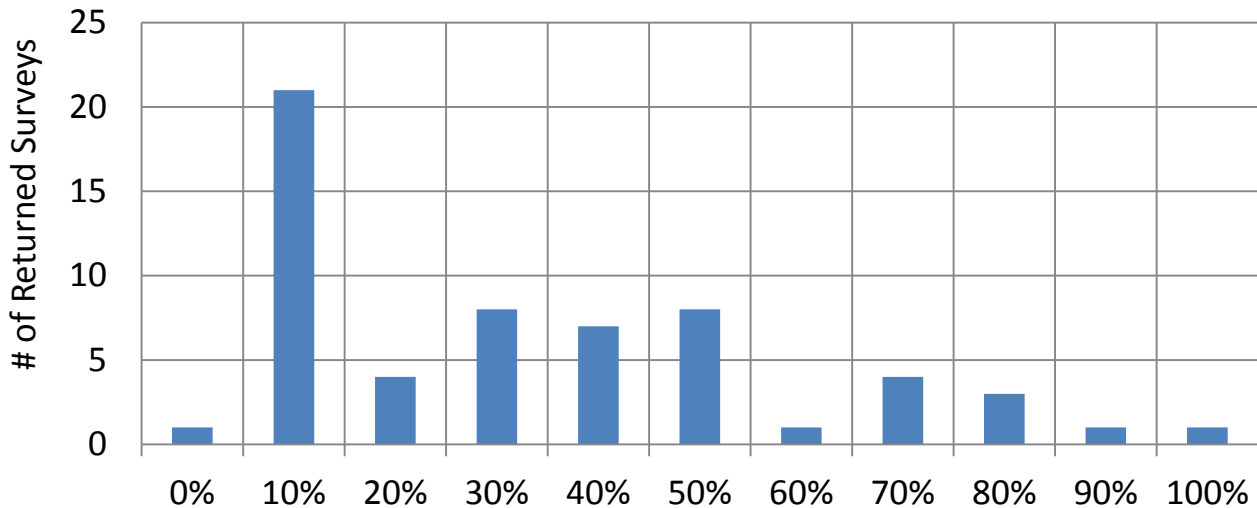


Figure 9 — EOS Survey Question 3b

Figure 9 shows nearly all respondents reported a non-zero percentage of EOS returns as related to the total percentage of electrical failures (looking at total electrical failures removes the “no trouble found” category). The average percentage of EOS returns out of total electrical failures was about 30%. Only one respondent reported a zero percent rate; 17 of 81 respondents reported EOS returns as being equal to or greater than 50% of their total electrical failures.

It should be noted that for respondents reporting greater than 20% of total failures being EOS-related or 30% of total electrical failures being EOS-related, this would make EOS the largest bar on the Pareto chart of that responder’s known causes of returns.

5.3.2.3 Failure Rates, Main Causes, and Origin of Failures

How does your company categorize the aforementioned cause of EOS failures?

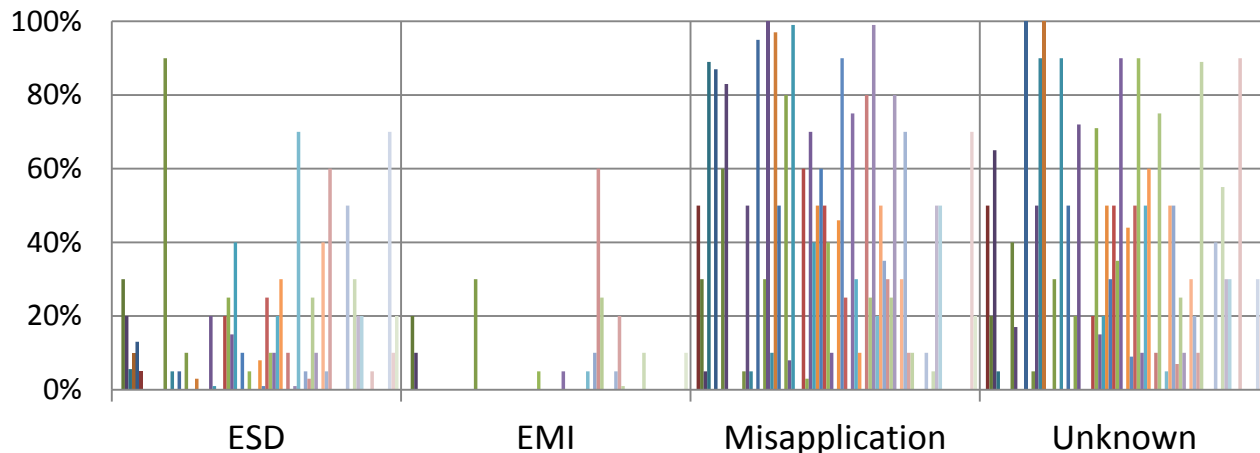


Figure 10 — EOS Survey Question 3c

Figure 10 shows a distribution for the four main reported causes of EOS damage as described in the fishbone included in the survey. Within each graph response category, the composite from all 81 companies are shown. In other words, the survey limited the response options to the 4 categories of ESD, EMI, Misapplication, and Unknown. The Y-axis shows the percentage out of 100% for each category with the sum of all 4 categories always equal to 100%. The same colored bar in each category represents one company's response percentage for that category. This visual format shows collectively how widespread each main cause is in the industry.

The most widely reported cause of EOS damage was misapplication. Misapplication failures include hot plugging (plugging into a powered socket; this had the most respondents, 21 of 81), unintended overvoltage on supplies occurring during testing, component misinsertion or misalignment, etc. There was a wide distribution of reported misapplication percentages, from 0 to nearly 100%.

The second highest reported percentage cause was “Unknown”, having almost as high a reported occurrence rate as misapplication. These returns could not be, or were not, traced to a root cause. There was a wide distribution of total percentages in the unknown cause category, similar to misapplication.

The third highest reported percentage cause of EOS damage was some form of ESD (charged board or charged cable events, system level events, charged devices discharging, incomplete or nonexistent ESD controls, etc.). Of the companies reporting ESD as a cause, the most common percentage of EOS damage being due to ESD was in the 10-19% range with a close second group of respondents reporting a percentage of 20-29% due to ESD.

The lowest reported percentage cause of EOS damage was EMI (which includes coupling and external non-contact events) which was reported by only 14 of 81 respondents, and the percentage incidence of reported EMI was lower than that of the other three groups, an average of 5%. Only 5 of 81 companies reported 20% or more failures due to EMI, with one respondent reporting a 60% failure rate. It is possible the low percentage reported for EMI is due to the difficulty in getting to a root cause for this category.

5.3.2.3 Failure Rates, Main Causes, and Origin of Failures (cont'd)

Where do EOS failures experienced by your company typically occur?

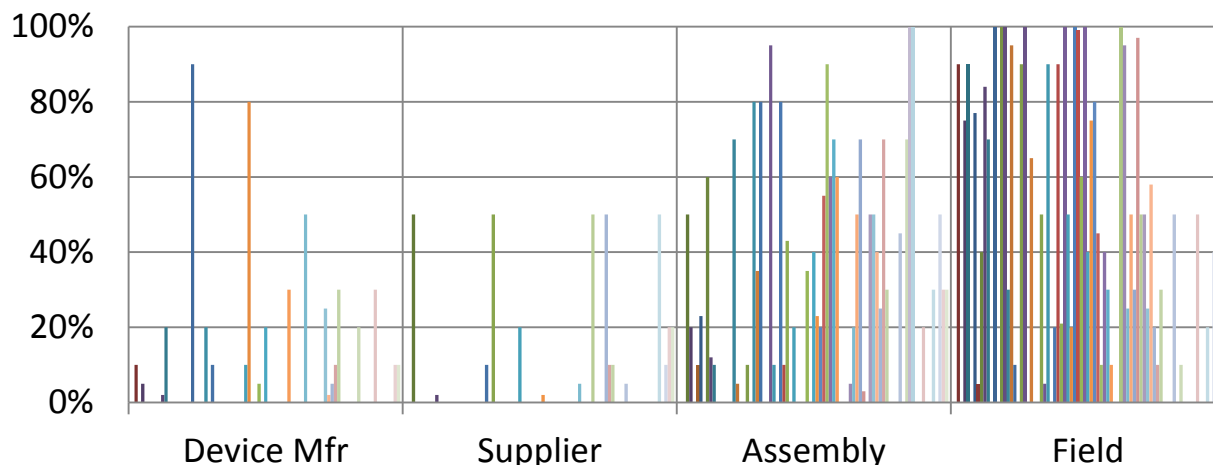


Figure 11 — EOS Survey Question 3d

Figure 11 shows the collective company response identifying where failures exhibiting EOS damage occurred in the electronic/system supply chain. Locations were divided into four categories: Device Manufacturer, Supplier, Assembly and Field. It should be noted that some overlap was expected, as respondents in one category could be in a category "earlier in the product cycle" with respondents in a later stage in the product cycle unlikely to classify failures in an earlier category.

The most common reported origin of EOS damage was "Field", with an average percentage of over 40%. There was a wide distribution in the percentages respondents gave with an origin of "in the field" (Figure 11 Field column).

The second highest reported origin of EOS damage was assembly-related. Most companies reported some percentage related to "Assembly" as an origin of EOS damage. Indicating "Assembly" as an origin of damage was somewhat lower than "Field" at an average of 30%. This category showed a wide distribution, ranging from less than 5 % to 100 %, with 13 of 81 companies reporting 60% or more of their failures occurring in assembly.

From these above two categories, when taking into account the reported location of where the EOS damage occurred, it is observed that misapplication in assembly or field resulting in EOS damage represents by far the largest reported location / root cause combination.

In the second lowest reported percentage category, 22 of 81 reported "Device Manufacturer" as the origin of EOS damage. The average percentage in this category was around 20%. 6 of 81 reported 30% or higher percentages (the greatest was 80%), while most others reported 20% or less.

In the lowest reported category, 14 of 81 respondents reported "Supplier" as the origin of EOS damage. Of these reports, the average percentage in this category was under 20% with greater than half reporting 10% and 5 of 81 reporting 50%. It should be noted that "Supplier" could have a different meaning depending on the reporting company's position in the manufacturing chain. For example, a device manufacturer's "Supplier" may be a contractor testing or assembly facility. An OEM's "Supplier" may also be reported as a "Device Manufacturer". This may account for the low reported "Supplier" location percentage.

5.3.2.4 Other Reported Causes of EOS

One outcome of the survey was that a number of respondents indicated EOS causes which did not fit well into the “fishbone” categorization of failures in the EOS survey. These reported causes included:

- oscillation
- linear mode
- shoot through
- vendor quality
- welding (soldering)
- electrostatic coating
- outsourced processes
- fails at card lamination (customer)
- connection to neighboring device
- weakness in PCB design

5.3.2.5 Diagnosis, Importance of EOS Reduction, and Failure Reports

What is the confidence level in your root cause of EOS diagnosis?

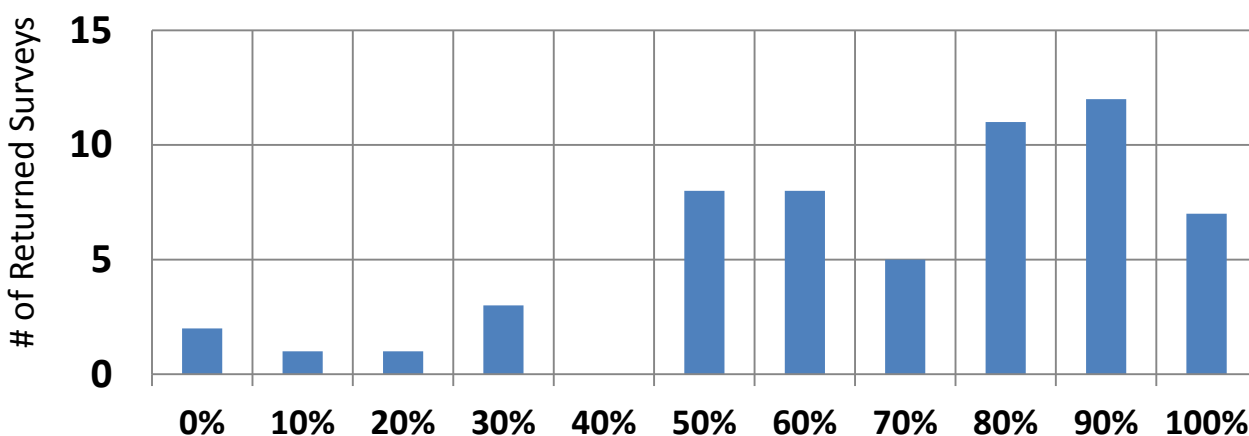


Figure 12 — EOS Survey Question 3f

Figure 12 assesses respondent confidence in determining root causes of EOS damage. A majority of respondents were confident that EOS damage could be correctly diagnosed and attributed to a root cause. Of the majority reporting 50% or higher confidence, the average is 80%. In review of responders showing a higher confidence level (70 % – 100 %), a majority of those responders also reported root causes most often which included hot plugging, overshoot / overvoltage / power surge, and misorientation. Table 1 summarizes the top 3 root causes from those companies with a confidence level of 70% or higher.

NOTE Not all companies gave details on the top root causes found.

5.3.2.5 Diagnosis, Importance of EOS Reduction, and Failure Reports (cont'd)

Table 1 — Top Root Causes for High Confidence Responders

Confidence in Diagnosing Root Cause (Percent)	Company Identifier	Root cause 1	Root cause 2	Root cause 3
100	6	Hot Plugging	Power Surge	Test Software
100	15	ESD; but very rare		
100	53	Assembly/Handling	Mis-Insertion	Power Supply (sequencing, spike, ...)
100	59	Hot Plugging	Ungrounded Equipment	Wrong polarity
100	61	Wrong parameters at testers (voltage or current is too high)	Hot plugging	
100	80	Burnt Features	Disconnect Bonding Wire	Specific Device Damage
90	12	Single Event Latch up	Transient Latch Up due to internal component noise	Poor documentation from supplier.
90	28	Fails at card lamination (done by customers) - exact root cause/model unknown!	Missing ESD protection equipment at customer assembly	
90	43	Overstress at supply pins	Overstress at the external buses, like I2C	Caused by connected neighboring devices
90	56	Unconsidered or hidden inductivities in circuitry design w/o protection for critical devices	EMI due to long cables between components or neighbored high power circuitry	missing derating combined with/ or "sportive" device specifications
90	62	ESD	EMI	
80	11	Hot plugging	System level design	component (date codes, process changes)
80	32	Overvoltage during Burn In	Overvoltage during Test	Misorientation during Test
80	54	Overvoltage	Hot Plug	
70	8	Breakage in ground path	Overstress of ESD materials	Faulty component
70	23	Instable Tests : Test Equipment Disorder	Misorientation	
70	42	Hot plugging	Inductive switching	Spec violations
70	70	Over current		

For companies reporting a low percentage in finding root cause, root cause “cannot be determined” was a likely outcome. This could be a consequence of not having complete information on conditions, or difficulty with replicating the environment that produced the initial damage. For example, for damage reported to be due to EMI, analysis to root cause may be very difficult. It is a goal of this document (in Clause 7 and Clause 8) to help give more information on how to trace an EOS diagnosis back to the root cause of the damage including root causes such as EMI.

5.3.2.5 Diagnosis, Importance of EOS Reduction, and Failure Reports (cont'd)

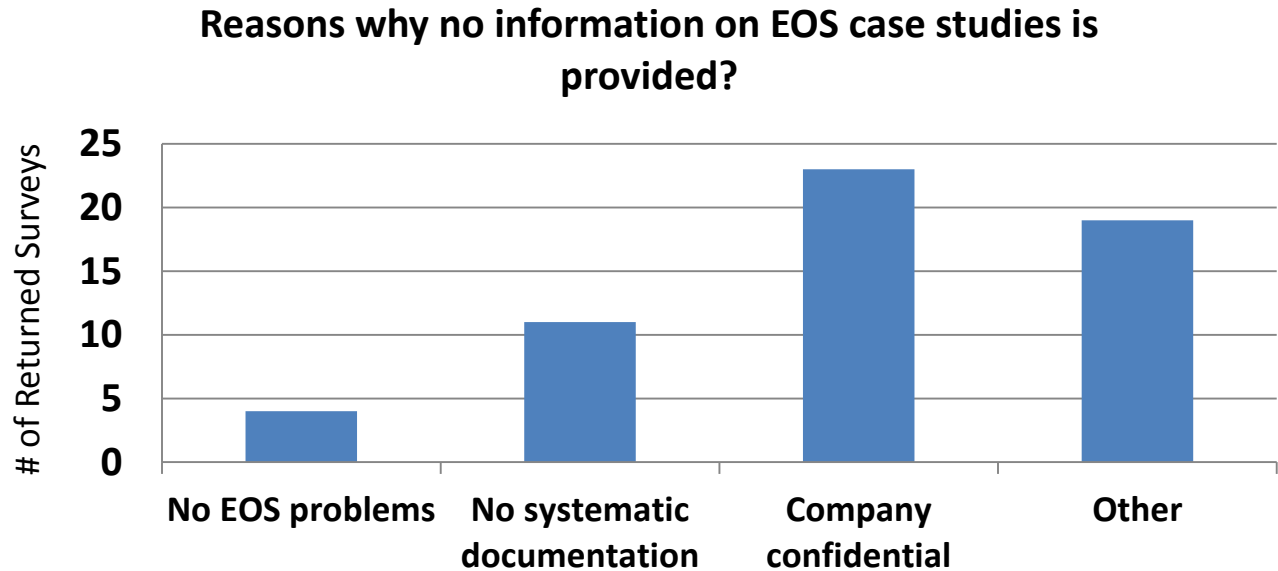


Figure 13 — EOS Survey Question 4

Question 4 of the survey asked for reasons why information on case studies of EOS could not be provided in the course of investigation. Figure 13 summarizes the results for companies not providing case studies. Confidentiality was a main reason, cited by 23 companies. A significant number cited “other” and did not elaborate. “No systematic documentation” was cited in 11 cases.

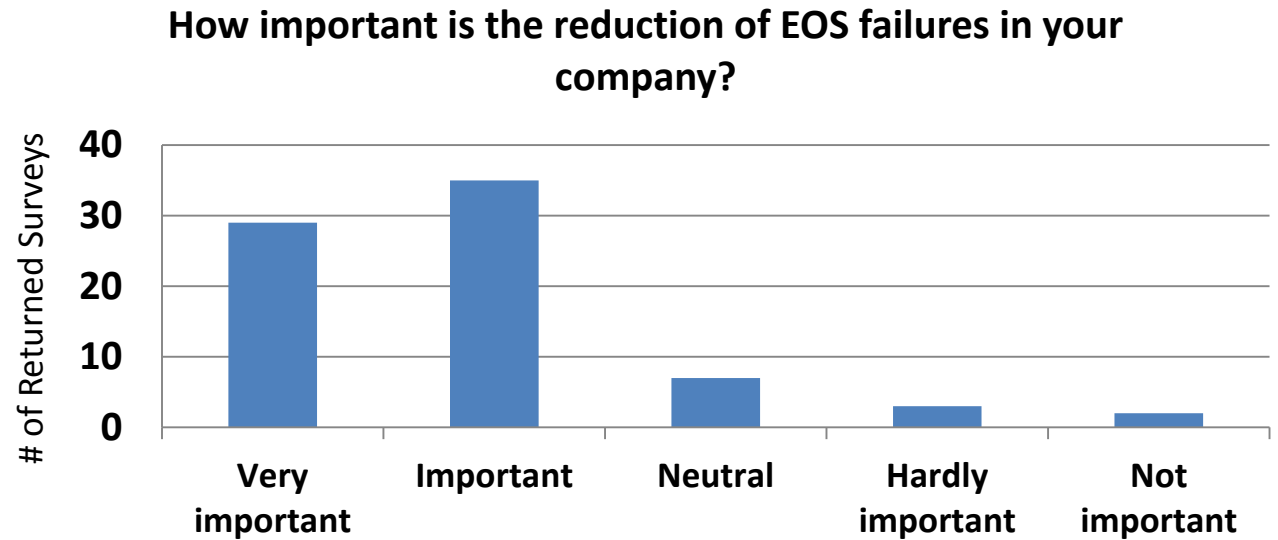


Figure 14 — EOS Survey Question 5a

Figure 14 shows the collective company response of perceived importance of reducing their EOS damage failure rate. 85% of respondents indicated a reduction of EOS failures was either “important” or “very important” to their company.

5.3.2.5 Diagnosis, Importance of EOS Reduction, and Failure Reports (cont'd)

Are the failure reports (8D reports) of device manufacturers helpful?

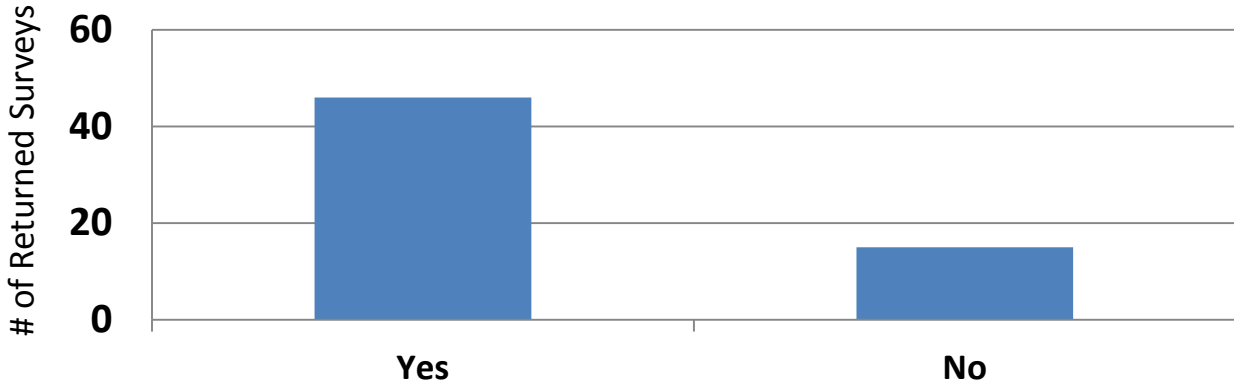


Figure 15 — EOS Survey Question 6a

For those respondents familiar with the “8D” (“8 Disciplines of Problem Solving” was first attributed to Ford Motor Company in the 1980s as a new process to address and solve difficult issues) problem solving methodology of system quality issues, Figure 15 shows that 75% of respondents indicated 8D reports are helpful to them. Although this result does not tie directly to reporting of EOS related issues, it indicates the 8D methodology would be helpful for investigating issues from EOS.

Does your company provide information on the conditions that caused the failure?

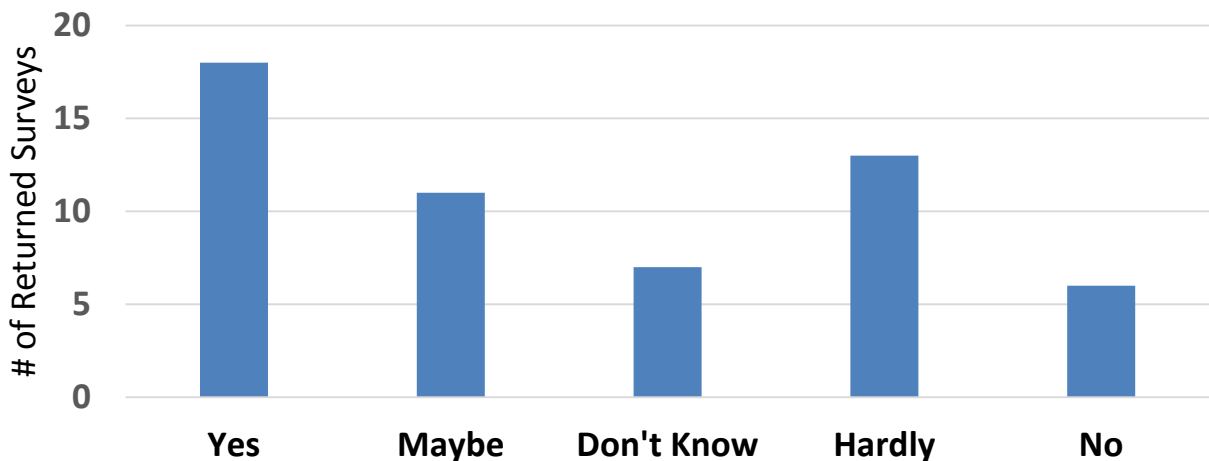


Figure 16 — EOS Survey Question 6c

A follow-on question to the 8D report importance question asked if the surveyed company would provide information on conditions that could have caused a failure exhibiting EOS damage. Although the highest percentage (34%) of companies reported they did report conditions, Figure 16 shows there was a wide distribution indicating many companies provided incomplete or no information on the failure conditions. This is a response indicating the need for improved communication in the EOS damage root cause diagnosis.

5.3.2.6 Responses on EOS Problem Minimization and Rate of Success

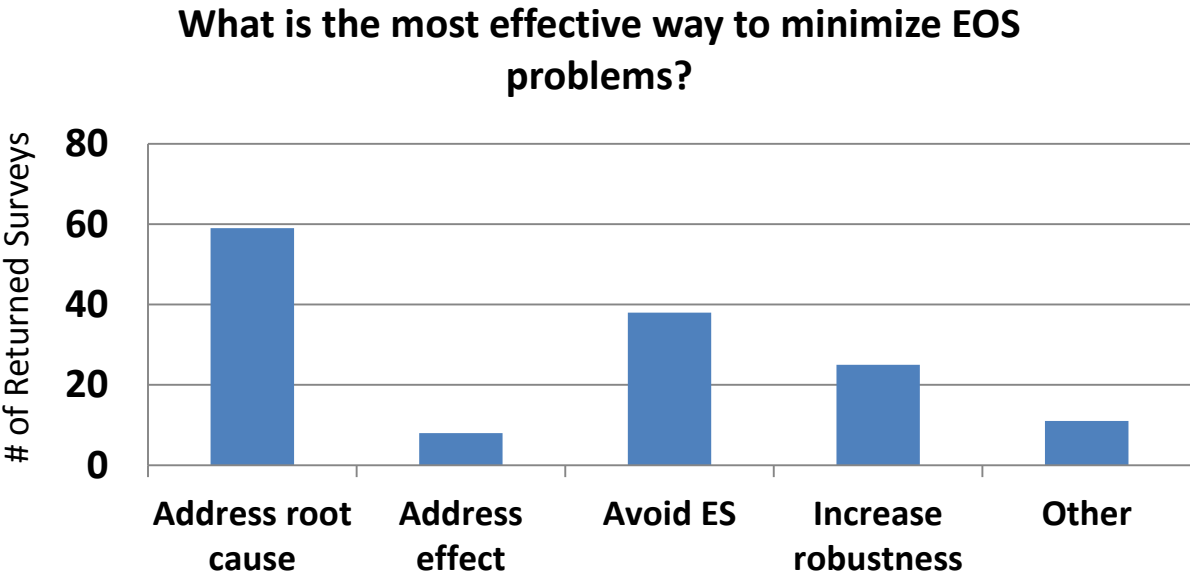


Figure 17 — EOS Survey Question 7a

Figure 17 shows the collective response to the question asking what the most effective way is to minimize EOS problems. The wide majority indicated addressing the root cause of the failure was the most effective way. Nearly half the respondents indicated avoiding the particular electrical stress was also a most effective way. Over 25% of the respondents felt that increasing the device robustness overall would help minimize EOS problems.

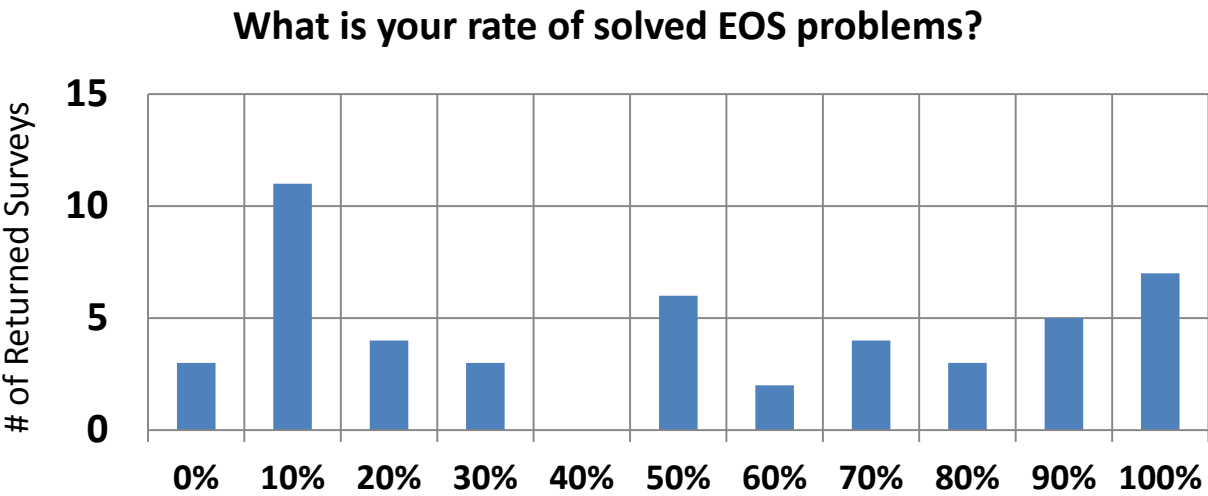


Figure 18 — EOS Survey Question 7b

Figure 18 shows the collective company response as to the “rate” of solved EOS problems. A wide distribution is indicated; there are higher percentages of responses selecting “very few”, 50%, and 90-100%. Looking over the last three survey questions, it can be seen that the lack of detailed industry wide information on the conditions of damage and addressing root cause creates a wide disparity in actually solving EOS problems. This is an area where communication and working together with more information could result in improvement.

5.3.2.7 AMR Usage and Importance

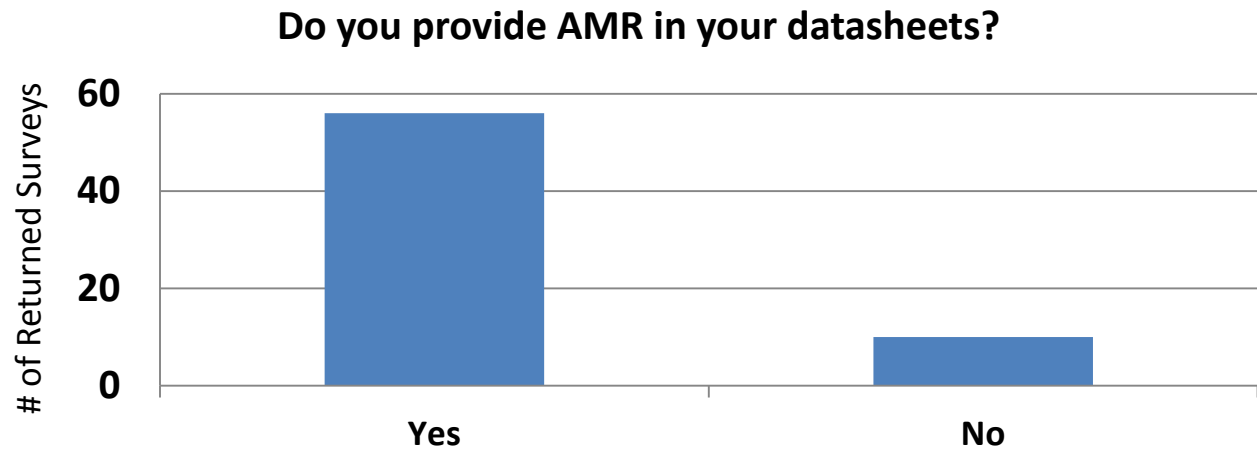


Figure 19 — EOS Survey Question 8a

Figure 19 shows the collective response to whether companies provide absolute maximum ratings values in product datasheets. The wide majority do provide AMR values.

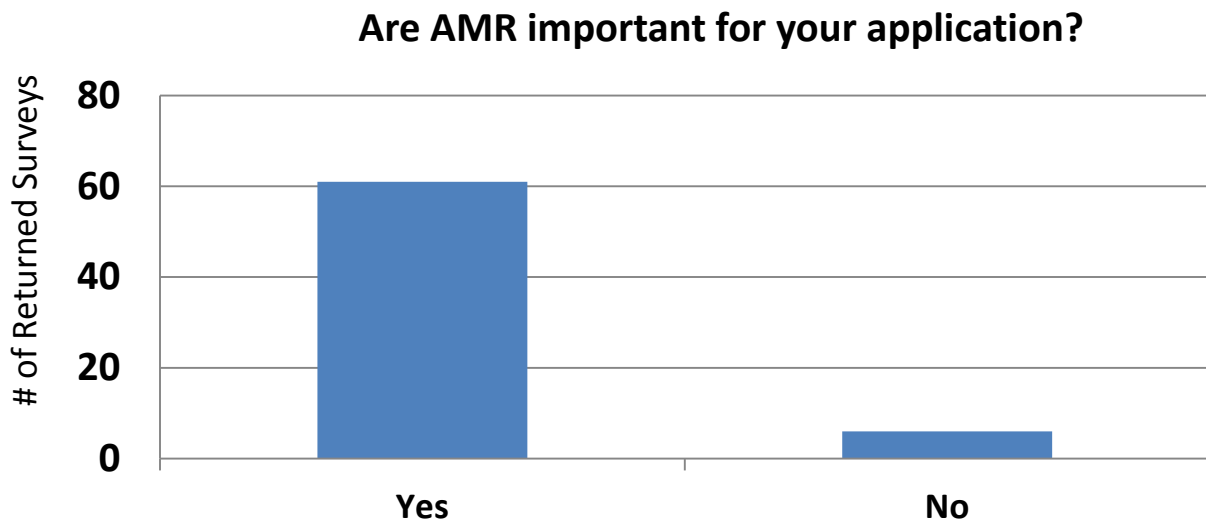


Figure 20 — EOS Survey Question 8b

A similar percentage of respondents reported in Figure 20 that they consider AMR important in their application. Nearly all responses were positive indicating suppliers, customers and OEMs agree on the importance of AMR.

5.3.3 Notable Industry Comments on the EOS Survey

In addition to the graphical response data, the EOS survey provided a forum for respondents to give specific comments on EOS issues. These responses included descriptions of how EOS is perceived within their company, how their customers view EOS, whether information on failure conditions is useful, how higher energy EOS damage could be differentiated from damage resulting from ESD events, etc. Below are some of those responses.

- *“We have spent considerable effort educating our customers on the difference between EOS and ESD. We request that the Industry Council take some care not to cause confusion. Very few EOS failures are due to ESD events - although we do have examples where the ESD cell is the weak point that is sensitive to an EOS event.”*
- *“As an IC supplier, we often see EOS induced failures, but receive very little to no feedback from the customer if they were able to identify the source of the EOS, or if any additional actions were taken as a result of the failure analysis provided by the IC manufacturer.”*
- *“EOS reduction/prevention should be a joint effort including (material supplier), IC suppliers, system applications to be more effective to find out. In my opinion, customers, modules and end-customers are even less aware of maximum applicable electric stress than it was the case in the past.”*
- *“If something goes wrong, the attitude is often: the device manufacturer has changed the process, because it has worked in the old module-versions.”*
- *“There is no longer a ‘sit-down-and-think-about’ attitude in case of a problem on system level. This leads to the problem that we do not get any clue from the customer side, what could happen. So we have to spend a lot of effort to prove a) it is not the process and b) do customer-side work and replicate a stress that gives us the same failure signature. When we are lucky, we get at least a very honest customer who tells us what he has done and what he has not done. So at least we have the chance to understand what has happened. Unfortunately in many cases a violation of already known text-book ESD/EMC/EOS was the “root” cause.”*
- *“A reliable way for characterizing AMRs is missing. Actually there are many definition/characterization ways presently used, which makes the definition of AMRs quite fuzzy as to how each manufacturer defines them. A comprehensive way is missing. Standardization could most probably help here.”*

Examples of ‘fuzzy’ AMRs are:

- 1) *A maximum supply voltage can be very close to the breakdown voltage of a given pin. How do we characterize this? How far should it be located? How can we take process spread in account for a given quality performance of the product in the field?*
- 2) *When characterizing for ESD, how much higher should the FAIL level be in order to specify a given PASS level?*
- 3) *Why some products have ESD-related AMR and some do not? Some AMRs shouldn't be compulsive for all products to be mentioned in the datasheet?*
- 4) *How to specify AMRs related to a transient performance of the IC?*
- 5) *How to test AMRs? Can ATE testing be enough and under which conditions?*

An AMR is a publishable parameter (stated in the datasheet). A priori it should not be dependent on the underlying manufacturing process. How can we guarantee this (such as in the case of process change or use of a new process)? AMRs related to misapplication/EMI types of EOS are missing.”

- *“Information is usually missing with respect to the real failure conditions at the system-maker, the car-manufacturer or from the user at the field. All should provide more information regarding the failure context (e.g. operation that was taking place during the failure and if possible voltages / currents available during that operation – for instance oscilloscope pictures). Also, handling tips should be available for products that do not fulfill the basic ESD specifications. The IC manufacturer should also provide hints in the 8Ds on how to mitigate EOS/ESD for a specific failure.”*
- *“We worry about EOS (for a product) when there are more than 2 quality hits on a product in a particular quarter (internal or external) with an EOS signature (very high current increase, FA result, field returns from one or more customers).”*

5.3.4 Top 4 Reported EOS Root Causes and Confidence Level

The information provided by the EOS survey results represents a collective summary of EOS perception in the industry. It also clearly identifies the most common important issues and observations. At the same time, the information reveals that a better industry-wide understanding is still needed to address EOS issues. It is helpful to keep in mind that while the information from the survey results may not address everything, it certainly points to the directions that should be considered.

First we summarize some generally accepted findings from the survey:

- EOS is the most common attribute of reported returns.
- The vast majority of respondents indicate that “damage signature” is used to determine EOS.
- EOS almost always represents permanent damage.

These observations alone suggest that, as expected by many in the industry, EOS is an industry wide issue (affecting supplier and customer operations in system / component development) that needs to be addressed. It is informative to list the top four root causes of failures exhibiting EOS damage as discerned from the survey.

1. **Misapplication:** Misapplication (referred to as power handling in Clause 7) stands out as the most widely reported root cause, involving a significant (over 20%) percentage of the reported failures exhibiting EOS damage. Misapplication can include unintended overvoltage, power supply sequencing, poor insertion (wrong orientation, misaligned devices), as well as incorrect biasing during applications.
2. **Absolute Maximum Rating:** A number of failures exhibiting EOS damage were attributed to applied voltages exceeding a specified AMR voltage. It is recognized that without proper AMR information on the datasheets, the likelihood of EOS damage increases. AMR are important for all applications that are utilized by the suppliers, manufacturers, and OEMs. It is important to note that a clear comprehensive definition of AMR becomes critical for effectively addressing EOS caused by misapplication.
3. **ESD Related:** Although it has been clearly established that component ESD target levels are not related to the rate of EOS damage, other forms of ESD have been observed at the system level and reported to contribute to the conditions causing EOS. These include charged board or charged cable events, system level events, discharges from charged devices, and ESD controls in manufacturing which are not compliant with handling ESDS devices. All of these events can be mitigated to a certain degree by paying close attention to, and improving ESD control practices, and ensuring that the levels of ESD control are appropriate for the devices, circuit boards, modules or products being handled.
4. **Miscellaneous Causes:** Beyond misapplication, AMR and ESD, many causes have been noted. As expected, these miscellaneous other reasons range from weak PCB designs to mishandling. Although each individual damage mode in this miscellaneous class is not widely reported, they do represent EOS root causes in their own right.

5.3.4 Top 4 Reported EOS Root Causes and Confidence Level (cont'd)

While these observations are all important, it is also useful to note the confidence levels regarding methods addressing these failures which exhibit EOS damage. These levels are listed below.

- i) **Root Cause Identification.** The survey results give the impression that most respondents are confident in tracing the root cause and confident that damage signatures from properly conducted FA reports can provide a *critical link* towards diagnosis of root cause.
- ii) **Communication.** The lack of information on conditions at the time of EOS damage can result in misdiagnosis of root causes, and can quite often result in ineffective or insufficient EOS prevention solutions. One effective way to address this is to clearly document the environmental and electrical conditions of applications in the 8D reports. Most feel confident that these would be very helpful. Including the AMR information in the communication process can go a long way to increase this confidence.

5.4 Impact of EOS Damage

It is clear that EOS has a large negative impact on the electronics industry. It is a primary, if not the top cause, of component returns at most companies. It was shown in the survey (see Figure 8) that the fraction of failures resulting from EOS damage among all failures ranged from 0% to 80%, with an average of about 25%.

It was further shown that the majority of damage was occurring not during component manufacturing, but in PCB/module assembly (30% on average) or in field applications (40% on average). As described earlier, component failures at these later stages can be very expensive, both in resolution time and cost. In most high reliability applications, if the failing devices in the board or product can be accessed, the devices are returned to the device manufacturer where resources are used to diagnose the failure and attempt to determine root cause. Failures exhibiting EOS damage during development or qualification of a new system can delay the entire program while the failure mechanism is found and an effective solution is found and implemented.

Failures resulting from EOS damage in the field are particularly troublesome. This is where the EOS impact is most keenly felt among multiple stake owners in the production chain. This is also where the potential for incorrect information or incorrect diagnosis about what actually happened becomes most troublesome. Often during the process a “discovery” may be found, and all parties are quick to put a “containment” fix in place and conclude victory, but the root cause of the underlying EOS issue may be left undiscovered. Care must be taken to analyze all potential locations where conditions leading to EOS can occur through a “fishbone” diagram that can involve multiple production facilities. “Maps” of where the damage can occur must be carefully tracked and updated, with severities noted, as both the energy levels and locations can give clues as to where the energy is coming from.

Communication among all parties is critical. The key is to share information and view the investigation, discovery and solution process as necessary opportunities for improvement and not to place blame. Often the solution can be a fix that is not EOS-related. That possibility must always be taken into account. A method for stakeholder interaction through the use of failure reports is given in 5.5. Clause 7 and Clause 8 give a number of examples of EOS investigations involving the entire supply chain and provide an illustration of good methodologies for EOS investigation and successful improvement.

5.5 Failure Reports of Products Exhibiting EOS Damage

There is perennial confusion in distinguishing and classifying failures resulting from EOS damage with those resulting from ESD events through FA reports. Simply classifying them as "EOS/ESD" is not helpful and mistakenly gives the impression that EOS and ESD are one and the same, which they are not. As most companies have indicated in the survey, the most effective manner to address failures resulting from EOS damage is through detailed analysis and identification of the true root cause. Therefore, FA reports can play a critical role as long as the conclusions are not misleading to the customer or to the supplier. It has been noted that EOS damage can occur in different locations on the chip, or within multiple components of a system, and so it can be difficult to pinpoint a root cause. For example, a latent defect in a very high yield process which, when present, may lower the breakdown voltage of a path such that operation over time changes a latent defect to failure. The failure may manifest as looking like ESD damage when in fact it was not subject to an event exceeding AMR at all. Careful failure analysis and communication between supplier and customer regarding device operating conditions can make the difference between a diagnosis of EOS from ESD and a process defect driven diagnosis which is not EOS.

The information from FA reports can lead to the creation of EOS-related 8D report "formats" that a majority of customers would like to see. The survey results indicated that the 8D reports serve an important function in the EOS analysis. It does not mean, however, that this directly relates to EOS. But it does indicate that following the 8D process could help reduce the incidences of EOS.

FA reports can fall into two categories: 1) reports with a well-defined damage mechanism and 2) reports with unknown conclusions. If a report shows a systematic failure mechanism in each case (or device after device), there is a clear case for finding the root cause and for fixing the problem. Finding the root cause should be the ultimate goal of the 8D report. But if the FA indicates detection of one random failure, never to be seen again, then writing the 8D report will very likely fall short of this goal. Thus, an overall balance between FA report results, documentation of the 8D reports to communicate the cause of the problem, recommendations to resolve them, and improved communication along these lines, could help to mitigate EOS.

6 The Definition of EOS – Finding Common Understanding

The purpose of this clause is to provide a practical interpretation of EOS using information commonly provided in datasheets: the AMR. This definition is essential for further discussion in this paper and is crucial for communication between suppliers and customers. Past experience shows that misunderstanding EOS can lead to disastrous results. An aligned understanding allows semiconductor manufacturers to clearly provide the maximum electrical limits for their devices. Knowing these limits allows system manufacturers to optimally incorporate those devices into their systems while providing a working environment in which the devices can safely operate.

During discussions to define EOS, it became obvious that there are many interpretations. While they often share some basic characteristics, the details of these definitions vary. For example, some definitions recognize the time dependency of the electrical stress; others are adamant that EOS is a DC or near DC phenomenon. To further complicate a single EOS definition, these many definitions are not held lightly by their advocates. Not only do the definitions have economic consequences, but they frequently represent years of hard work and effort and, as a result, are often fiercely defended.

Many kinds of situations can cause an electrical device to operate outside its intended electrical range. Whether these conditions are caused by its environment, happen during testing, or occur during regular operation, a critical distinction must be made: has the device reached the level of an EOS event or is it still below the specified maximum operating condition of the system or device? It is well known that brief operation above the specified maximum operating condition may not result in immediate failure, even though this operation will stress the device and may decrease its lifetime. Increasing the stress condition further then leads to immediate damage in the same device or device region where the initial stress was seen. The essential requirement is to provide limits to electrical parameters for electrical devices describing when they begin to be exposed to EOS.

To reach a common understanding which more precisely describes the situation of electrical overstress, a differentiation has to be accepted between an EOS event, EOS damage, and an EOS root cause. An **EOS event** is notable when it results in disruption of normal system operation, particularly if the device is permanently damaged. This is called a **failure related to EOS damage**. However, damage can still occur in a system that remains functional, only showing up as a reduction in the device lifetime.

Similarly, a clear definition of EOS should aid in the analysis of failures which exhibit EOS damage by providing common ground for categorizing the actual **root cause of the EOS**. It is necessary to be able to correctly categorize the root cause in order to debug, correct, and optimize systems to protect against EOS (as discussed in Clause 7).

Taking into account the broad understanding of the phenomenon, the following definition of EOS is presented and will be used as the basis of all discussion in this white paper:

An electrical device suffers electrical overstress when a maximum limit for either the voltage across, the current through, or the power dissipated in the device is exceeded and causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.

Critical to this definition is a clear understanding of what is meant by maximum limit. The rest of this clause will further expand this definition by providing a practical interpretation of EOS in terms of AMR, looking at existing, accepted documentation practices to bring color and life to our definition.

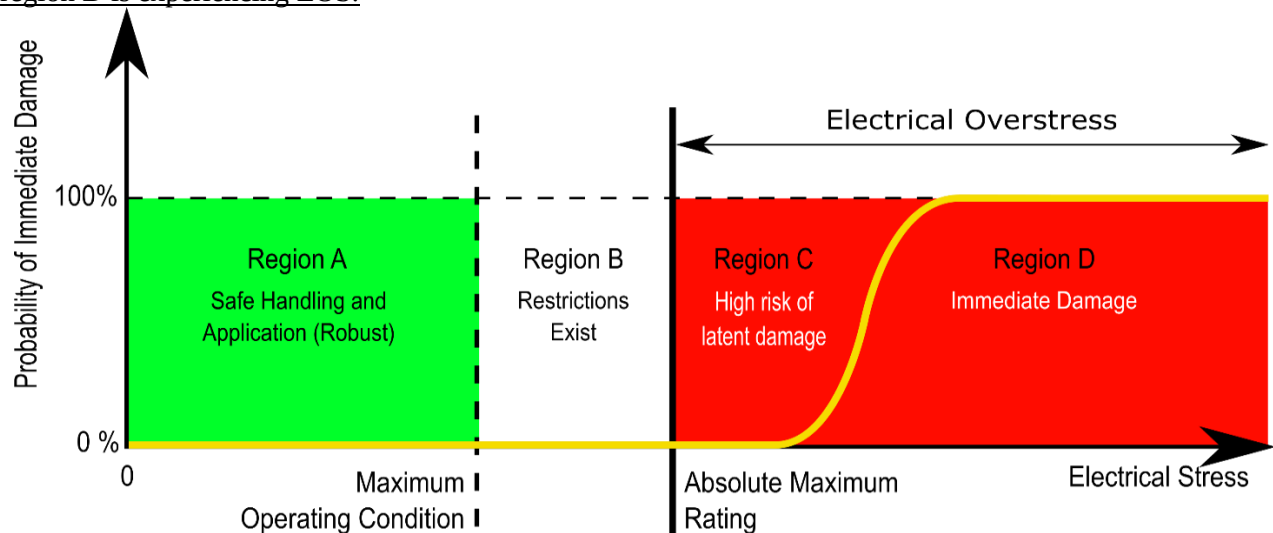
6.1 Existing Documentation Practices of AMR Values

The purpose of 6.1 is to look at different uses of AMR across the industry to describe the maximum limits of operation which should never be exceeded. Examination of existing documentation shows that different manufacturers have their own unique ways of defining an AMR for a semiconductor component.

One use of AMR can be found at JEDEC. Here it is defined as the maximum voltage that may be applied to a device, beyond which damage (latent or otherwise) may occur. However, absolute maximum ratings can refer to voltage, temperature, currents and any other operation parameter which can cause damage to the device.

Similarly, some industry references indicate that stresses above absolute maximum ratings may cause permanent damage to the device [107-110]. It is emphasized that this is a stress rating only and functional operation at this or any other conditions above the specified operation conditions is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Due to the statistical nature of destructive fails, any AMR level needs to be related to an acceptable failure-in-time (FIT) value. However, in general, no details on failure rates are provided with AMR tables in datasheets. Similarly, the specification of unique destruction levels for short duration stress is not evident due to the time dependence of the damage mechanisms.

Insight into the electrical aspects of AMR can be gained by examining the voltage ranges illustrated in Figure 21. First, there is the safe operating area, a region of robust operation (region A). This is the region in which the manufacturer designed the device to operate. This is followed by a region in which operating restrictions exist (region B). In region B, the device is not guaranteed to function as specified, however the device is not expected to be physically damaged. Operating the device in region B for extended periods of time may also result in reliability issues. The upper limit of region B is the AMR. At and beyond the AMR the user should expect problems. Beyond the AMR are two regions of electrical overstress with either latent (region C) or immediate (region D) damage as a result of exceeding AMR. Note that the transition between latent damage and immediate damage is subject to normal process variations as illustrated by the yellow S curve starting at the high end of region C. In order to properly evaluate the product reliability and robustness, it is important to understand that some qualification stresses, such as device level ESD and latch-up, are *expected* to run evaluations that will exceed AMR. For example, in the case of latch-up, this may be necessary in order to get significant current injection to assess latch-up robustness. Regardless, a device operating in either region C or region D is experiencing EOS.



NOTE The yellow line is the number of components suffering immediate, catastrophic EOS damage, repeated from Figure 1.

Figure 21 — Graphical depiction of how Absolute Maximum Ratings should be interpreted

6.1 Existing Documentation Practices of AMR Values (cont'd)

In addition to the electrical and ambient conditions that the AMR values are based on, there are differences in the way stress data is assessed when the AMR values are being extracted.

- **Region C:**

A manufacturer may pick conservative AMR values not based on physical properties of the product. This results in a wider region C before the onset of immediate damage. Alternatively, the manufacturer may define the AMR values based on detailed circuit and technology understanding for an accurate prediction of the damage threshold. This detailed approach would result in the yellow S curve in Figure 21 shifting left until the point where it rises up from the X axis while nearly touching the AMR boundary, greatly reducing region C. Regardless of the method chosen, the manufacturer is *solely* responsible for defining the AMR values.

- **Time dependence:**

The AMR may be defined by a single voltage or current or it may have different values for different stress durations. Ideally, any documented value should have a fixed time association.

In general, the astute system manufacturer should understand that while an operating region may exist between the specified maximum operating condition and the AMR values (region B), this region is there to provide a buffer for stress events to the system without disrupting normal operation. The device is typically not tested or guaranteed to be fully functional above the specified maximum operating conditions. Any attempt to operate in this region must be discussed with and agreed upon with the supplier. Additionally, not every device will fail immediately upon experiencing an event above AMR (region C). However, this is still an EOS event and is considered high risk for latent damage and likely future permanent damage. Any unit experiencing an event exceeding AMR will have the risk of experiencing latent EOS damage. Finally, a well written AMR will often be specific to the environment in which the device is expected to operate by its manufacturer. It is not only the manufacturer's definition of the maximum electrical and thermal limits, it also defines the limits of the manufacturer's responsibility when the component is damaged as a result of exceeding those limits.

Beyond this discussion of regions of operation where the AMR describes maximum electrical and environmental values of operation, there is controversy about whether it should also refer to ESD limits. As noted above, while recognizing that this definition of EOS focuses attention on the AMR, placing greater significance and expectations on its limits than may have been given in the past, each supplier has their own approach to setting the AMR values. With respect to ESD, several different approaches have been observed:

- Some suppliers do not include ESD limits as part of their AMR because testing to establish the ESD limits often does not have similar statistical data collected as is required for setting more traditional items such as voltage.
- Some suppliers do place ESD limits in their AMR definition as it is felt that this is part of the overall agreement that must be met between supplier and customer.
- Other suppliers have placed ESD limits in an AMR section for no other reason than it was the only place that it made sense to them.

Regardless of the approach taken, the supplier is *solely* responsible for deciding what parameters and limits are included in their product's AMR.