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Guideline for evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion

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GUIDELINE FOR EVALUATING BIAS TEMPERATURE INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION

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Foreword

This publication has been drafted and approved by the JEDEC JC-70.2 SiC Power Electronic Conversion Semiconductor Standards subcommittee, which consists of recognized industry experts from foundries and fabless member companies.

- existing JEDEC documents such as JEP122 and JESD241 already address threshold voltage instability for metal-oxide-semiconductor (MOS) devices, their focus is primarily silicon devices for CMOS and memory applications, and as such, do not fully address aspects of SiC devices that can make threshold-voltage-instability characterization more complex;
- this document does not have the intention of superseding or changing the guidance of JC-70.2: TG702_3 “Guidelines for Threshold Voltage (V_{th}) measurement of SiC MOSFET” regarding measurements of threshold voltage for device characterization purposes;
- the Annexes included here (A - D) are informative in nature.

Introduction

The objective of this publication is to provide useful definitions and procedures for characterizing the threshold voltage instability of SiC-based power electronic conversion semiconductor (PECS) devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS devices such as field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs). Monitoring of threshold-voltage instability in MOS devices is commonly referred to by the term “bias-temperature instability” (BTI), while the applied stress to check for instability is usually referred to as “bias-temperature-stress” (BTS). The terms BTI, BTS, and threshold-voltage instability will be used throughout this document.

GUIDELINE FOR EVALUATING BIAS TEMPERATURE INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION

(From JEDEC Board Ballot JCB-21-16, formulated under the cognizance of the JC-70.2 Subcommittee on SiC Power Electronic Conv. Semiconductor Standards.)

1 Scope

The scope of this document covers SiC-based PECS devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS devices such as MOSFETs and IGBTs. In this document, only NMOS devices are discussed as these are dominant for power device applications; however, the procedures apply to PMOS devices as well.

This document does not define device failure criteria, acceptable use conditions or acceptable lifetime targets. That is up to the device manufacturers and users. But it provides stress procedures such that the threshold voltage stability over time as affected by gate bias and temperature can be demonstrated and evaluated.

2 Normative References

JEP183, *Guidelines for measuring the threshold voltage (V_T) of SiC MOSFETs*.

3 Terms and definitions

3.1 metal-oxide-semiconductor field-effect transistor, MOSFET: an insulated-gate field-effect transistor in which the insulating layer between the gate electrode and the channel is oxide (or dielectric) material and the gate is metal or another highly conductive material. (Ref. IEC 747-8 and JESD77).

3.2 silicon carbide, SiC: A wide bandgap semiconducting material that serves as the active device semiconductor material, for example the channel and drift region. Typically the 4H hexagonal polytype is preferred, denoted 4H-SiC, in the (0001) wafer orientation (other polytypes sometimes used are 6H-SiC, or 3C-SiC).

3.3 power electronic conversion semiconductor (PECS) devices: Power devices used for power conversion to different voltage or current levels, or as inverters between alternating and direct current power (or vice versa).

3 Terms and definitions (cont'd)

3.4 gate oxide: oxide (or dielectric) region under the gate electrode in the MOS portion of the MOS device

3.4.1 oxide thickness (T_{ox}): gate oxide (or dielectric) thickness, measured electrically, optically, or physically.

3.4.2 oxide field (E_{ox}): oxide field (V/cm), V_{ox}/T_{ox} .

3.4.3 oxide voltage (V_{ox}): voltage drop across gate oxide (V).

3.4.4 gate to source voltage (V_{GS}): Voltage drop from gate to source (V).

3.4.5 gate current (I_G): Gate current (A) measured with a bias on the gate electrode.

3.5 drain to source voltage (V_{DS}): Voltage drop from drain to source (V).

3.6 drain current (I_D): Drain current (A) measured with a bias on the drain.

3.7 voltage of tied gate and drain to source (V_{GDS}): Voltage drop of gate and drain to source (V), when gate and drain biases are tied together (gated diode configuration).

3.8 gate-source voltage maximum (V_{GSmax}): Maximum gate-source voltage recommended for a device, for any time period during operation.

3.9 gate-source voltage recommended operating value (V_{GSop}): Recommended range of gate to source bias during normal on-state or off-state operation.

3.10 bias temperature instability (BTI): susceptibility of the threshold voltage of an MOS device to change over time under bias and temperature stress.

3.11 negative BTI (NBTI): BTI due to a negative gate bias stress, at a fixed stress temperature.

3.12 positive BTI (PBTI): BTI due to positive gate bias stress, at a fixed stress temperature.

2.13 bias-temperature stress (BTS): stressing a device by simultaneous exposure to gate bias and elevated temperature. Often used in place of the acronym BTI; the difference (if any) is that BTI refers more specifically to the effect of stress on V_{th} , whereas BTS is more of a descriptor of the stress condition on the device.

3 Terms and definitions (cont'd)

3.14 threshold voltage V_T : the gate-source voltage V_{GS} value (at some specified drain voltage V_{DS}) at which the device conducts forward current of a specified current value. A drain-current-defined threshold is used in this document, with the selected current at threshold being a very small fraction of the rated device current.

3.14.1 threshold current (I_T): the drain current at which V_T is defined.

3.14.2 threshold voltage, gate-source sweep configuration ($V_{T(GS)}$): V_T measurement performed by sweeping the gate bias with a constant and relatively low drain bias (~ 100 mV min, up to a few Volts typically) until a certain I_D current value is reached.

3.14.3 threshold voltage, gated-diode configuration ($V_{T(GDS)}$): V_T measurement performed by sweeping the gate and drain together ($V_{GS} = V_{DS}$) until reaching a chosen constant I_D value. The gated-diode configuration allows for fast and reproducible point measurements of the V_T and guarantees a constant electron density in the channel during V_T readout.

3.14.4 threshold voltage measurement, following a Negative Bias Stress (V_T^{UP}): the V_T measurement performed immediately following a negative gate bias stress during NBTI, or following a negative V_{GS} conditioning pulse (as in a hysteresis measurement), or if performed by sweeping the gate bias starting from a negative gate voltage and sweeping up until I_T is reached. In general, V_T^{UP} will represent the low V_T side of the hysteresis in V_T . To minimize recoverable fast charge-trapping effects and achieve repeatable results, it is recommended to stabilize the traps by holding at the negative V_{GS} for a sufficient duration; 100 ms is a typical recommended value for SiC.

3.14.5 threshold voltage measurement, following a Positive Bias Stress (V_T^{DOWN}): the V_T measurement performed immediately following a positive gate bias stress during PBTI, or following a positive V_{GS} conditioning pulse (as in a hysteresis measurement), or if performed by sweeping the gate bias starting from a positive gate voltage and sweeping down until I_T is reached. In general, V_T^{DOWN} will represent the high V_T side of the hysteresis in V_T . To minimize recoverable fast charge-trapping effects and achieve repeatable results, it is recommended to stabilize the traps by holding at the positive V_{GS} for a sufficient duration; 100 ms is a typical recommended value for SiC.

3.14.6 threshold voltage at a given stress time ($V_{T\#}$): the V_T is measured over time during the BTI stress, thus a time-related subscript can be used when referring to a particular stress time. For improved extrapolation of V_T over time, the initial measured V_T during BTI should be after a brief (~ 100 ms) initial stress and/or conditioning, such that V_{Ti} (or V_{Ti0}) occurs after the initial brief stress. The initial pre-stress V_T and the final post-stress V_T may be defined using different subscripts, such as V_{Tpre} and V_{Tpost} , respectively.

3 Terms and definitions (cont'd)

3.15 threshold voltage shift ($\Delta V_T^{\text{shift}}$): a change in the measured V_T value from an initial to a final condition, here particularly focused on the V_T shift during BTI stress. This shift is described as the ongoing shift over time ($V_{T\#} - V_{Ti}$), which by the end of the stress would be the final V_{Tf} minus the initial V_{Ti} . This shift value could be due to: 1) transient charging effects ($\Delta V_T^{\text{trans}}$) which are fully recoverable, 2) transient effects which have a permanent component (ΔV_T^{HYST}), or 3) permanent (non-transient) interface effects ($\Delta V_T^{\text{drift}}$). More generally, V_T shift is the change in V_T between any two measured values, and can arise from a change in gate bias, or the continued application of the same gate bias.

3.15.1 threshold voltage drift ($\Delta V_T^{\text{drift}}$): threshold voltage drift describes BTI changes in V_T ($\Delta V_T^{\text{shift}}$) which are relatively permanent, after transient V_T recovery effects are removed. For example, if a V_T^{shift} is measured without a change in transient effects, there would be a shift in the voltage location of the threshold voltage due only to a $\Delta V_T^{\text{drift}}$ effect.

3.15.2 threshold voltage transient shift ($\Delta V_T^{\text{trans}}$): portion of the BTI threshold shift ($\Delta V_T^{\text{shift}}$) that quickly recovers after removal of gate stress. This is typically larger or beyond what a short hysteresis measurement would reveal, due to time at bias effects during BTI that result in charging on a time scale that a short hysteresis measurement does not capture.

3.16 threshold voltage hysteresis ($V_T^{\text{HYST}} = V_T^{\text{DOWN}} - V_T^{\text{UP}}$): difference in threshold voltage measured after a positive gate bias stress (V_T^{DOWN}) and that measured after a negative gate-bias stress (V_T^{UP}) of equal stress time. For normal devices, with at least some active interfacial traps (and little or no mobile ions), this hysteresis value will be positive. For what is here considered intrinsic device hysteresis, the timing for the stress and sense portions of a hysteresis measurement called for are on the order of 100ms. Faster or slower measurements can be useful to reveal more complete details of the transient effects.

3.16.1 change in threshold voltage hysteresis ($\Delta V_T^{\text{HYST}} = V_T^{\text{HYST}}_{(f)} - V_T^{\text{HYST}}_{(i)}$): the difference between final (post-BTS) and initial (pre-BTS) hysteresis values would comprise a change in hysteresis. Because there is a stress time dependence of the magnitude of this value, this term is used to describe the permanent (repeatable) hysteresis effects observed when performing a standard 2-sequence hysteresis measurement as described above.

3.17 conditioning: term to describe applying a gate bias to induce a certain charge state immediately prior to a V_T measurement. To make a fair comparison of changes in V_T due to a BTS, the same V_{GS} conditions (conditioning) should be used before each measurement.

3.18 relaxation: term referring to charge redistribution over time after gate bias is removed, which typically allows the V_T to shift back towards values before stress was applied.

3.19 recovery: term to describe the change of the V_T value after BTI towards the previous value due to a removal of bias (similar to relaxation), or due to the application of a different fixed bias.

3 Terms and definitions (cont'd)

3.20 degradation: a change in the charge state or trap density of the interface or near-interface regions as a result of BTI stress, which will manifest itself as a change in $\Delta V_T^{\text{drift}}$, V_T^{HYST} , or $\Delta V_T^{\text{trans}}$, depending on the physical nature of the interface changes.

3.21 drain-source on-state resistance ($R_{\text{DS(on)}}$): resistance of the device (Drain-Source) in the on-state with the rated V_{GS} applied, and at a specified (typically the rated) on-state current.

3.22 off-state drain current ($I_{\text{DSS(off)}}$): drain leakage from source with device in the off-state (at $V_{\text{GS}} = 0$ V or the rated off-state V_{GS} value), in the static mode (non-switching), at a specified high V_{DS} bias (such as the rated blocking voltage).

4 General Introduction to threshold voltage (V_T) stability and SiC-based MOS devices

Threshold voltage (V_T) stability is a general aspect of MOS device reliability that has been studied extensively for Si-based MOS devices [1-4] and has been touched upon in existing JEDEC documents focused on Si device reliability [5-11]. However, numerous literature reports have shown that SiC devices have more excessive threshold instability and much larger fast V_T recovery effects than Si-based devices [12-16], and unlike Si have appreciable shift in both PBTI and NBTI stress conditions. Thus, a more detailed BTI document is needed to address SiC MOS device behavior.

The different behavior of SiC MOS devices is believed to be related to the much more complex interface and near-interface trap levels (differences in both density and energy level compared to Si devices). Although high interface trap density (D_{IT}) levels at the oxide/SiC interface have been reduced by using N interface passivation for SiC (as H passivation is ineffective for the (0001) Si-face of SiC), the interface trap density of modern SiC MOS devices is still >10X higher than that of silicon MOS devices, covering a wider range of energy levels as well. In addition to interface traps, the near-interface oxide trap (also known as a border trap) density is also high. Border traps may be charged more readily due to the larger bandgap of SiC and the smaller band offsets to the oxide. The wide bandgap of SiC allows existing oxide defects that may be electrically inactive in Si to now fall within the SiC bandgap and act as traps.

The higher density of charge traps (regardless of origin) and other interface bonding differences can result in larger amounts of threshold voltage shift with time, temperature and bias; this phenomenon is commonly referred to as bias-temperature instability (BTI). This higher trap density can also result in faster V_T recovery when bias is removed, if the density of traps close to the conduction band energy level is very high. This means that V_T shift due to permanent and transient effects need to both be well understood and evaluated. Although both silicon-based and SiC-based devices display BTI likely due to the same general physical phenomena, the BTI in SiC-based devices is higher and transient effects are larger in magnitude. Therefore, it is critical to have well described approaches to characterize the BTI of SiC devices.

4 General Introduction to threshold voltage (V_T) stability and SiC-based MOS devices (cont'd)

The trap charging and discharging process also results in a threshold voltage hysteresis (V_T^{HYST}) when V_T is measured after positive and negative gate bias sequences. Some portion of the BTI shift may not recover over time in an unbiased state; this would be defined as a (permanent) drift ($\Delta V_T^{\text{drift}}$) arising from the BTI stress. It may also be the case that the threshold hysteresis magnitude (V_T^{HYST}) increases during BTI stress, termed a change in hysteresis (ΔV_T^{HYST}). Because the faster transient portion of the $\Delta V_T^{\text{shift}}$ has a time dependence and may increase with stress time, this fast-transient shift is termed here $\Delta V_T^{\text{trans}}$ (this can contain changes in the hysteresis as well, depending on the measurement conditions).

In summary, the measured threshold shift ($\Delta V_T^{\text{shift}}$) during BTI is composed of possibly three components: permanent drift (V_T^{drift}) + transient effects ($\Delta V_T^{\text{trans}}$), wherein the transient effects may include changes in hysteresis (ΔV_T^{HYST}). The inherent hysteresis (V_T^{HYST}) which is present may or may not be monitored during BTI, depending on the method of the BTI measurement.

SiC PECS devices are typically used in switching applications, in which the gate can either be switched continually from zero to positive gate bias or from a small negative gate bias to positive gate bias. In those cases, the V_T shift would depend on frequency of switching and duty cycle as well as V_{GS} levels of the positive and negative switching states. However, the most straightforward stress for the determination of MOS device stability is BTI stress performed under constant gate bias, as also occurs in qualification stress methods such as high temperature gate bias (HTGB) called out in JESD47 [8]. The procedures described here can be applied to HTGB stress as well. BTI under constant positive (PBTI) and negative (NBTI) bias results in V_T shifts which serve as a good metric to demonstrate MOS interface quality. Both PBTI and NBTI need to be characterized because they represent device on-state and off-state situations, and can show different time, temperature, and bias dependences.

Measurement of device switching characteristics, whether under conditions of high-power dissipation or not, while extremely important, falls outside the scope of BTI stress methods discussed here. However, a general description of device behavior during gate switching is included in Annex C.

5 Considerations for bias-temperature instability (BTI) stress methods and shift evaluation for SiC-based MOS devices

BTI stress procedures would ideally cover the operational limits of gate bias, temperature, and time, such that a ‘safe-operating-area’ (SOA) can be understood by the device user in an application. While it is very difficult to cover all conditions (especially regarding time), the goal is to cover appropriate stress conditions that will enable V_T shift projections to long use times; or at least to demonstrate the device threshold voltage behavior under constant bias gate stress.

In general, BTI V_T stability stress should be an evaluation of V_T stability over time at different levels of gate bias and device temperature, ideally without allowing the effects of V_T recovery to mask any application-relevant device instability. The measured threshold shift during BTI can be composed of long term V_T drift ($\Delta V_T^{\text{drift}}$), transient V_T changes ($\Delta V_T^{\text{trans}}$), and hysteresis behavior (V_T^{HYST}) or changes in hysteresis (ΔV_T^{HYST}); these will be discussed in detail below. Constant bias stress under both PBTI and NBTI conditions should be performed to allow V_T shift behavior to be determined under both positive and negative gate bias conditions (device on-state and off-state situations).

There are a variety of stress and measurement techniques that have been described in the literature; some appropriate approaches will be described in this document. Some differences in the $\Delta V_T^{\text{shift}}$ will be observed depending on the V_T sense approach used, as will be discussed. Thus the BTI approach used must always be described with a BTI V_T shift dataset.

In summary, the goal of BTI stress is to determine the shift of the threshold voltage as a function of the stress time (t_S), stress voltage (V_{GS}) and stress temperature (T_S), to demonstrate threshold characteristics under constant gate bias stress (representing a situation that can readily be compared between devices). A final goal would be to determine general safe operating limits (SOA) before the on-state resistance $R_{DS(\text{on})}$ and the off-state blocking leakage $I_{DSS(\text{off})}$ fall outside of data sheet or application specific operation conditions; however, this may not represent actual applications well because the devices don’t typically operate under unipolar gate stress. However, BTI stress results nevertheless represent a useful standard approach to demonstrate V_T stability. This document describes appropriate measurement approaches, and appropriate ways to interpret the measurement results.

5.1 Mechanisms of V_T shift and hysteresis resulting from PBTI/NBTI stress

The threshold voltage and the shift in V_T depends on the charge state of existing interfacial traps (typically interface and near-interface (border traps)), the effects of new traps created by the stress, and how these change over time. Typically trap filling and/or trap generation occurs during stress, and de-trapping occurs when stress is removed, resulting in an observed V_T hysteresis when the device experiences an opposite polarity bias (switching) sequence.

Interface traps and near-interface oxide traps (border traps) are intrinsically present at or near an interface between an oxide and semiconductor due to property differences between any two materials that are not epitaxial and lattice-matched. Processing can reduce the density of these defects, but some are always present. These intrinsically present defects will shift threshold in the direction of the applied V_{GS} stress during BTI stress. Extrinsic contamination near the interface region usually makes the V_T shift much worse. These can cause additional shift in the stress bias direction, or even a shift opposite to the applied bias if the impurity is a mobile ion species or forms a polarizable molecule. The discussion throughout this document is focused on the effect of intrinsically present traps that are not due to extrinsic impurities. However, regardless of the origin of V_T shift during BTI stress, the stress methodology remains the same.

The effect of the BTI phenomena is that when V_T changes, other device parameters such as $R_{DS(on)}$ and $I_{DSS(off)}$ can shift relative to their values when the device was manufactured. The mechanisms and effects are similar in SiC-based and Si-based devices, but the effects can be more pronounced and have a different time dependence in SiC-based devices. The issues are complicated due to: A) the wide bandgap of SiC (resulting in different trap densities and energy levels), B) differences in the interface chemistry/properties of the various SiC crystal faces (for example, the planar MOSFET device channel is typically on the Si-face (0001) of SiC while a trench device may have an MOS interface on the perpendicular a-face {11-20} family of planes), C) the chemical difference of SiC versus Si at the interface with SiO_2 , D) the higher temperatures used for oxide processing in SiC MOSFETs, and E) the different interface passivation elements utilized for SiC MOS devices (usually nitrogen, not hydrogen).

The large concentration of fast-acting trap states results in the parametric shifts recovering partially or completely when the bias is removed or reversed, such that post-stress V_T measurements at ambient temperature may show little of the shift that was recorded at high temperature during the stress. However, this recovery does not necessarily indicate that the effects of the stress are entirely removed; rather, the recovery may mask the effects of the BTI stress (the effects of BTI may return quickly under device operating conditions). Therefore special stress procedures are required to condition the interface such that transient effects are observed. It is recommended that both permanent and transient effects are measured in the BTI stress if possible. The long-term V_T shift during BTI and the V_T hysteresis before and after stress both need to be monitored to get a complete understanding of the effects of BTI stress, and recovery effects.