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Guideline for Evaluating dv/dt Robustness of SiC Power Devices

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GUIDELINE FOR EVALUATING DV/DT ROBUSTNESS OF SIC POWER DEVICES

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Foreword

This publication has been drafted and approved by the JEDEC JC-70.2 SiC Power Electronic Conversion Semiconductor Standards subcommittee, which consists of recognized industry experts from foundries and fabless member companies.

While existing JEDEC document JESD94B “Application Specific Qualification Using Knowledge Based Test” already addresses an application-oriented approach for qualification, the focus is primarily on the general method of an application specific qualification independent of a single stress test. Especially, for SiC power devices higher dynamic stress conditions occur due to the fast switching of such kind of devices compared to Si. Therefore, specific investigations are necessary to evaluate the dv/dt robustness of SiC power devices under dynamic conditions.

Introduction

The objective of this publication is to provide useful definitions and procedures for evaluating the dv/dt robustness of SiC-based power electronic conversion semiconductor (PECS) devices like SiC MOSFETs and Diodes.

GUIDELINE FOR EVALUATING DV/DT ROBUSTNESS OF SiC POWER DEVICES

(From JEDEC Board Ballot JCB-22-38, formulated under the cognizance of the JC-70.2 Subcommittee on SiC Power Electronic Conv. Semiconductor Standards.)

1 Scope

The scope of this document covers SiC-based power electronic conversion semiconductor (PECS) devices as SiC MOSFETs and Diodes.

This document provides stress procedures, general failure criteria and documentation guidelines such that the dv/dt robustness can be demonstrated, evaluated and documented. This document gives examples for test setups which can be used and the corresponding test conditions. Additionally, criteria are explained under which device manufacturers can select an appropriate test setup.

Furthermore, for the evaluation the test setups are usually used under normal laboratory conditions. The usage of the test setups is not limited to specific environmental conditions like high humidity for instance. But it would have been taken into account that additional failure modes like corrosion might be initiated.

2 Normative references

JEDEC JESD94B, *Application Specific Qualification Using Knowledge Based Test Methodology*, October 2015.

JEDEC JESD24-7, *Commutating Diode Safe Operating Area Test Procedure for Measuring DV/DT During Reverse Recovery of Power Transistors*, October 2002.

3 Terms and definitions

DUT	Device under test
I_{DSS}	Drain source leakage current
I_{GSS}	Gate source leakage current
R_{dson}	Drain source on-resistance
V_{br}	Breakdown voltage
V_f	Diode forward voltage
V_{th}	Threshold voltage
V_{SD}	Body diode forward voltage