

JEDEC PUBLICATION

Survey On Latch-Up Testing Practices and Recommendations for Improvements

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SURVEY ON LATCH-UP TESTING PRACTICES AND RECOMMENDATIONS FOR IMPROVEMENTS

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Introduction

This white paper reports on a survey that has been conducted to better understand how the latch-up standard JESD78 revision E (JESD78E) is interpreted and was used in the industry. It also lays a path for potential adaptations needed to accommodate its use in future technologies and applications. This executive summary provides a high-level overview of the key findings of the survey analysis and recommendations for future JESD78 improvements. It serves explicitly as an invitation to read further clauses of this report and analysis details.

NOTE At the time of the survey the standard JESD78E was in effect. After the close of the survey JESD78F was released. JESD78F is a largely rewritten version of JESD78E but the basic testing strategy of the test method is unchanged. While a few issues involved in this survey were addressed in JESD78F there is no reason to believe that the results of this survey would be substantially different if JESD78F were in force at the time of the survey. In this white paper, references to the “current”, “present”, or “existing” JEDEC standard are referring to JESD78E unless otherwise specified.

The survey was set-up to answer high level questions such as:

- How is the test standard interpreted and executed across the industry?
- Which real-life events does JESD78 intend to simulate? Do these occur in present day applications?
- The prescribed voltage compliance limits prevent any significant current injection for low voltage pins. Is that intended and/or desired?
- Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
- What changes should be made to the standard to better suit the reality of present day and future technologies and products?

The survey was divided into nine clauses, each addressing sub-topics like the ones listed above. More details on the structure of the survey are provided in [Clause 4](#) of this report.

[Clause 5](#) describes the analysis of the responses. An effort was made to address topics in the same sequence as the questions appeared in the survey. The analysis is meant to strictly report and summarize the information provided by the respondents and to find potential correlations between different topics. However, whenever the analysis team felt it was appropriate to offer a “possible interpretation”, it was clearly indicated using a special box format with the disclaimer that other interpretations would be possible. The full survey and an overview of all responses are provided in [Annex B](#) and [Annex C](#), respectively.

The conclusions and recommendations are provided in [Clause 6](#). Some of the key results are summarized below. For a full understanding of the survey results, it is recommended to read the full report.

One of the most relevant questions is if JESD78 latch-up testing ensures robustness of products in the field. Related key findings are:

- JESD78 is considered useful and should not be removed.
- It is evident that passing JESD78 testing is insufficient to guarantee latch-up robustness in the field, as shown in Figure 1, and seems to be more related to the type of stress rather than the levels.
- Respondents see value in JESD78 testing for modeling real world stress events beyond the specified test conditions.

Introduction (cont'd)

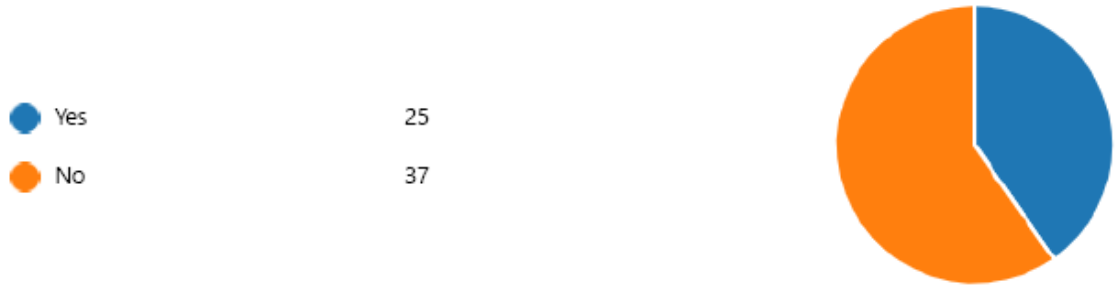


Figure 1 — Pie Chart of [Q41]

[Q41] “Does passing JESD78 testing guarantee latch-up robustness in the field?”

Another major topic is the assessment how large the latch-up problem is in practice. The figures below show at what step latch-up was detected (Figure 2), what the root causes were (Figure 3) and how often such cases lead to re-spins (Figure 4).

Examples of key findings related to this are:

- Figure 2 shows the majority of latch-up fails are reported during the JESD78 qualification test and many of these fails result in a re-spin, but this accounts for a very small fraction of the total number of re-spins as shown in Figure 4.
- More than 50% of all latch-up failures (field + JESD78 testing) do not require a re-spin, but the failure drives alternative mitigations such as board modifications or software changes

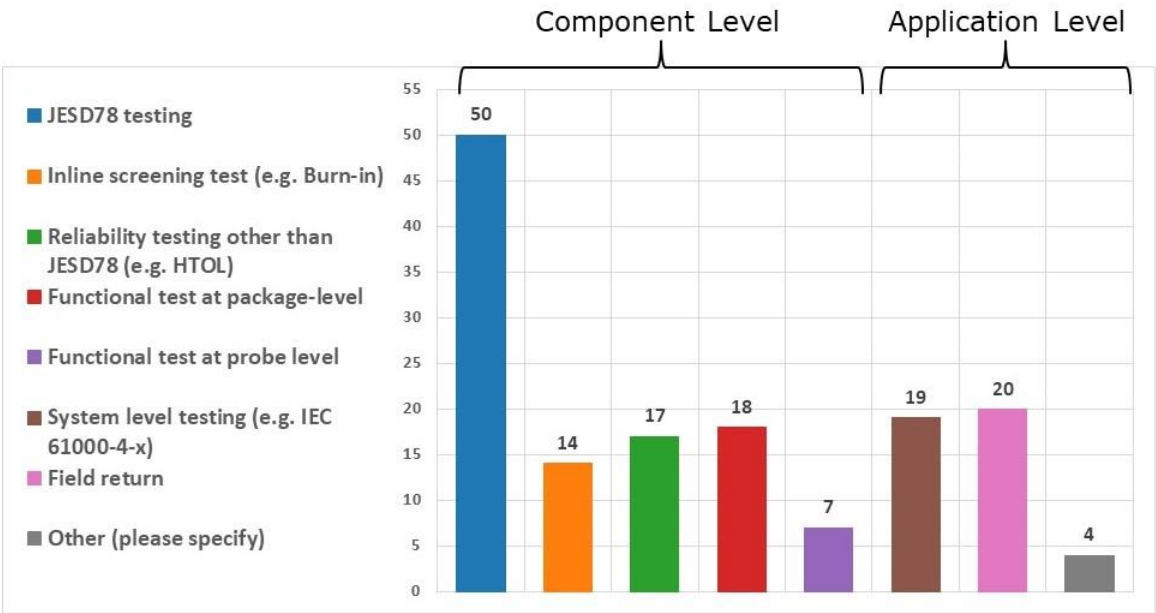


Figure 2 — Feedback to [Q12], in the Case Where [Q11], Was Answered “Yes”

[Q12] “Where have you experienced latch-up failures?”

[Q11] “Have you experienced latch-up failures?”

Introduction (cont'd)

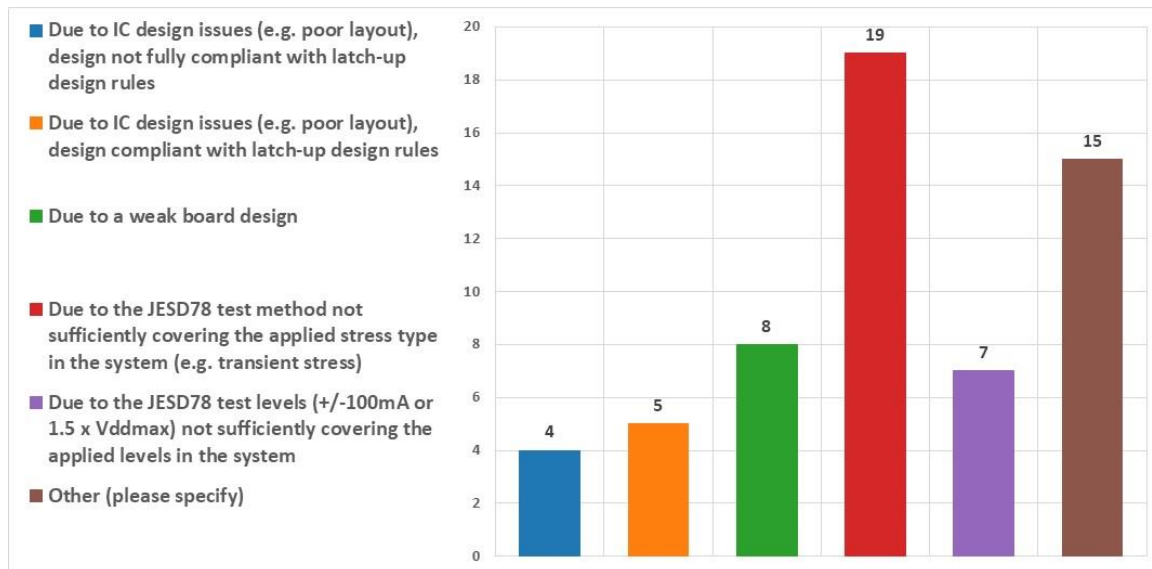


Figure 3 — Pareto of [Q20]

[Q20] “For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?”

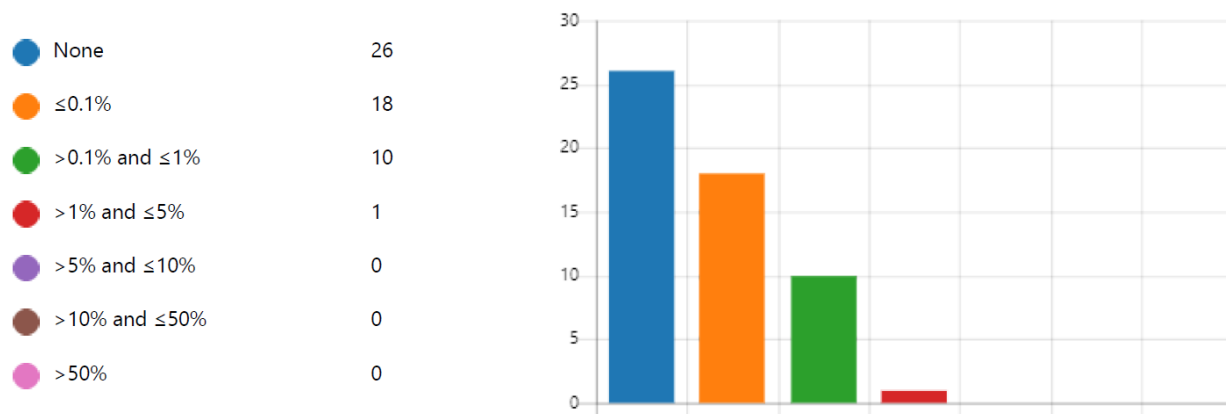


Figure 4 — Pareto of [Q21]

[Q21] “What percentage of your company's product re-spins were due to latch-up failures in a system application?”

The last highlighted topic is the question if the standard is sufficiently clear. It appears that some concepts in the standard are not interpreted in the same way by all users and sometimes are even used incorrectly. The most important examples are:

- The concept of the “Maximum Stress Voltage” is commonly used in the industry but very often misinterpreted or incorrectly applied to JESD78 testing.
- Many respondents believe that the pin stress voltage should not exceed the product AMR, see Figure 5.

Introduction (cont'd)

- Yes, if damage occurs while exceeding the AMR, it is not a latch-up failure
- No, the AMR is not applicable to latch-up testing

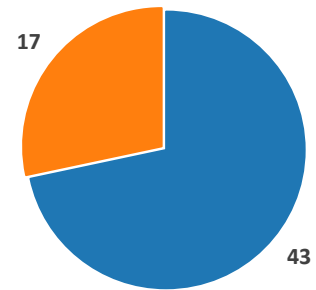


Figure 5 — Pie Chart of [Q90]

[Q90] “Do you set the pin stress voltage limits so that they do not exceed the product AMR?”

Key recommendations for possible improvements and extensions of JESD78E are listed below. Some of them may reach beyond the JESD78 specification – they may appeal to other industry bodies, symposia, trainers, vendors, etc. A more comprehensive list of recommendations is given in [Clause 6.3](#).

- Create a JESD78 user guide with practical explanations, hints, and examples.
- Provide seminars and workshops aligned with the latest JESD78 revision F release, discussing the major changes from JESD78 revision E and implications to LU testing.
- Consider ways to standardize LU testing at the application level (System Level ESD, Transient LU).

[Clause 6.4](#) concludes the white paper with a summary of the major differences between JESD78 revision E and JESD78 revision F.

SURVEY ON LATCH-UP TESTING PRACTICES AND RECOMMENDATIONS FOR IMPROVEMENTS

(From JEDEC Board Ballot JCB-22-57, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This white paper presents the results of a latch-up survey on JEDEC JESD78E conducted by the Industry Council on ESD Target Levels. Results of the survey are presented with interpretation of the results along with recommendations for future revisions of JEDEC JESD78. In this white paper, references to the “current”, “present”, or “existing” JEDEC standard are referring to JESD78E unless otherwise specified.

2 References

- [1] <https://www.esdindustryCouncil.org/ic/en/documents>
- [2] B. L. Gregory and B. D. Shafer, “Latch-Up in CMOS Integrated Circuits”, IEEE Transactions on Nuclear Science, Volume: 20, Issue: 6, pp 293-299, 1973
- [3] R. R. Troutman, “Latch-up in CMOS Technology”, Springer-Verlag, 1986 (2nd edition in 2012)
- [4] https://www.jedec.org/document_search?search_api_views_fulltext=jesd78
- [5] J. Salcedo-Suner et al., ‘A new I/O signal latch-up phenomenon in voltage tolerant ESD protection circuits’, Proceedings of the International Reliability Physics Symposium Proceedings, 2003, pp. and Jorge Salcedo-Suner et al., "Latch-up in voltage tolerant circuits: a new phenomenon", Microelectronics Reliability, vol. 44, pp. 549, 2004
- [6] <https://www.surveymonkey.com/>

3 Terms and Definitions

AEC	Automotive Electronics Council
ATE	automated test equipment
CDE	cable discharge event
CDM	charged device model
CMOS	complementary metal-oxide semiconductor
CFOM	correlation figure of merit
DPI	direct pin injection
DUT	device under test
EDA	electronic design automation
EIPD	electrically induced physical damage
EIAJ	Electronic Industries Association of Japan
EFT	electrical fast transient
EOS	electrical overstress
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association; EOS/ESD Association, Inc.
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
GPIO	general purpose I/O
HBM	human body model
HDMI	high-definition multimedia interface
HTOL	high temperature operating life
IC	integrated circuit
IDD	positive supply current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
I/O	input/output
IP	intellectual property
ISO	International Organization for Standards
JEDEC	JEDEC Solid State Technology Association
JEITA	Japan Electronics and Information Technology Industries Association
LDO	low-dropout
LU	latch-up
LV	low voltage
NPN	negative-positive-negative (transistor)
OEM	original equipment manufacturer
PCB	printed circuit board
PNP	positive-negative-positive (transistor)
PNPN	positive-negative-positive-negative (thyristor)
QBS	qualification by similarity
RF	radio frequency
SoC	system on a chip
SEL	single event latch-up
TLP	transmission line pulse
TLU	transient latch-up
USB	universal serial bus
VCC, VEE	voltage applied to the collector and emitter, respectively (bipolar BJT)
VDD, VSS	positive voltage supply and negative (or GND) voltage supply, respectively (MOSFET)

3 Terms and Definitions (cont'd)

absolute maximum rating (AMR): The maximum limit for either the voltage across, the current through, or the power dissipated in a device which causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.

maximum operating voltage (MOV): The maximum voltage allowed during normal operation of the device which still meets all data sheet specifications, typically including the DC/AC tolerance of the power supply.

maximum stress voltage (MSV): The maximum voltage (duration dependent) allowed to be placed on a given pin *during latch-up immunity testing* without causing irreversible damage to the device from a permanent physical breakdown of the silicon device or circuit not related to latch-up.

NOTE 1 A positive MSV is higher than the maximum operating voltage and a negative MSV is lower than the minimum operating voltage.

NOTE 2 MSV is NOT the same as the absolute maximum voltage rating (AMR) from the device datasheet. MSV applies to latch-up testing only, protecting the DUT from physical damage from stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in non-latch-up induced catastrophic breakdown of the silicon device/circuit.

NOTE 3 MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. In many medium and high voltage designs, MSV is very rarely the same value as AMR.

NOTE 4 The MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should consider the pulse width as well as process technology and circuit topology.

.

4 Latch-Up Characterization

4.1 Short Introduction to Latch-Up and Standards Timeline

After publishing white papers [1] on target levels for [human body model \(HBM\)](#), [charged device model \(CDM\)](#), [system level electrostatic discharge \(ESD\)](#), and the elimination of MM testing, the Industry Council on ESD Target Levels recognized the effectiveness of this organization for addressing fundamental reliability issues facing the electronics industry. This led to the publication of a white paper on [Electrical Overstress \(EOS\)](#) which has brought increased clarity to the understanding of EOS and the need for cooperation between suppliers and users of integrated circuits for understanding the causes and solutions to EOS issues. In light of these successes, the Council has addressed the issue of latch-up and latch-up testing by performing a survey of industry experience with latch-up and latch-up testing. This white paper is a report on the finding of that survey.

Latch-up, which is the triggering of a parasitic low-ohmic path between power supply rails that can either damage the integrated circuit (IC) or make the IC inoperable, has been described since the late 1960s [2]. Latch-up became a reliability concern in the mid-80s [3], leading to the first standard document JESD17. The first practical industry IC latch-up testing method with injection current requirement, JESD78, was published in the mid-90s by JEDEC and has been revised five times by the JESD78 Working Group (see Figure 6) [4]. Subsequent revisions brought improvements, clarifications, and different trigger conditions, as illustrated in Figure 6.

At the time this survey was conducted, latch-up standard JESD78E was in effect and used for most latch-up testing. However, JESD78F was in the ballot process at that time. JESD78F was approved and issued in early 2022. JESD78F is a substantial rewrite of JESD78E intended to make the standard easier to understand and deal with the challenges of applying latch-up testing to a wide variety of integrated circuits functioning over a wide range of voltages. It is important to understand however that the basic latch-up testing requirements in JESD78F are fundamentally the same as in JESD78E. In this white paper, references to the “current”, “present”, or “existing” JEDEC standard are referring to JESD78E unless otherwise specified.

4.1 Short Introduction to Latch-Up and Standards Timeline (cont'd)

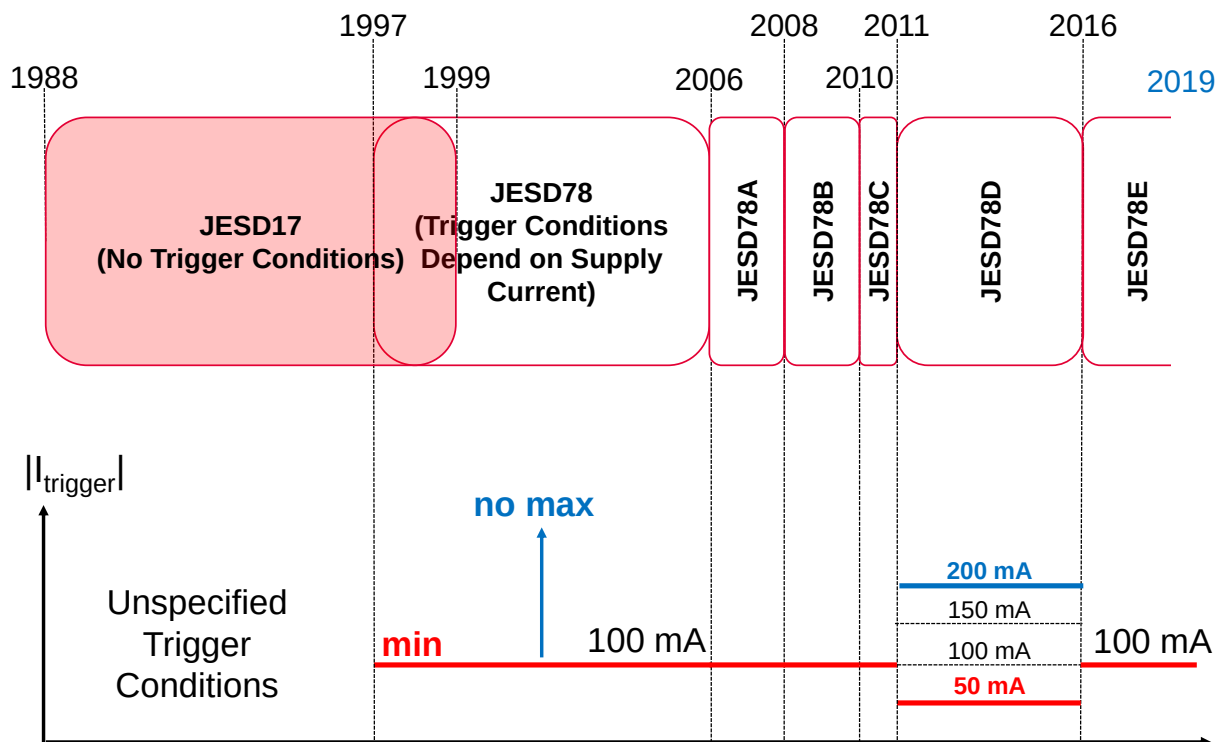


Figure 6 — Latch-up Testing Method Revisions and Associated Current Injection Requirements

The I/O test method essentially tests latch-up robustness by trying to inject a ± 100 mA current with a clamping voltage applied to the pin. This will lead to substrate currents that may, for example, trigger a parasitic thyristor in an I/O or an internal buffer, as illustrated in Figure 7.

For various reasons, including technology scaling, increasing amounts of integration, and the complexity and variety of semiconductor components, the standard has faced challenges addressing the needs of the increasingly diverse semiconductor product space. Some of those challenges include:

- It is unclear how this test method correlates to real threats.
- Lack of data to show that the same standard applies under all applications.
- Challenge of testing a wide range of integrated circuit working voltages.
 - In many low-voltage I/O cases, the current injected in the I/O is very limited.
 - Avoiding overstress for high voltage devices.
- Many technicalities can disqualify a result. Examples are the active state of the device under test (DUT), the definition of special pins and power supply instability.
- There is confusion about the method and its results. Examples are the required temperature setting, the definition of low-dropout (LDO) pins, and the use of the maximum stress voltage (MSV).

4.1 Short Introduction to Latch-Up and Standards Timeline (cont'd)

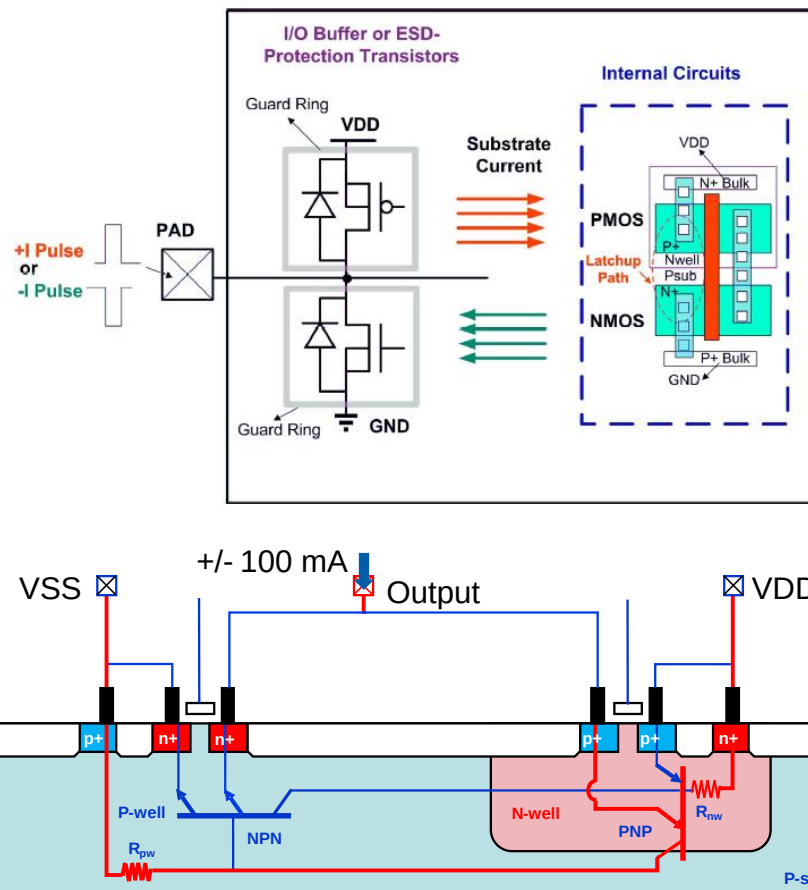


Figure 7 — Example of I/O Test with Cross-Section of Parasitic Thyristor in CMOS Buffer

4.2 Survey Report Organization

These challenges have prompted the industry Council on ESD Target Levels to re-evaluate the existing latch-up standard, JESD78E, in today's context. Throughout this document definitions of terms like e.g., injection current and MSV, are used as described in JESD78E. To understand more on how the industry is dealing with the topic and to get more information on how the industry uses latch-up testing results and to understand what industry expects from latch-up testing, the Industry Council on ESD Targets has set up a concise, yet detailed survey. A full version of the survey is available in [Annex B](#).

4.2 Survey Report Organization (cont'd)

Some of the major questions that this survey is trying to answer include:

- How is the test standard interpreted and executed across the industry?
- Which real-life events does JESD78 intend to simulate? Do these occur in present-day applications?
- Why does the test specify ± 100 mA for I/O assessments? Are the recommended qualification levels appropriate? Does a uniform specification make sense?
- The prescribed voltage compliance limits prevent any significant current injection for low voltage pins. Is that intended and/or desired?
- The formal latch-up definition describes parasitic thyristors. Should latch-up testing only be concerned about that? What about latch-up of other structures under the same conditions?
- Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
- What changes should be made to the standard to better suit the reality of present day and future technologies and products?

The survey was created by a sub-team of the Industry Council on ESD Targets and made available online for anonymous responses. The survey was announced via publicity channels of the Industry Council on ESD Targets, ESDA, JEDEC, JEITA, and an article in In Compliance Magazine.

The goal of this survey is to provide clarification on the test execution and use of the testing results and to derive recommendations, based on the data collected from a wide audience, for future directions of the JESD78 standard and potentially other standards. The data analysis and the recommendations are presented in this report. The response summary is available in [Annex C](#).

For better readability, Clause 5 (“[Detailed Analysis of the Survey](#)”) is split into different parts. We do this by following the same order of individual clauses as used in the survey, which is:

1. Affiliation and Background
2. Case Studies and Field Returns
3. Goal and Testing Strategy
4. Next Steps of Latch-up Testing
5. Reporting and Design Rules
6. Test Execution Details
7. Maximum Stress Voltage
8. Failure Criteria
9. Conclusion

In some cases, the feedback and result of a question are given descriptively (“high-level”). But in some other cases, we bring the analysis one level further as one important aspect of this survey analysis was finding meaningful correlations between answers to certain questions. This approach is described in detail in Annex A [Clause A.2](#) and is used throughout this document. The method provides the possibility to make statements like:

- Respondents who answered “<answer text x>” to [Qxx] were more likely to answer “<answer text y>” to [Qyy] (<Nx> % versus <Ny> % baseline).
- Respondents who answered “<answer text x>” to [Qxx] were more likely to agree/disagree with the following statement, “<statement derived from [Qyy]>” (<Nx> % versus <Ny> % baseline).

4.2 Survey Report Organization (cont'd)

Through such correlations, it is possible to check the data for consistency, but also work out information that is not obvious at first glance and identify relevant coherences and implications. This helps enormously to better understand how users interpret, apply, and use JESD78 testing.

NOTE Whenever we refer to a specific question in this document, we use the term [Q?]. Here, “?” represents the number of the question according to its listing in the survey (e.g.: [Q11] relates to question “11” in the survey, which is “Have you experienced latch-up failures?”)

[Clause 6](#) then summarizes the findings and provides recommendations for future work.

5 Detailed Analysis of the Survey

5.1 Affiliation and Background

This part of the analysis deals with the responses to [Q01] through [Q08] of the survey, which are:

- [Q01] Which company do you represent?
- [Q02] In which country are you working?
- [Q03] Which market segments does your company serve?
- [Q04] What type of business is your company?
- [Q05] Which IC product types do you support?
- [Q06] How many latch-up related customer complaints does your company receive per year (approximate number)?
- [Q07] Are you filling out the survey for the whole company or just a part of it?
- [Q08] Which aspects of the JESD78 test standard are you familiar with?

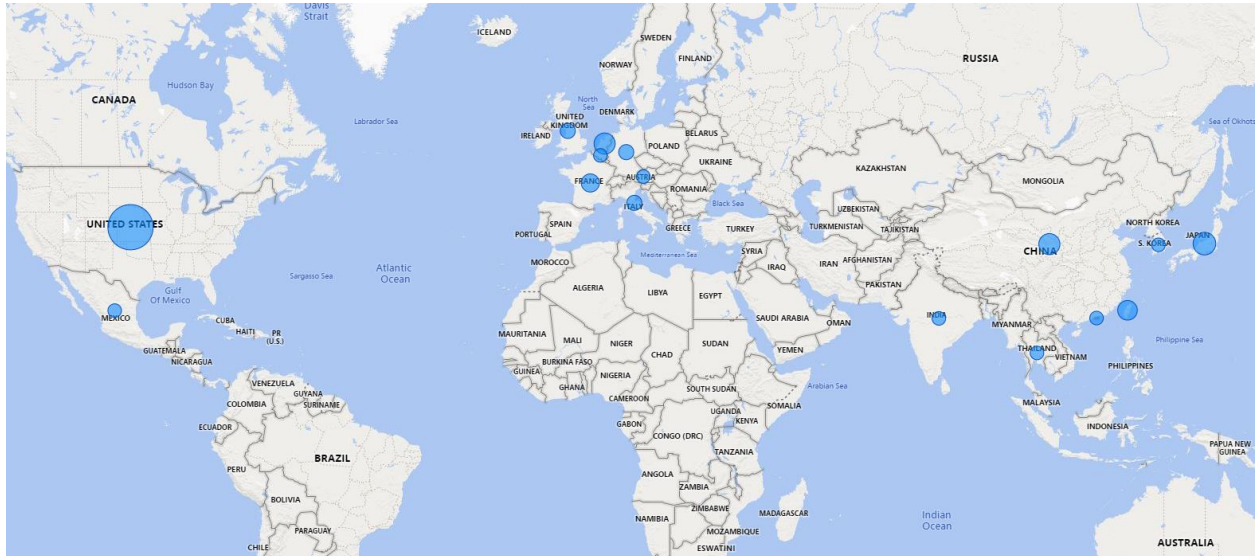
5.1.1 Demographics and Response Numbers

This clause describes important aspects of the responses to the survey, such as the number of responses, the distribution over different fields of the industry, the geographical distribution, etc. This serves to get an impression of how well the responders represent the industry.

The Industry Council on ESD Targets received 70 individual responses, from at least 35 companies from more than 16 countries. As we explain in detail in Annex A [Clause A.1](#) (Statistical Meaning), the number of 70 responses let us claim the data of the survey has statistical relevance and is meaningful to derive conclusions and recommendations for the future of latch-up testing in the industry.

The distribution around the globe and different regions is illustrated by Figure 8 and Figure 9. Multiple responses per company were encouraged because of the wide diversity of products, customers, and requirements. This makes it likely that even within one company, different approaches to latch-up testing may be used. Figure 10 shows that most responses received are representing relatively large groups or whole companies, while about 20% of the responses are on an individual basis.

5.1.1 Demographics and Response Numbers (cont'd)



NOTE The size of the balls is an indication of the number of responses from a country.

Figure 8 — Global Distribution of Responses

Responses according to regions

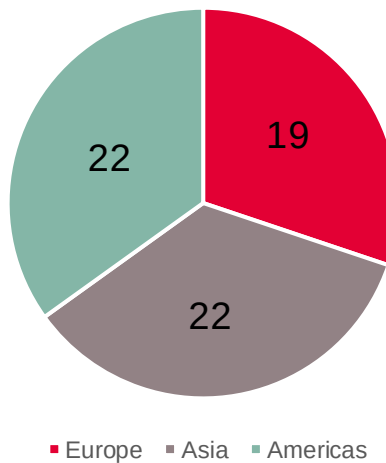


Figure 9 — Pie Chart of Responses Assigned to Different Regions

5.1.1 Demographics and Response Numbers (cont'd)

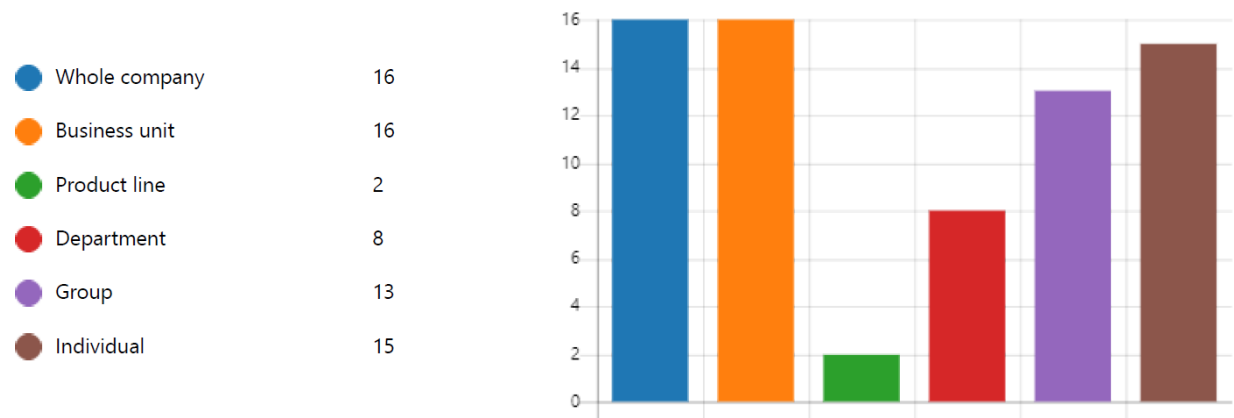


Figure 10 — Pareto of Group Representation per Response Received [Q07]

[Q07] “Are you filling out the survey for the whole company or just a part of it?”

5.1.2 Distribution Over Type of Market Space/Business/Application

Figure 11 and Figure 12 show the distribution of the responses over the type of business and type of IC respectively. The highest number of responses are from the category “IC Supplier with Fab”. Although the responses were obviously not evenly distributed, Figure 13 illustrates that the overall industry is well covered. The exceptions are OEMs using analog and respondents from the “Tier/subsystem” category using very low voltage ICs.

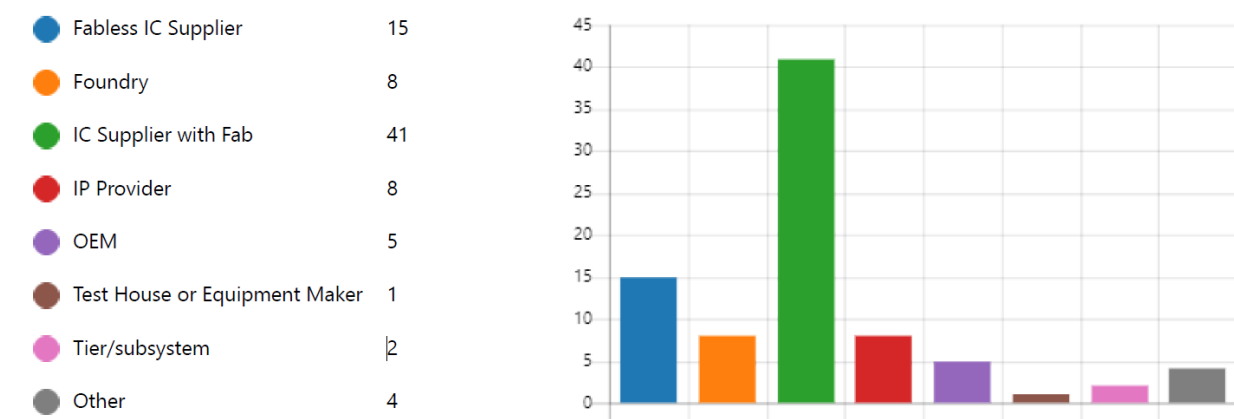


Figure 11 — Pareto of Responses Across Business Type [Q04]

[Q04] “What type of business is your company?”

5.1.2 Distribution Over Type of Market Space/Business/Application (cont'd)

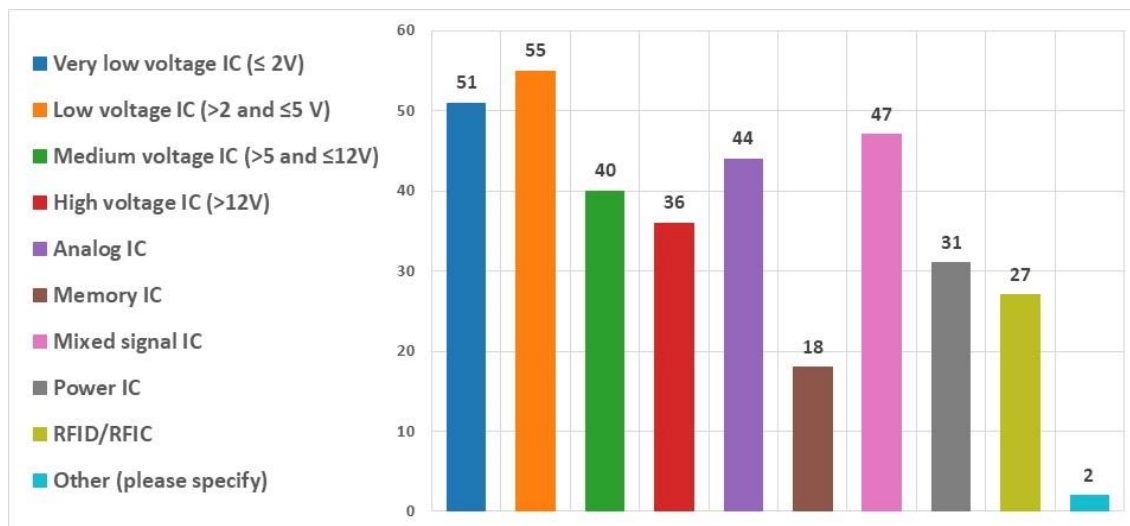


Figure 12 — Pareto of Responses Across Product Type [Q05]

[Q05] “Which IC product types do you support?”

	Very low voltage IC ($\leq 2V$)	Low voltage IC (>2 and $\leq 5 V$)	Medium voltage IC (>5 and $\leq 12V$)	High voltage IC ($>12V$)	Analog IC	Memory IC	Mixed signal IC	Power IC	RFID/RFIC	Other (please specify)
Fabless IC Supplier										
Foundry										
IC Supplier with Fab										
IP Provider										
OEM										
Test House or Equipment Maker										
Tier/Subsystem										

NOTE A green filled cell indicates that this combination of the type of business and IC product type is covered by at least one response in the survey.

Figure 13 — Combination of Responses from [Q04] and [Q05].

5.1.2 Distribution Over Type of Market Space/Business/Application (cont'd)

Finally, Figure 14 shows that the respondents are primarily active in the Automotive, Consumer, and Industrial market segments. The other market segments combined make a comparable contribution to the responses. In [Clause 5.2](#), selected questions will be analyzed for possible correlations with business type or market segments.

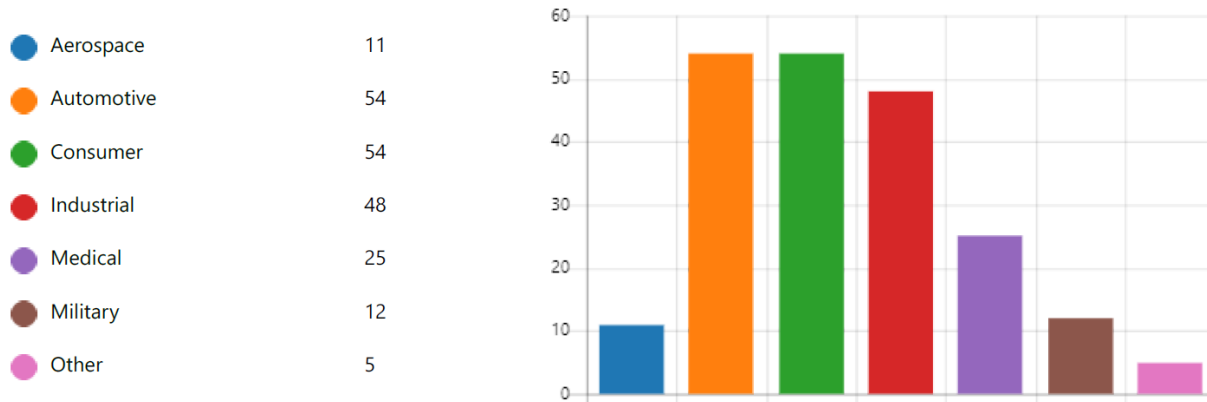


Figure 14 — Pareto of Responses Across Market Segments [Q03]

[Q03] “Which market segments does your company serve?”

5.1.3 Familiarity of the Industry Community Concerning the Different Aspects of Latch-Up Testing According to JESD78

To assess the significance of responses, it is relevant to have a general impression of how familiar the respondents are with the different aspects of latch-up testing. In general, the JEDEC JESD78 standard can be divided into different clauses, starting with "Immunity levels classification", "Detailed test procedure", and "Pass / Fail criteria" up to the more specific clauses like "Special Pins", "Maximum Stress voltage" and "Reporting Requirements".

[Q08] was designed to gauge the familiarity of the survey participants with the different aspects of latch-up testing. To do this [Q08] simply asked if the survey participants were familiar with the following aspects of latch-up testing:

- Pass/Fail criteria
- Immunity levels classification
- Detailed test procedure
- Special pins
- Reporting requirements
- Maximum stress voltage (MSV)

The general familiarity of the industry community with latch-up testing could then be gauged by the percentage of participants that agreed they were familiar with each of the aspects of latch-up testing listed above. The results are shown in Figure 15, first considering all 70 responses by the community.

5.1.3 Familiarity of the Industry Community (cont'd)

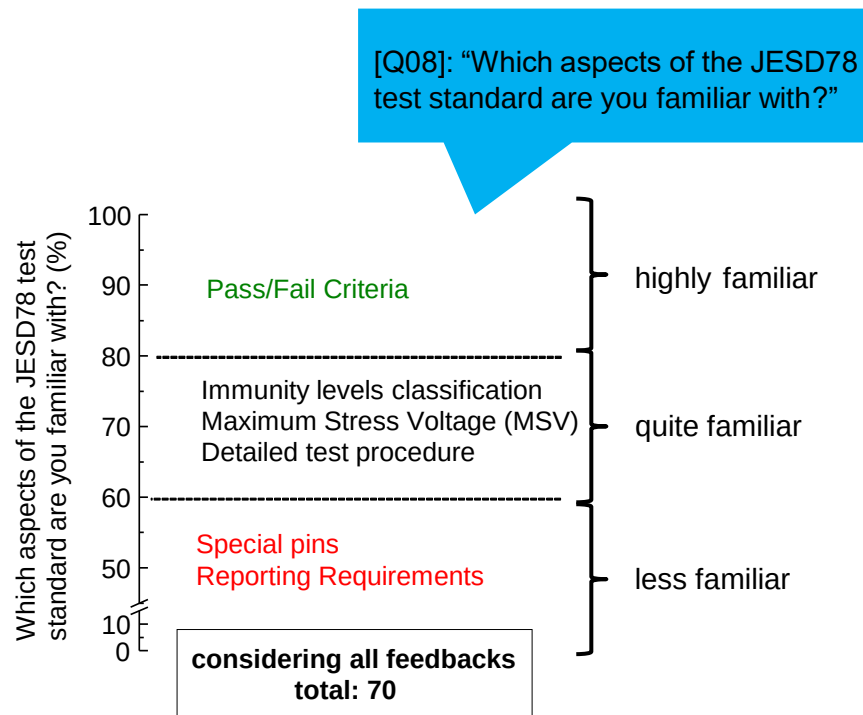


Figure 15 — Responses Regarding the Familiarity of Different Clauses of the Latch-up Standard [Q08], Considering all Feedback.

[Q08] "Which aspects of the JESD78 test standard are you familiar with?"

To better classify the data, three categories were created, and correspondingly sensible levels were introduced, which then map to the degree of familiarity with individual clauses: from "highly familiar" (agreement of 100% - 80% of all participants in the survey) to "quite familiar" (80% - 60%) down to "less familiar" (< 60%). Accordingly, almost 90% of all participants (and thus practically everyone) were familiar with handling the "Pass / Fail Criteria", the highest value reported here. In the areas of "Immunity levels classification", "Detailed test procedure" and "Maximum stress voltage (MSV)", familiarity has decreased with 70% agreement in the middle ("quite familiar"). In the areas of "Special Pins" and "Reporting Requirements", the level continues to slide, so that only every second participant states that they are very familiar with the requirements of the corresponding clause in the standard.

Knowing the complexity and scope of the latch-up standard, this question was re-evaluated, but now only for those respondents who have given feedback for a company as a whole. It is undisputed that the topic of latch-up is multifaceted, starting with topics relating to the derivation of protective measures against latch-up within the scope of product design, the implementation, and organization of latch-up tests, through to the subject of field relevance and field returns. In this context, field returns refer to returned goods following production release at the corresponding level of integration. We have assumed that respondents who overlook the entire process and cycle are much more familiar with the individual clauses of the latch-up standard.

5.1.3 Familiarity of the Industry Community (cont'd)

We now demonstrate the change of the previous results (Figure 16), but now focusing only on feedback given by survey participants responding for a company as a whole.

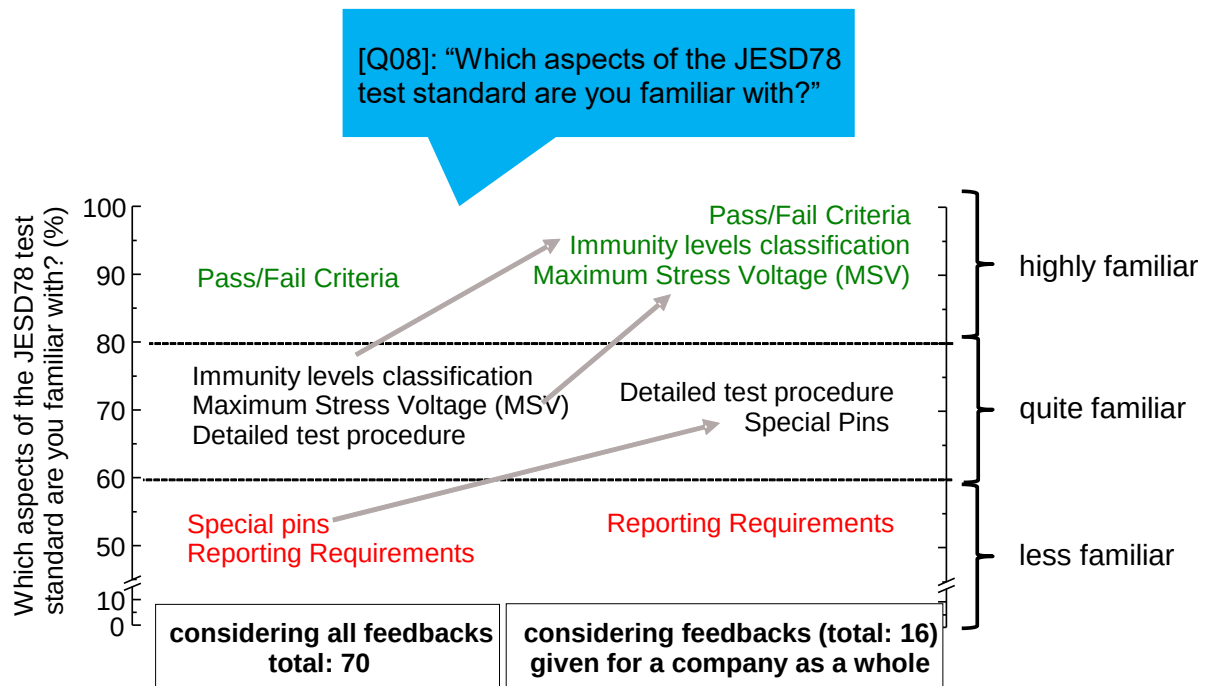


Figure 16 — Change in the Distribution of Responses Regarding the Familiarity if Restricted to Respondents Giving Feedback for a Company as a Whole.

A clear trend can be perceived and confirms the hypothesis made above. For this group of respondents, confidence in the knowledge of the relevant clauses of the standard is higher in all areas. In return, however, this means that colleagues who only have an overview of part of the latch-up value chain, have a greater need for training or clarification.

Finally, taking any of the different aspects ("Pass/Fail Criteria", "Immunity levels", "MSV", "Detailed test procedure", "Special Pins", "Reporting Requirements"), it becomes apparent that it is more or less always the same group consisting of Tier, OEM and "Other" that respond to be less familiar with each particular topic (see Figure 17). In contrast, the IC Supplier and Test House groups seem to have a good understanding. They deal with these issues "naturally" more often than other comparison groups and are trained accordingly. It is relevant to note that this trend is unique regardless of which of the potential answers to the base [Q08] "Which aspects of the JESD78 test standard are you familiar with?" is considered for correlating the data.

5.1.3 Familiarity of the Industry Community (cont'd)

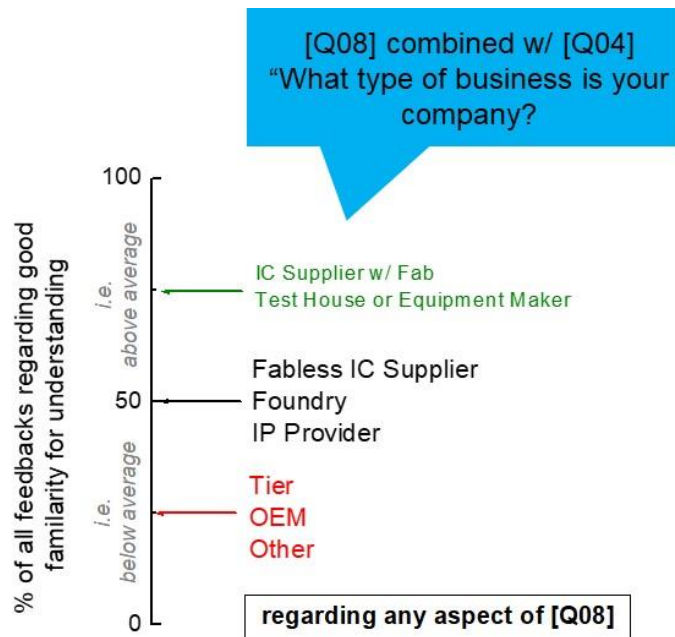


Figure 17 — Taking Any Aspect of the JESD78 Standard Like “Pass/Fail criteria” or “Reporting Requirements” and Correlating to the Type of Business [Q04]

5.2 Case Studies and Field Returns

This clause is dedicated to the survey responses on JESD78 latch-up test implementation, failures, and root causes. Particular topics that will be discussed include questions on return rates, expected field issues prevented by meeting JESD78 requirements, coverage of real-life threats, etc. This part of the analysis deals with the responses to [Q09] through [Q22] of the survey, which are:

- [Q09] Do you think that the JESD78 standard is useful to prevent system failure caused by overcurrent or overvoltage in real world scenarios?
 - [Q10] Please provide examples of the above reply
- [Q11] Have you experienced latch-up failures?
 - [Q12] If yes, where have you experienced latch-up failures?
- [Q13] Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?
 - [Q14] If yes, were the actual stress levels reported to the customer?
 - [Q15] If yes, did that part have any latch-up related field returns?
 - [Q16] If yes, please specify approximate return rate
 - [Q17] If yes, were there any measures taken at the board/system level to mitigate the latch-up risk (e.g., add board-resistor, etc.)?
 - [Q18] If yes, please describe the measures taken
- [Q19] For products that have had latch-up failures in the system, what were the conditions needed to replicate the failure?

5.2 Case Studies and Field Returns (cont'd)

- [Q20] For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?
- [Q21] What percentage of your company's product re-spins were due to latch-up failures in a system application? (Discussed in [Clause 5.3.1](#))
- [Q22] Has your company experienced EIPD (electrical induced physical damage) related to latch-up with parts that passed JESD78 testing at the semiconductor supplier? (Discussed in [Clause 5.4.3](#))

5.2.1 Failure Rates

To get an impression of the occurrence rates of problems at the end-customer side, several questions were included in the survey. As a first high-level question, the number of latch-up related customer complaints (returns) was requested. 58 respondents provided an answer, the results of which are shown in Figure 18. The overwhelming majority receive very few customer complaints per year.

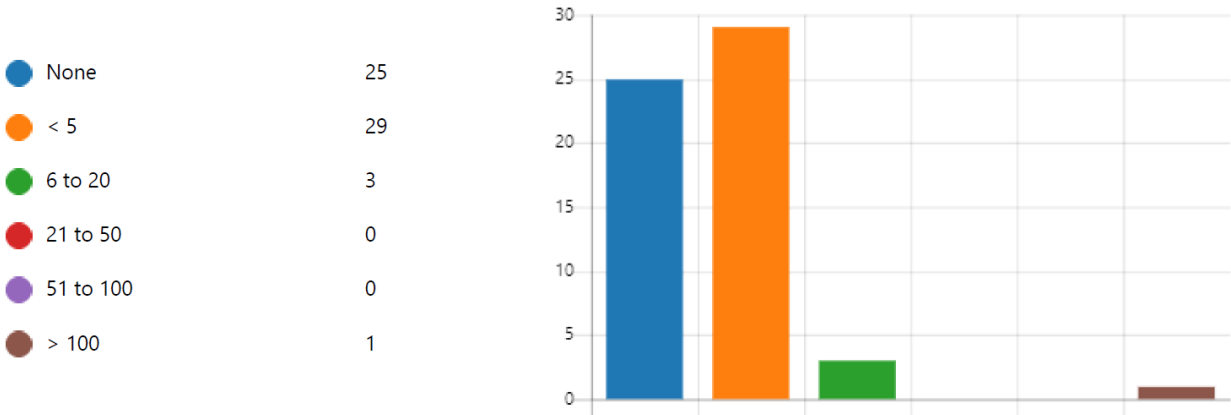


Figure 18 — Pareto of [Q06]

[Q06] “How many latch-up related customer complaints does your company receive per year (approximate number)?”

To better understand what the contribution of JESD78 testing is in preventing customer complaints, a series of questions dives deeper into the testing results.

[Q11] through [Q17] investigate different ways to look at failure rates. From the response on [Q11] “Have you experienced latch-up failures?” we learn that the vast majority (59 out of 69 respondents, 85%) of the respondents have experienced latch-up failures. When asked where failures were observed, 85% of the respondents include JESD78 testing, but 60% include a situation that can (only) occur in the final application and/or at the location of the customer. Looking at it another way, 25% exclusively list JESD78 testing, whereas only single responses exclusively list situations that can be done by the customer. This is discussed in more detail in [Clause 5.2.3](#). From [Q13] “Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?” we learn that immunity level B qualification is used by about 50% of the respondents, see Figure 19, and most of them use it for both voltage and current. In most of these cases, the actual stress levels are shared with the customer. Follow-up questions did not lead to a conclusion on increased failure rates: 1 out of 24 had field returns, but without any measure taken to mitigate it. 17 out of 24 did not get any field returns, while for 6 it was too early to tell.

5.2.1 Failure Rates (cont'd)

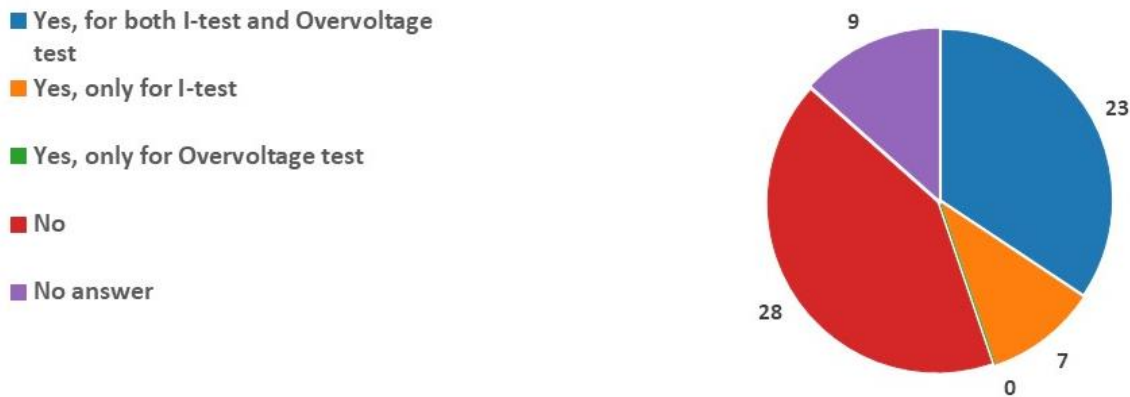


Figure 19 — Pie Chart of [Q13]

[Q13] “Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?”

Next, the survey addresses in [Q19] how the failure could be replicated. The five main categories are surprisingly evenly distributed in the answers of 59 respondents, as shown in Figure 20. Forty out of those responding provided a single answer and this distribution is shown in the small inset. The distribution is very compatible with the overall distribution. The “Other” category showed very diverse answers, however about 1/3 of those entries were related to the stress pulse. Respondents used non-default pulses to trigger the latch-up event: longer or shorter pulses, special system-level pulses, or ESD pulses. All other answers were combinations of the pre-defined answers, but each of these combinations occurred only once or twice. The combination that occurred most was “Within maximum operating conditions per datasheet specification” combined with “With System level stress testing (e.g., IEC 61000-4-x)”.

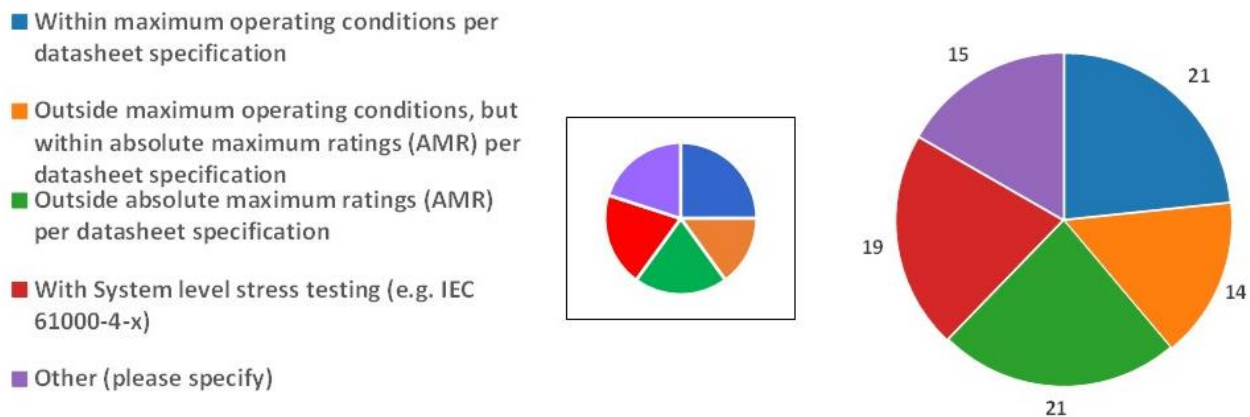


Figure 20 — Pie Chart of the Distribution of the Replication Methods [Q19]

[Q19] “For products that have had latch-up failures in the system, what were the operating conditions needed to replicate the failure?”

5.2.1 Failure Rates (cont'd)

[Q20] asked about failure root causes for products that had passed JESD78 testing. The raw distribution is provided in Figure 21. After analyzing the “Other” category it can be concluded that the main root causes of failures while passing JESD78 are:

1. Issues with standard not addressing the phenomenon (54%)
2. Issues with board design (19%)
3. Issues with IC design (16%)

This indicates that the most common problem is that JESD78 does not address a significant category of real-life stresses that can bring an application into latch-up attributed to fast events, like system level ESD stress and fast power-up situations for example. As indicated by the purple bar in Figure 21 it is generally not a matter of the levels being too low. A minority of IC design-related latch-up problems are not caught by the current way of JESD78 testing. Board issues cannot be expected to be caught by an IC level test.

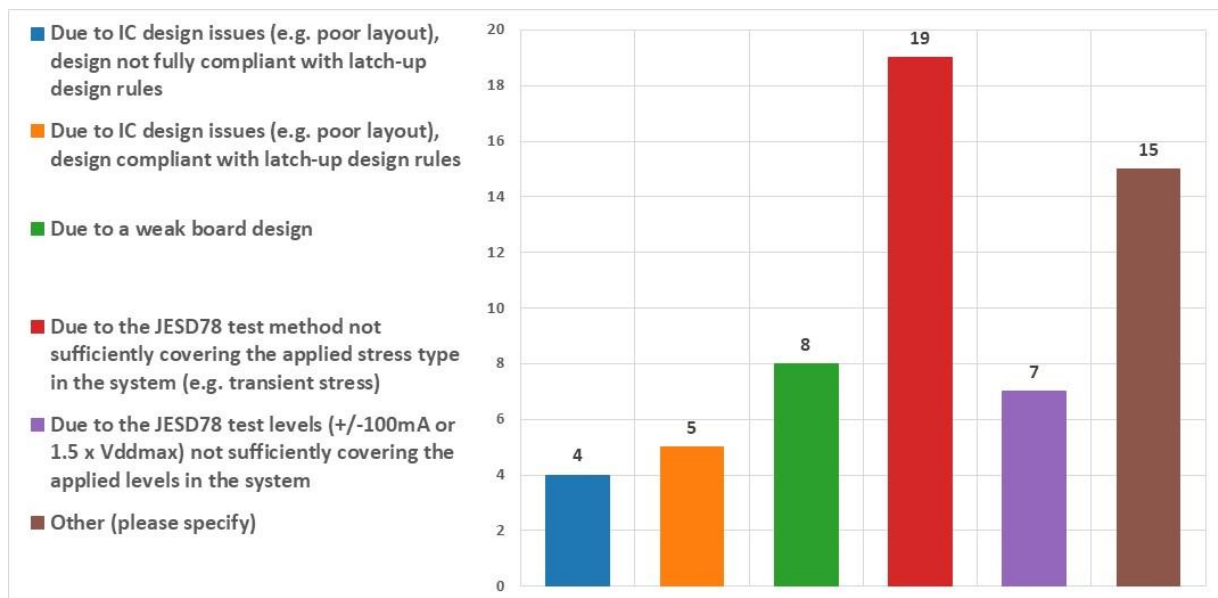


Figure 21 — Distribution of Responses for [Q20]

[Q20] “For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?”

5.2.2 Latch-up Testing vs. Real-World Latch-up Failure Scenarios

It is evident that the main motivation for performing a latch-up qualification on semiconductor products is to check the conformity of the individual IC pins regarding the occurrence of latch-up-related damage in specific overcurrent or overvoltage situations. At this stage, we simply refer to the term "failure caused by latch-up" as the triggering of a low-impedance internal path between supply and ground in the IC.

5.2.2 Latch-up Testing vs. Real-World Latch-up Failure Scenarios (cont'd)

JESD78 describes a method for performing latch-up testing, including the specification of corresponding target values. The question now is to what extent this method and the requirements for overcurrent and overvoltage described therein are sufficient and complete. Complete in the sense that all situations that occur in reality, i.e., in the field, regarding overvoltage and overcurrent are covered. Ideally, applying the JESD78 standard within the scope of a latch-up product qualification could then prove that the IC reacts robustly in its environment at any time and in any situation and does not suffer any damage with regard to latch-up-like phenomena.

As a first step, [Q12] is worked out to confirm that such “real” latch-up-like damage and situations do indeed exist (see Figure 22).

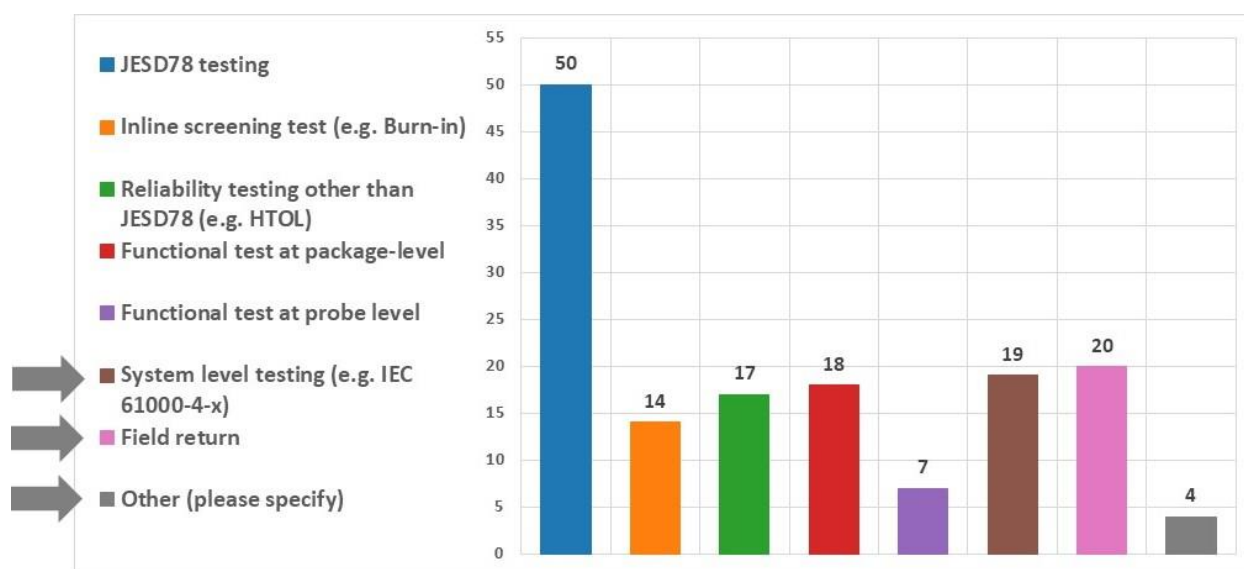


Figure 22 — Pareto of [Q12], in the Case Where [Q11] Was Answered “Yes”

[Q12] “Where have you experienced latch-up failures?”

[Q11] “Have you experienced latch-up failures?”

The term “real-world scenarios” is used here to summarize the areas “System Level Testing”, “Field Returns” and “Others”. According to the evaluation, for each category, there is definitely corresponding feedback on occurrences available.

To what extent the JESD78 standard has been useful to prevent system failure caused by overcurrent or overvoltage in real-world scenarios is addressed in [Q09] and the results are shown in Figure 23.

5.2.2 Latch-up Testing vs. Real-World Latch-up Failure Scenarios (cont'd)

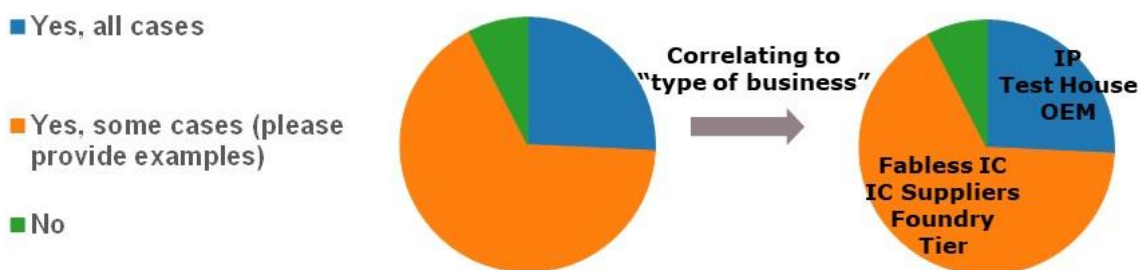


Figure 23 — Pie Chart to Visualize Opinion About [Q09] (Step 1) and Then Correlating Feedback to [Q04] (Step 2)

[Q09] “Do you think that the JESD78 standard is useful to prevent system failure caused by overcurrent or overvoltage in real-world scenarios?”

[Q04] “What type of business is your company?”

Almost 3 out of 4 of all respondents, and thus the vast majority of the participants in the survey, believe that the application of the JESD78 standard was not helpful in identifying all, but only some of the latch-up-type damage observed in the field. In reality, there exists many more latch-up-like failure scenarios that are not addressed by the JESD78 standard. Which specific scenarios that could be (for example transient-related latch-up stress or ESD system-level-related stress) will be dealt with in detail in a later part of the survey. Only about 1 out of 4 participants expressed that through testing according to JESD78, latch-up-like events in the field can be principally avoided.

With the help of the feedback to [Q04], and as shown in Figure 23 it is possible to find out who responded predominantly optimistically and who responded more pessimistically. For example, more than 65% of all respondents from Fabless IC companies, IC suppliers, Foundries, and Tier found that JESD78 would only catch some cases of latch-up susceptibility. In contrast, 75% of respondents from IP Suppliers, Test Houses, and OEMs had faith that JESD78 would find all latch-up susceptibility.

5.2.3 Experience of the Semiconductor Industry Concerning the Amount and Frequency of Latch-up Failures and their Root Cause

The question about the frequency of failures due to latch-up was asked twice. First with the background of how many times *per year* every single participant of this survey *currently* must deal with such an error pattern. This was addressed in [Q06] and the results are shown in Figure 24.

5.2.3 Experience of the Semiconductor Industry (cont'd)

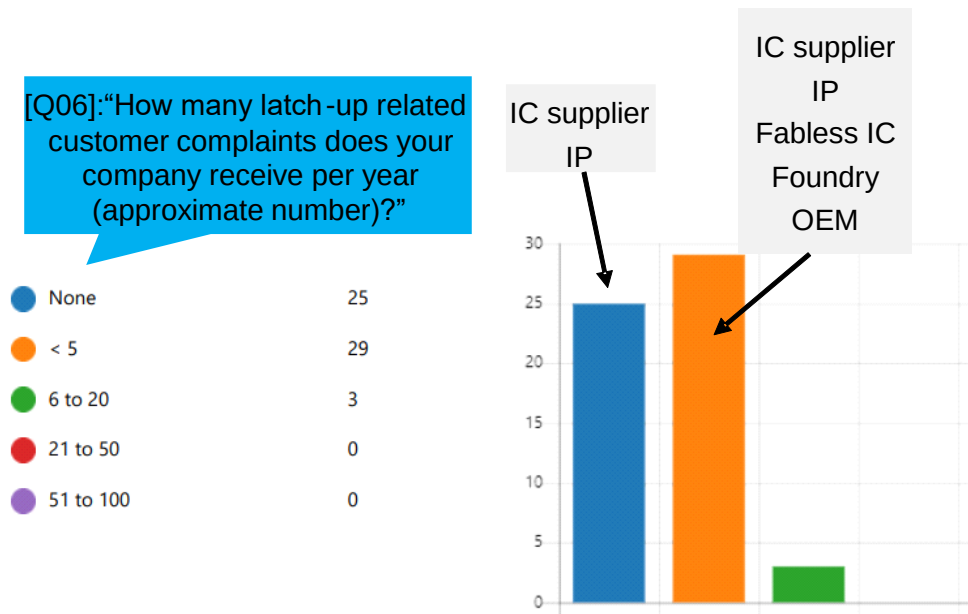


Figure 24 — Pie Chart of [Q06], and Correlating Feedback to [Q04]

[Q06] "How many latch-up related customer complaints does your company receive per year (approximate number)?"

[Q04] "What type of business is your company?"

The vast majority of the answers given are limited to the two options "no complaints" or "number of complaints < 5". The occurrence of higher failure rates is rarely reported. With the help of the answers to [Q04] "What type of business is your company?", it can be determined that it is fifty-fifty of the participants of the group "IC suppliers" and "IP providers" that report they either have no complaint or complaint rates below 5. On the other hand, more or less all participants from the areas of fabless IC, foundry, and OEM must deal with some small number of failures each year.

If one does not look at the current day-to-day business but asks whether there have been latch-up failures *in the past in general* ([Q11]), the following picture emerges in Figure 25.

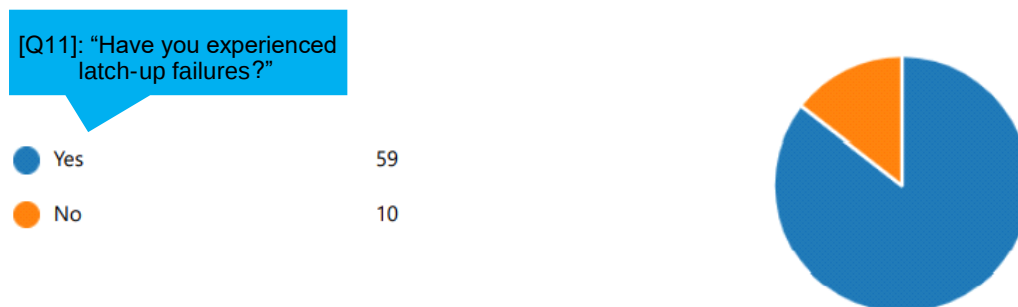


Figure 25 — Pie Chart of [Q11],

[Q11] "Have you experienced latch-up failures?"

5.2.3 Experience of the Semiconductor Industry (cont'd)

Accordingly, almost 85% of all participants of the survey had to deal with latch-up failures in the course of their work. The subject of latch-up failure is therefore present in all branches of the semiconductor industry.

Continuing by asking in which situations a latch-up failure occurred [Q12], the results are shown in Figure 26.

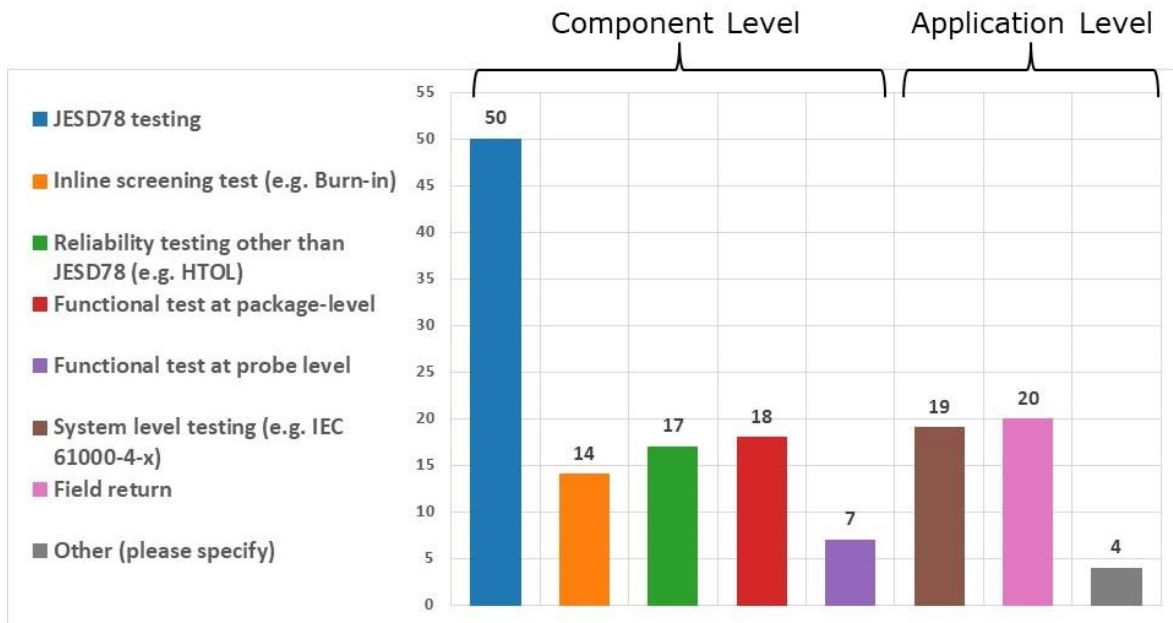


Figure 26 — Feedback to [Q12], in the Case Where [Q11] Was Answered “Yes”

[Q12] “Where have you experienced latch-up failures?”

[Q11] “Have you experienced latch-up failures?”

First of all, it is important to note that there was the possibility of submitting multiple answers to this question. For better orientation, it is marked additionally, whether the underlying failure situation appeared in a situation when the component was "isolated" or used in a system or application.

In this presentation and overview, the category "JESD78 testing" clearly dominates. About two-thirds of all participants have reported at least one latch-up-like failure during a latch-up qualification over the years. However, there are definitely further situations at the level of a single component or its use in the application (for example due to the use of additional test procedures such as screening or system level stress) that have led to a latch-up-like failure.

If one evaluates the data further, the dominance that it is precisely the class of JESD78 testing that rules the number of latch-up failures is lost! To do this, we take the number of responses that stated that they had ever had to deal with latch-up failures (59 in [Q11]) and divided them into these 3 categories, as shown in Figure 27.

- Exclusively fails from JESD78 testing ⇒ 13
- Fails from JESD78 testing and at least one other event ⇒ 38
- Latch-up failures but not caused by JESD78 testing ⇒ 8

5.2.3 Experience of the Semiconductor Industry (cont'd)

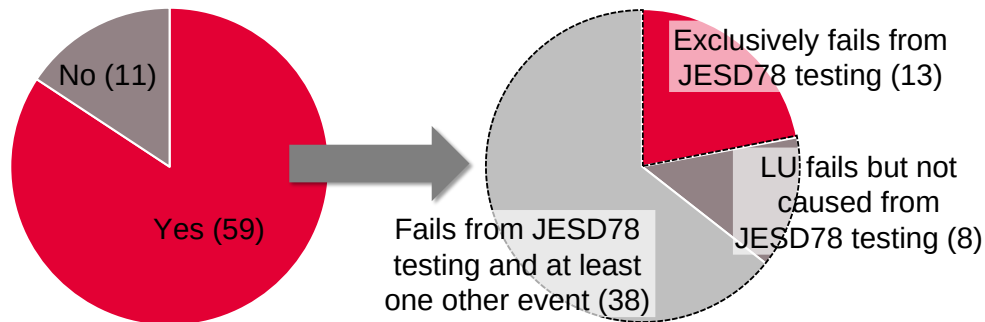


Figure 27 — Evaluation of [Q11], and in the Case of “Yes”, Identifying How Many Responses Saw Any Further Event Besides JESD78 Testing Mentioned.

[Q11] “Have you experienced latch-up failures?”

Only in 13 cases (22%), and thus for a smaller part of the participants, latch-up failures in the past were solely due to JESD78 testing. On the other hand, $8 + 38 = 46$ (78%) of the responses indicated that events other than JESD78 testing were also possible to explain latch-up damage in the past.

From this evaluation, one could conclude that it was indeed very likely that latch-up-like damage was not generated by JESD78 testing alone but popped up in a variety of other ways.

Finally, Figure 28 illustrates which business areas reported situations that led to a latch-up-like behavior. The participants from the “Fabless IC”, “Foundry”, and “IC Supplier” areas showed latch-up-like failures in all the areas listed. In the “IP Supplier” domain, the failures are limited to “Testing according to JESD78” and for OEMs to “System Level Testing” or “Field failure”.

5.2.3 Experience of the Semiconductor Industry (cont'd)

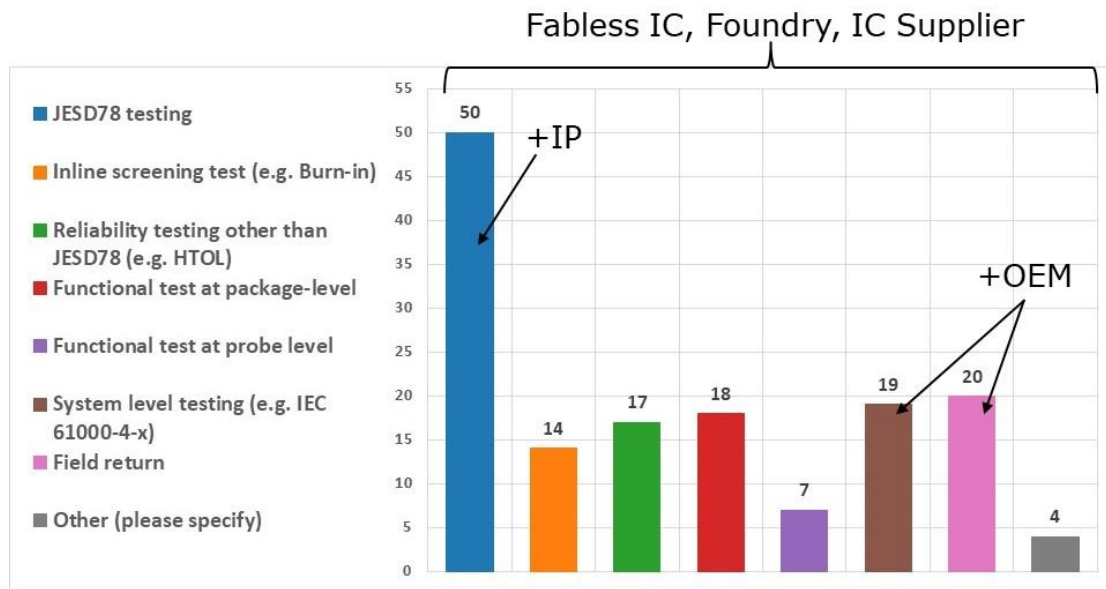


Figure 28 — Correlating [Q12], in the Case Where [Q11] Was Answered “Yes”, With [Q04],

[Q12] “Where have you experienced latch-up failures?”

[Q11] “Have you experienced latch-up failures?”

[Q04] “What type of business is your company?”

5.2.3.1 Further Observations and Implications for the Case Where Participants in the Questionnaire Indicated That They Have Had or Had Not to Deal with Latch-Up Faults at All.

From the deeper correlation analysis, interesting clues emerge as to how participants ...

- who have not previously had to deal with latch-up failures on their products, or
- who were facing latch-up issues during “System level testing (e.g., IEC 61000-4-x)” or “Inline screening test (e.g., Burn-in)”...

think about whether the JESD78 standard is sufficient to prevent latch-up failures in the field. First, the relevant data for the group of respondents having no latch-up problem in its overview is shown in Figure 29, Figure 30, and Figure 31.

5.2.3.1 Further Observations and Implications (cont'd)

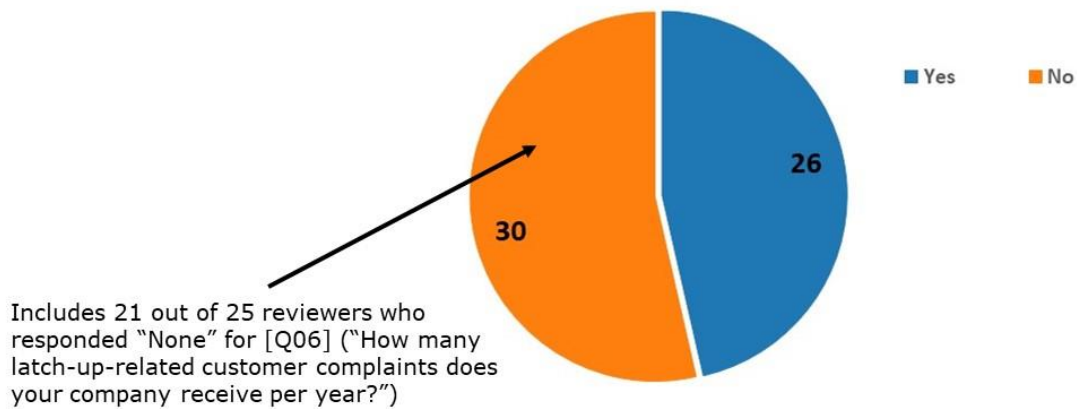


Figure 29 — Correlating Those Who Answered “No” for [Q49] With Those Choosing “None” as Feedback for [Q06]

[Q49] “Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?”

[Q06] “How many latch-up related customer complaints does your company receive per year (approximate number)?”

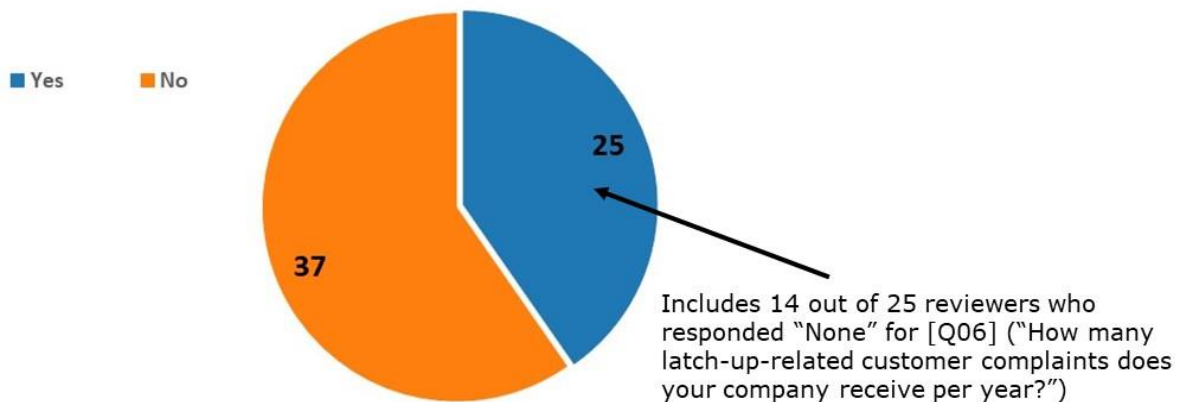


Figure 30 — Correlating Those Who Answered “Yes” for [Q41] With Those Choosing “None” as Feedback for [Q06]

[Q41] “Does passing JESD78 testing guarantee latch-up robustness in the field?”

[Q06] “How many latch-up related customer complaints does your company receive per year (approximate number)?”

5.2.3.1 Further Observations and Implications (cont'd)

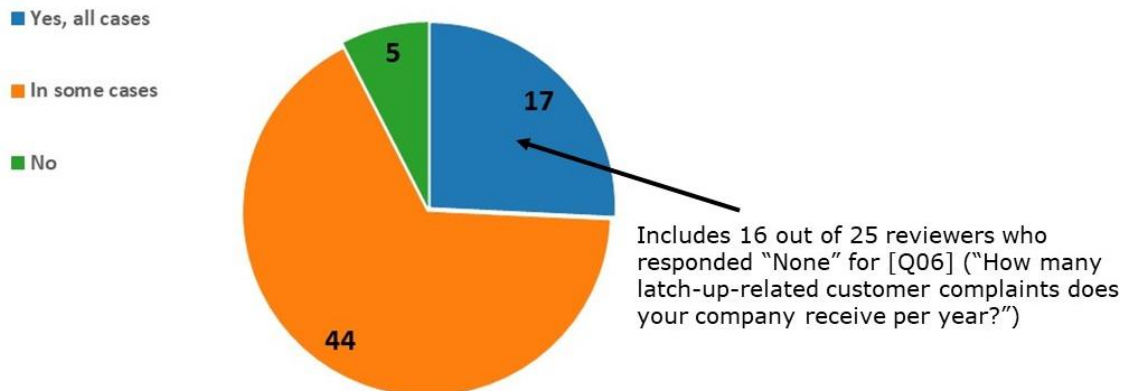


Figure 31 — Correlating Those Who Answered “Yes, All Cases” for [Q09], With Those Choosing “None” as Feedback for [Q06]

[Q09] “Do you think that the JESD78 standard is useful to prevent system failure caused by overcurrent or overvoltage in real world scenarios?”

[Q06] “How many latch-up related customer complaints does your company receive per year (approximate number)?”

From the standards point of view, it is good to learn that the group of respondents who have not previously been affected by any latch-up damage in the context of JESD78 testing or field returns are also convinced that the application of the JESD78 standard in effect when the survey was performed is perfectly sufficient to detect and avoid latch-up situations.

What is the mindset of respondents that had to deal with latch-up issues in the past caught during either “System level testing” or “Inline Screening test”? The results are shown in Figure 32.

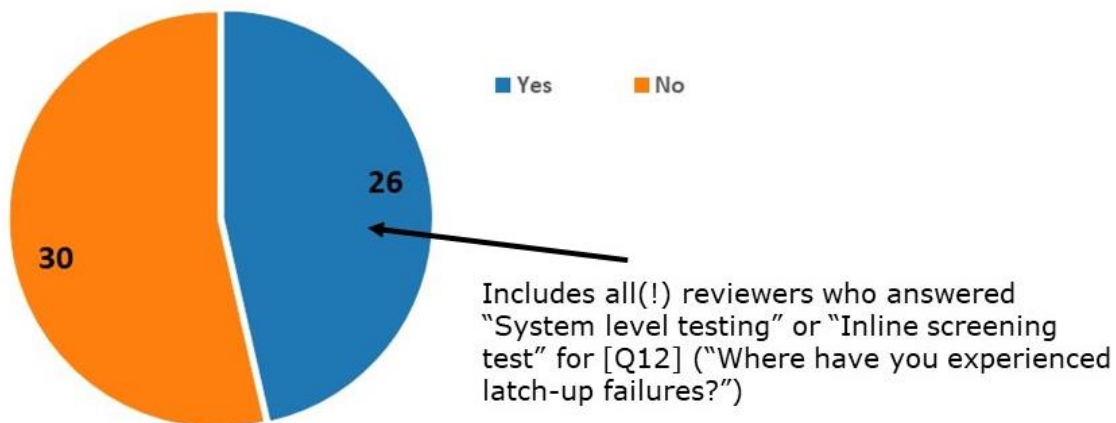


Figure 32 — Correlating [Q49] With Those Choosing “System Level Testing” and “Inline Screening Test” for [Q12]

[Q49] “Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?”

[Q12] “Where have you experienced latch-up failures?”

5.2.3.1 Further Observations and Implications (cont'd)

All(!) affected respondents choosing either “System level testing” or “Inline Screening test” suggested a need for a new test method that specifies generic current injection and voltage testing.

5.2.4 Qualification vs. Real Life

About half of the respondents (30) affirm that their companies are selling immunity level B components (either for current injection or overvoltage) according to [Q13]. However, 25 of them didn't get any latch-up related field return and just 1 declared to have failures without giving any rate. The remaining cannot report any data since the qualification is recent.

For products that have had latch-up failures in the system ([Q19]), conditions to replicate the failure can be grouped as “within AMR limits”, and “outside of AMR limits”. This grouping suggests that a number of latch-up failures lie within the testing range of JESD78 since the voltage limits specified by the standard and MSV values frequently exceed AMR values (see Figure 33).

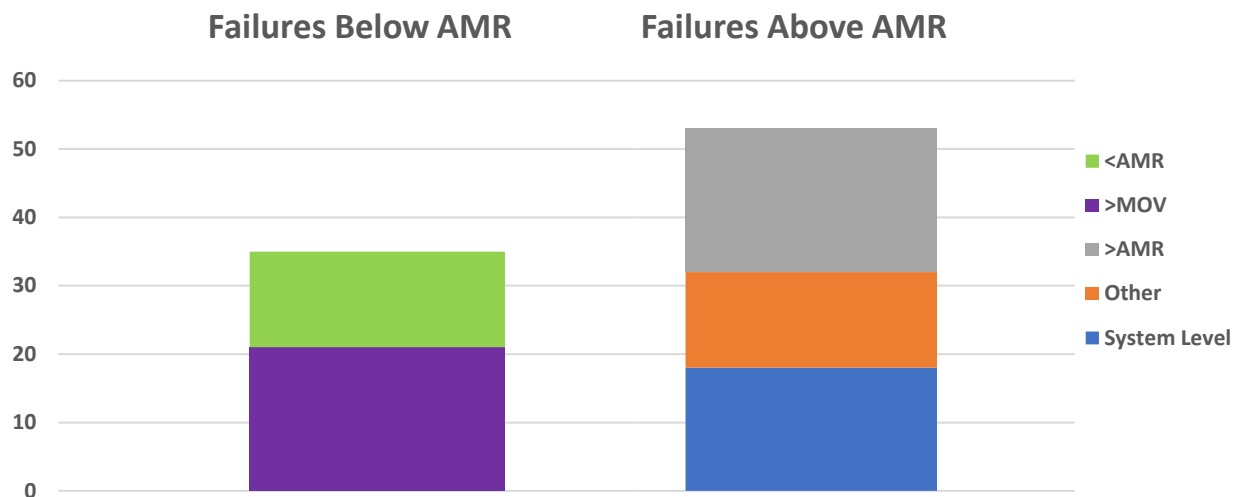


Figure 33 — Conditions to Replicate Failures in the System

For products that have had latch-up failures in the system, but had passed JESD78 testing ([Q20]), we can perform the same analysis grouping that results in:

- JESD78 not covering the applied stress (26)
- IC design issues (8)
- Board or Other issues (23)

Two main detractors are lack of JESD78 coverage and Board or Other causes.

This result is almost market, technology, and type of business independent, although all IC issues are related to companies that are dealing with Mixed Signal (8/8) and that are in Automotive (7/8) and Industrial (6/8) markets.

5.2.4 Qualification vs. Real Life (cont'd)

Latch-up is a mandatory qualification test ([Q23]) but for products that are offered in multiple packages that use the same die ([Q25]) half of the companies perform trials on all packages while half qualify their ICs by similarity regardless of market. Looking to company business, Fabless IC suppliers seem to prefer testing all packages (9/12) while IC Suppliers with Fab prefer qualification by similarity (20/31).

Possible Interpretation

This is not surprising because Fabless IC suppliers have less control on technology and maybe less products to compare having lower confidence level. Companies selling multichip products generally qualify them using the same strategy used for single die ICs.

In the same way, it is possible to roughly distinguish product types in two macro categories: technologies based on standard I/O cells (low or very low voltage, memories and radio frequency (RF)) or based on custom I/O cells (medium or high voltage, Analog, Mixed signal, and Power ICs); given this definition testing all packages is the preferred methodology for custom I/O designers while for the others both strategies are equally used ([Q25]).

Qualification strategies do not have any impact on either the latch-up experience ([Q11]) nor on where the latch-up has been detected ([Q12]).

5.3 Goal and Testing Strategy

This part of the survey addresses issues like “Reflecting latch-up Test Goals”, “latch-up test coverage vs. real world”, and “supplier latch-up reporting”. In particular, it is the response to [Q23] through [Q42] of the survey, which are:

Latch-up test goals:

- [Q23] Is JESD78 testing a product qualification requirement in your company?
 - [Q24] If only for certain product types, please specify
- [Q25] What is the JESD78 test requirement in your company for products that are offered in multiple packages that use the same die? (Discussed in [Clause 5.2.4](#))
- [Q26] What is the JESD78 test requirement in your company for Multi-Chip Products?

Occurrence rate of latch-up failures and consequences:

- [Q27] What percentage of your company's products has experienced latch-up failures (either in JESD78 qualification testing or in the field)?
- [Q28] What percentage of your company's product re-spins were due to failures during JESD78 qualification test?
- [Q29] What percentage of your company's product re-spins were due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?

Latch-up test coverage vs. real world:

- [Q30] What is the goal of the supply overvoltage test and I/O (signal pin) injection test in the present JESD78 standard?

5.3 Goal and Testing Strategy (cont'd)

- [Q31] Does the JESD78 testing address real world stress events like HBM and CDM do?
 - [Q32] If JESD78 testing were removed as a qualification requirement for the industry, what would happen?
 - [Q33] Please specify why

Latch-up reporting

- [Q34] Do you require detailed JESD78 information from an IC supplier?
- [Q35] Do you scrutinize the JESD78 information provided by an IC Supplier?
- [Q36] How are JESD78 test results provided in an IC Supplier datasheet or qualification report used for system design?

Modes and Test-Parameters considered for latch-up testing:

- [Q37] Would increasing the overvoltage or injection current levels of JESD78 decrease the latch-up failures in the field?
- [Q38] Is the operational state of an IC used during JESD78 testing (i.e., low power mode, stable current) representative of real-world applications?
 - [Q39] If not, please specify why not
- [Q40] If a product has multiple modes of operation, how does your company test for JESD78 latch-up?
- [Q41] Does passing JESD78 testing guarantee latch-up robustness in the field?
 - [Q42] If no, what other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?

5.3.1 Customer Complaints

In the next questions, we try to assess the magnitude of the latch-up problem in practical situations. Figure 34 shows the Pareto of the percentage of products that experienced latch-up failures, in qualification testing or the field.

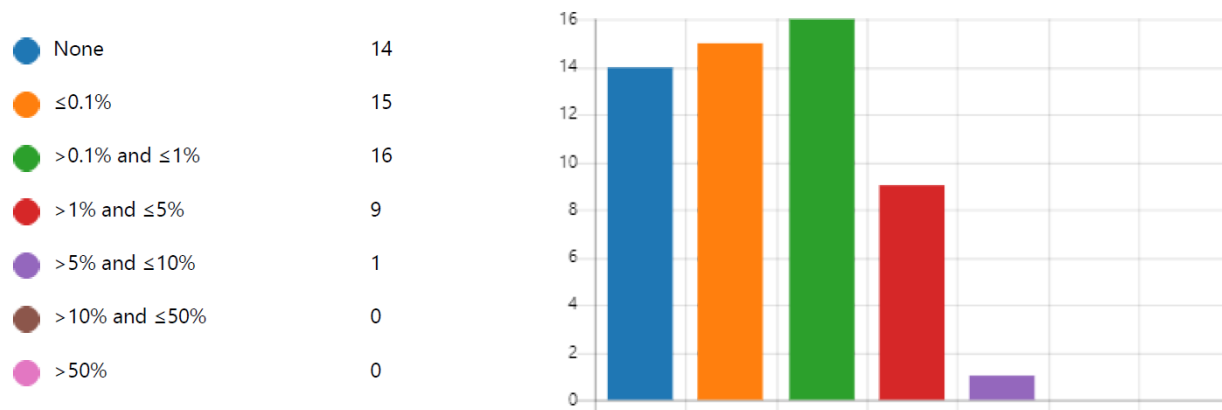


Figure 34 — Pareto of [Q27]

[Q27] “What percentage of your company's product has experienced latch-up failures (either in JESD78 qualification testing or in the field)?”

5.3.1 Customer Complaints (cont'd)

Next, it is time to look at re-spins resulting from latch-up related problems. Figure 35 shows a Pareto of the re-spin rates provided by the respondents. Roughly, 50% of the respondents do not have re-spins due to latch-up related problems. This can indicate that the problems can be solved in other ways, are not severe enough, or are not even reported.

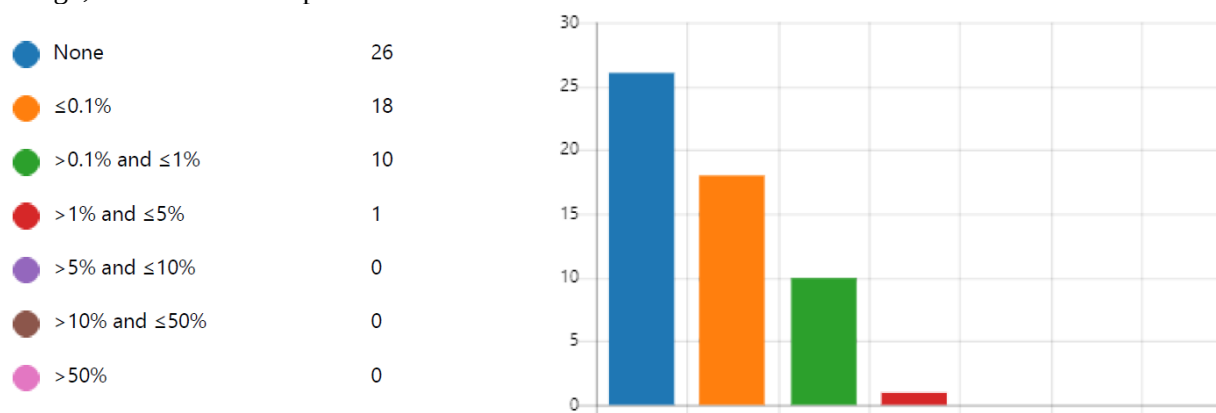


Figure 35 — Pareto of [Q21]

[Q21] “What percentage of your company's product re-spins were due to latch-up failures in a system application?”

Possible Interpretation

It is likely that for 50% of the LU related problems, options exist to solve the issue without an IC re-spin, for example, by software modifications or by changes on the application board.

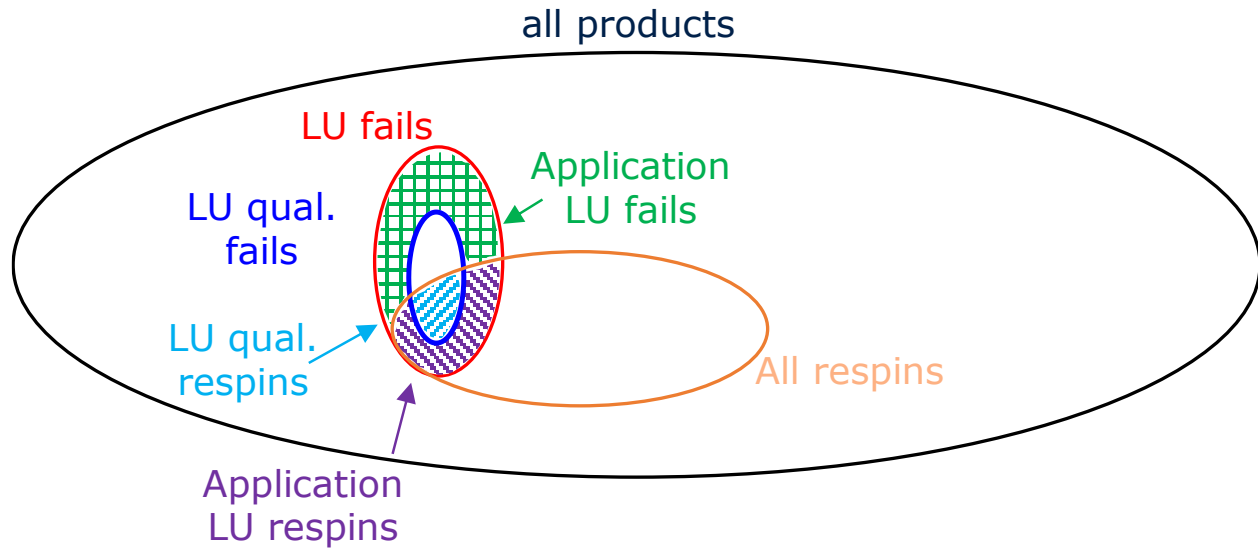
To get a numerical impression of the relationship between the questions related to returns and re-spins the following estimate may be useful. For each question, the sum of the upper limit of each interval times the number of responses for that limit is calculated and the result is divided by the total number of responses. This way a “weighted average” of the percentages serves as an estimate. The results are provided in Table 1. Based on these numbers the average system application latch-up re-spin rate is smaller than 0.3%. Similarly, a rough upper bound estimate for the average percentage of problematic products is 1.3%.

Table 1 — Calculated Estimates of Occurrence

Question	Weighted Average
[Q21] – re-spins after latch-up failures in system application	0.3%
[Q27] – latch-up failures in JESD78 & field	1.3%
[Q28] – re-spins after failure in latch-up qualification	0.6%
[Q29] – re-spins after latch-up failure not caught by JESD78	0.5%

5.3.1 Customer Complaints (cont'd)

From [Q28] and [Q29] we find that the distributions of latch-up related re-spins from qualification testing and application-related failure are almost identical. Figure 36 provides a graphical illustration of how the responses relate to each other.



NOTE All latch-up failures [Q27] comprise latch-up qualification failures and re-spins [Q28] and application testing latch-up re-spins [Q29] and failures [Q21] within the groups of all re-spins and products.

Figure 36 — Illustration of how the Responses to [Q28] and [Q29] Relate to Each Other

[Q28] “What percentage of your company's product re-spins were due to failures during JESD78 qualification test?”

[Q29] “What percentage of your company's product re-spins were due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?”

5.3.1 Customer Complaints (cont'd)

Figure 37 gives an example of how the occurrence of latch-up failures relates to re-spins resulting from qualification fails.

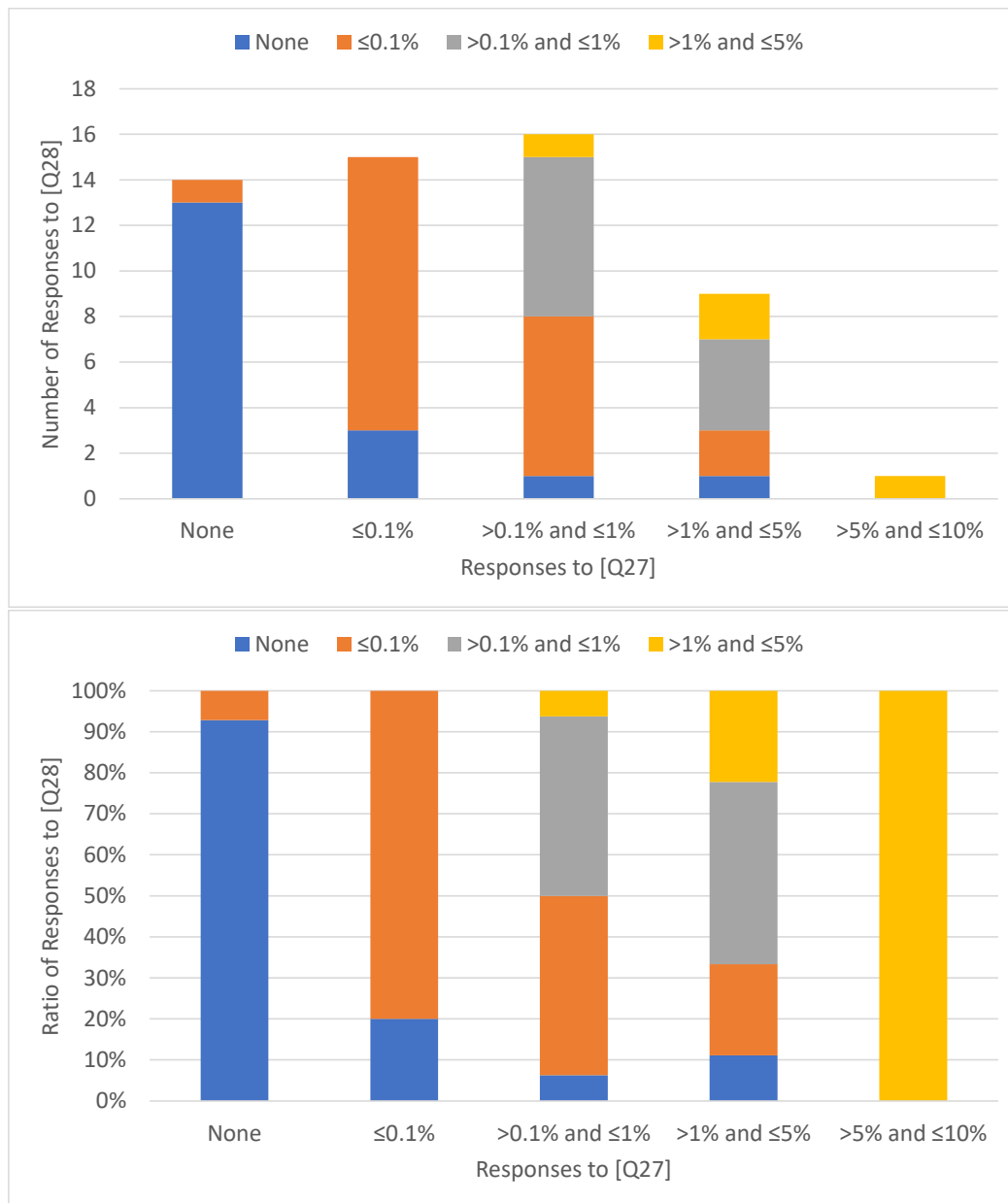


Figure 37 — Relationship Between [Q27] and [Q28] in Absolute Numbers (Top Graph) and Relative to the Number of Replies per Answer to [Q27] (Bottom Graph)

[Q27] “What percentage of your company's product has experienced latch-up failures (either in JESD78 qualification testing or in the field)?”

[Q28] “What percentage of your company's product re-spins were due to failures during JESD78 qualification test?”

5.3.1 Customer Complaints (cont'd)

Figure 37 shows some things that are unexpected (and may say something about accuracy). For example, the first column is about responders indicating “NO failures”. Yet at least one respondent is stating they did re-spins for latch-up. Therefore, further analysis was done.

Another way of looking at this data is the following. [Q27] asked for the percentage of products that had experienced latch-up failures (either in JESD78 qualification testing or in the field). Fourteen out of 55 respondents replied ‘None’. For consistency, it was verified that these respondents also replied ‘None’ to [Q21], [Q28], and [Q29]. For the respondents that replied with a percentage to [Q27], the responses to these questions are categorized in Table 2.

Table 2 — Categorization of Responses to Questions Related to Re-Spins

Base: [Q27] & replied with > 0%		
	# Of Responders Reporting Redesigns	# Of Responders Reporting No-Redesigns
[Q21] re-spins due to latch-up failures in a system application?	27	11
[Q28] re-spins due to failures during the JESD78 qualification test?	36	5
[Q29] re-spins due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?	22	17

This leads to the following observations:

- 2/3 of all participants reported having latch-up failures.
- In the case of latch-up failures detected during JESD78 testing, a significant majority of the products received a re-design.
- In the case of latch-up failures detected during reliability testing or system testing, only half of the situations were contained by re-designs.

The interpretation of the data is as follows: Generally, the number of re-spins is smaller than the number of failures (consistency check). But e.g., in the column “failures between 1% and 5%” there is only a small number of respondents saying that the percentage of re-spins is between 1% and 5%. This is an indication that latch-up failures do not automatically lead to re-spins and that re-spins (which are very costly for the suppliers) are under-represented.

This supports the claim that there are more ways to solve latch-up problems.