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Guideline for Gate Oxide Reliability and Robustness Evaluation Procedures for Silicon Carbide Power MOSFETs

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GUIDELINE FOR GATE OXIDE RELIABILITY AND ROBUSTNESS EVALUATION PROCEDURES FOR SILICON CARBIDE POWER MOSFETS

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Foreword

This document was drafted by the JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use by SiC product suppliers and related power electronic industries. It provides guidelines for evaluating gate reliability and lifetime testing for silicon carbide (SiC) based power devices with a gate oxide or gate dielectric. The information is for manufacturers of SiC power devices, for quality evaluation and lifetime prediction purposes.

Introduction

This document has the purpose of laying out generally acceptable practices for testing gate oxide reliability of silicon carbide (SiC) based power devices having a gate dielectric region involved in turning devices on and off. This typically refers to metal-oxide-semiconductor (MOS) devices such as capacitors, field-effect transistors (MOSFETs), or insulated-gate bipolar transistors (IGBTs). All presented examples are from MOS gated SiC devices. Specifically covered is time-dependent dielectric breakdown (TDDB) testing, with either constant-voltage stress (CVS), constant-current stress (CCS) or ramped voltage stress (RVS) / ramped current stress (RCS) for ramped breakdown (RBD) tests.

An issue related particularly to SiC substrates is their high defect density; which has been rapidly decreasing over time as substrate quality improves, but remains orders of magnitude higher than for silicon substrates. This, and the resulting high interface trap levels present at SiO₂/SiC interfaces, has in the past interfered with the understanding of the intrinsic properties of SiO₂ on SiC. Thus, in the testing guidelines presented here, the intrinsic properties of the oxides on SiC are themselves important to demonstrate/determine. Extrinsic failures can often be related to intrinsic material defects in the SiC wafer material, or to processing issues, and any mathematical treatment of extrinsic defects is beyond the scope of this document. For detailed analysis of early fail populations (See JESD74A). Of course, the testing recommended here is to allow determination of the intrinsic and extrinsic populations, specifically through analysis of the failure distributions. However, the reasons for extrinsic failures, and means to eliminate them, are not addressed here, but helpful experimental procedures to analyze extrinsic failures will be described.

GUIDELINE FOR GATE OXIDE RELIABILITY AND ROBUSTNESS EVALUATION PROCEDURES FOR SILICON CARBIDE POWER MOSFETS

(From JEDEC Board Ballot JCB-22-61, formulated under the cognizance of JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee.)

1 Scope

This document has two purposes; the first is presenting guidelines for the gate dielectric lifetime extraction and wear-out of MOS devices on silicon carbide substrates ("intrinsic behavior"). Specifically, it is designed for MOS devices (capacitors or transistors) where oxide thickness (t_{ox}) $\gg$ 10 nm. Therefore, 'soft' breakdown behavior is not expected to be observed, and oxide breakdown occurs instantaneously as a 'hard' breakdown event. Thus, issues relating specifically to thin oxides and soft breakdown are not addressed here. The second purpose is presenting guidelines for the measurement of gate dielectric breakdown, which are assumed to be defect related and occur much earlier than the wear out ("extrinsic behavior"). Although almost all data available in literature is on SiO₂ as a gate dielectric, the procedures outlined in this document apply to any dielectric layer. In case of a gate stack of different dielectrics, special care has to be taken when calculating the field distribution across the dielectric stack. This is not covered by this document.

MOS devices such as MOSFETs and IGBTs are designed to be operated at a fixed gate voltage (V_{GS}) level in the ON-state. As-such, oxide lifetime under controlled gate bias conditions is most appropriate for oxide lifetime extraction. On the other hand, charge to breakdown measurements or constant current stress can provide an alternative way to estimate lifetime, provided some conditions are fulfilled. Practical tests, which give oxide lifetime-related information, are (usually on-wafer and/or packaged devices):

- Constant-voltage stress (CVS) time-dependent dielectric-breakdown (TDDB) testing over short and relatively long time periods.
- Ramped-voltage stress (RVS) or ramped breakdown (RBD) approaches in which data for many samples can be obtained quickly. A voltage ramp is typically used for this test (V-Ramp), although a current, or current density ramp (J-Ramp), can be performed as well.
- Constant current stress (CCS) time dependent dielectric breakdown testing for low and high current densities.

It should be pointed out that all discussed tests provoke so-called hard-fails. This means that the device is typically "short" after the failure. "Soft" gate oxide failures (only a slight increase of the gate leakage current) as well as fails by parameter shifts were not expected in the typical gate oxide thickness range of SiC-based power-semiconductors. Furthermore, parameters like V_{TH} are typically shifting in such tests, but this is not a topic of interest in the evaluation of the tests.

Testing of gate oxide breakdown under accelerated bias, current or temperature conditions does not replace traditional qualification tests such as high-temperature gate bias (HTGB) testing called for in, for example, JESD22-A108F. This document is not meant to define acceptable lifetime limits, or proscribe acceptable use conditions; that is up to the device manufacturers and users.

2 Normative References

This guideline is meant to point out specific practices that may be applicable when testing gate oxide reliability for SiC-based power MOS devices. Practices proscribed in the following documents are to be followed, except where they are specifically modified in this present document:

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

JEP001A, *Foundry Process Qualification Guidelines* (2014).

JEP122H, *Failure Mechanisms and Models for Silicon Semiconductor Devices* (2016).

JESD35-A, *Procedure for the Wafer-Level Testing of Thin Dielectrics* (2001).

JESD35-2, *Test Criteria for the Wafer-Level Testing of Thin Dielectrics* (1996).

JESD47J.01, *Stress-Test-Driven Qualification of Integrated Circuits* (2017).

JESD91B, *Method for Developing Acceleration Models for Electronic Device Failure Mechanisms* (2022).

JESD92, *Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics* (2003).

3 Terms and Definitions

For the purposes of this publication, the following terms and definitions apply.

Terms in order of relevance:

TDDB: Time-dependent dielectric breakdown; most properly applies to conditions where all parameters are fixed except for time, but it is often applied to breakdown testing when other parameters are also varied (such as voltage or current) besides time.

CVS: Constant voltage stress; this is the typical TDDB condition, sometimes referred to as CV-TDDB to differentiate from ramped tests.

CCS: Constant current stress; is a TDDB condition in which the current density is kept constant during the duration of the stress.

RBD: Ramped breakdown; if voltage is ramped, it may be referred to as Ramped Voltage Stress (RVS), or V-Ramp; if current (or current density) is ramped, it is referred to as a Ramped Current Stress (RCS) or J-Ramp test.

3 Terms and Definitions (cont'd)

Defined variables in order of relevance:

t_{BD} : Time to breakdown (often units of seconds, or hours). The value t_{63} refers to the failure time for 63% of the devices (the Weibull alpha α), t_{50} refers to the time, at which 50% of the population fails (for lognormal distributions), etc.

t_{ox} : Oxide (or dielectric) thickness, measured electrically, optically, or physically.

V_{ox} : Voltage drop across oxide [V]

E_{ox} : Oxide field [V/cm], V_{ox}/t_{ox} . V_{ox} should be corrected for capacitor flatband voltage (V_{fb}) if V_{fb} is significant compared to V_{BD} .

V_{BD} : Oxide film breakdown voltage [V]

Q_{BD} : Charge to breakdown : $t_{fail} \times J_{dens}$ for a CCS experiment. J_{dens} is the current density during stress, t_{fail} is the time to failure.

4 Intrinsic G_{ox} Quality: Constant-Voltage Breakdown Stress

For SiC power MOS-based devices (MOS capacitors, MOSFETs, and IGBTs, for example), constant-voltage time-dependent dielectric breakdown (TDDB) testing should in most regards be consistent with the approaches established for silicon-based MOS devices in JEP001A for process qualifications, in JESD47J.01 for part qualifications, or as in JESD92 for characterizing gate oxide reliability and predicting lifetime, and JEP122H for mathematical description (models). Generally important aspects of testing are mentioned herein as guidelines for SiC power device testing.

JESD47J.01 recommends that either TDDB data or charge-to-breakdown data be available when new wafer fabrication or dielectric materials are utilized in a device family. General testing guidelines follow from JEP001 and JESD92. Because MOS devices are operated with a constant gate bias in the ON-state, constant voltage TDDB testing (time dependent dielectric breakdown, time-to-breakdown) is recommended for failure distribution and lifetime evaluation rather than constant-current testing (charge-to-breakdown). Although capacitor structures fabricated with the same processing as MOS transistors are allowed in other existing JEDEC documents, we recommend the testing of the actual product (i.e., transistors) where possible with positive polarity at the gate terminal (use case of the devices). Also voltage stress with negative polarity at the gate terminal should be considered if the devices are specified to have a negative gate voltage during turn-off.