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Guideline for Evaluating Gate Switching Instability of Silicon Carbide Metal- Oxide-Semiconductor Devices for Power Electronic Conversion

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Foreword

This publication has been drafted and approved by the JEDEC JC-70.2 SiC Power Electronic Conversion Semiconductor Standards subcommittee, which consists of recognized industry experts from foundries and fabless member companies.

While the existing JEDEC document JEP184 “GUIDELINE FOR EVALUATING BIAS TEMPERATURE INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION” addresses the bias temperature instability and related static gate stress, this document addresses more application-oriented gate stress testing and how to quantify the silicon carbide specific degradation mechanisms of gate switching instability.

Introduction

The objective of this publication is to help to further extend the information given by JEP184 regarding the long-time stability of parameters like threshold voltage not only under static conditions but also under application near switching conditions. Under such conditions a SiC specific degradation mechanism called “gate switching instability” can occur including drift values that can exceed the drifts seen under static conditions. After describing the mechanism and the influencing factors this guideline suggests a test procedure called “gate switching stress test”. The aim of this test procedure is to evaluate the drift that has to be expected in the application for a device technology.

GUIDELINE FOR EVALUATING GATE SWITCHING INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION

(From JEDEC Board Ballot JCB-22-62, formulated under the cognizance of JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee.)

1 Scope

The scope of this document covers SiC-based PECS having a gate dielectric region biased to turn devices on and off. This document should enable the reader to evaluate the consequences of SiC MOSFET specific parametric drift mechanism called “gate switching instability” for the device and/or the application. Additionally, the gate switching stress (GSS) test is described, enabling the calculation/measurement of the worst-case drift that has to be anticipated until the end of the application profile

2 Normative References

JEDEC JEP183, Guidelines for measuring the threshold voltage (VT) of SiC MOSFETs, 2021.

JEDEC JEP184, Guideline for Evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion, 2021.

3 Terms and Definitions

Terms that are already defined in JEP184 are only listed if something relevant for this document is added. For the missing definitions, consolidate JEP183 and JEP184.

Gate switching instability (GSI): threshold voltage instability of a MOS device operating in a gate switching mode between a voltage much above the threshold voltage and below the flatband voltage. Generally, describes the degradation in the conduction path of the device driven by the switching event.

Gate switching stress (GSS): Stress test to measure the GSI-induced degradation under simplified switching conditions.

Frequency (f): switching frequency of the SiC MOSFET

Number of switching cycles (N_{cycles}): number of switching cycles between gate and source calculated by multiplying the time under operation with the frequency: $N_{\text{cycles}} = t \times f$.

End of application profile (EoAP): assumed end point in time of a given application profile.