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A Case for Lowering Component- level CDM ESD Specifications and Requirements Part II: Die-to-Die Interfaces

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**A CASE FOR LOWERING COMPONENT-LEVEL CDM ESD
SPECIFICATIONS AND REQUIREMENTS
PART II: DIE-TO-DIE INTERFACES**

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Introduction

This document addresses the targets of electrostatic discharge (ESD) design, manufacturing control, and testing for die-to-die (D2D) interconnects, **which is exclusively a topic for IC assembly and testing of chiplets by OSATs, foundries, or IDMs**. Once the chiplets are assembled in a package these die-to-die interfaces are no longer exposed to ESD risk.

For this purpose, an industry-wide survey of requirements and targets for D2D interfaces has been performed. More than 60 responses across industry and geographic locations were collected. It shows the high relevance and urgency of the topic. The need for standardization of the charged device model (CDM) design goals as well as the manufacturing assessment was clearly expressed.

It should be noted that throughout this white paper, the term system-on-chip (SoC) will commonly be used to refer to any 2.5D or 3D multi-chip package (MCP) or multi-chip module that contains D2D interconnects.

This paper is the foundation for the standard intellectual property (IP) development of D2D hard IP. Area, performance and power constraints enforce an unprecedented lowering of the CDM requirements for D2D interfaces to 5 V for products starting as early as volume production in 2024. The implementation of the required ESD control is anticipated to occur in steps. While a few lead assembly sites equipped for advanced heterogeneous integration are already prepared for the lower-level ESD robustness of D2D interfaces, others in the industry might take a couple of years to comply with the requirements. This is indicated in the graph in the time frame from 2024 to 2028. It is also anticipated that another transition to 3 V beyond 2028 for high-density D2D interfaces with even tighter bump pitches (see Figure 1) will be needed.

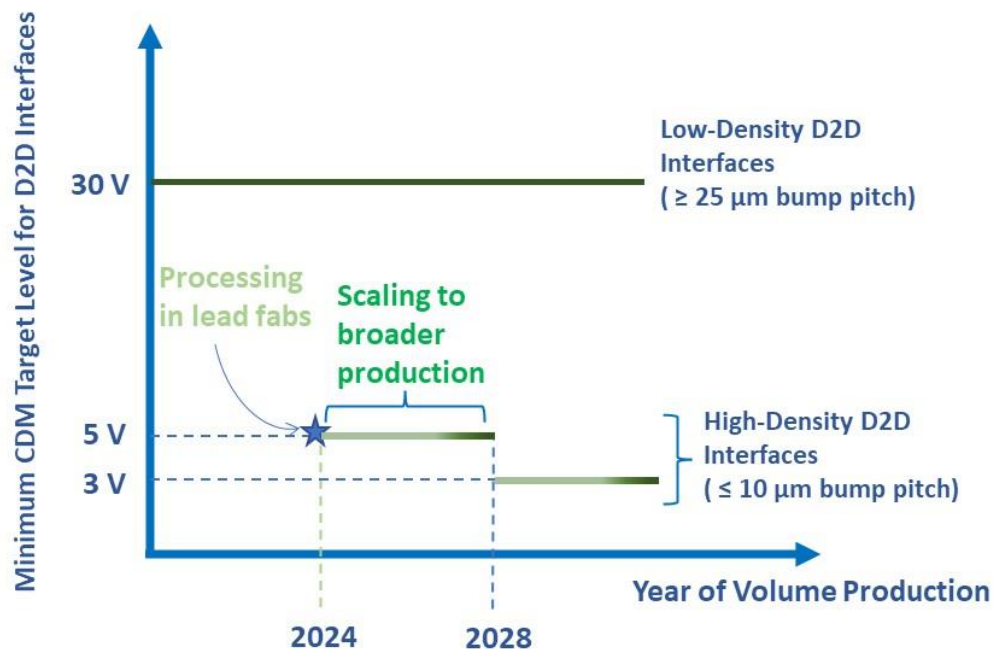


Figure 1 — Roadmap of CDM Targets of Die-to-Die Interfaces

Introduction (cont'd)

IP development must be related to CDM peak current. The peak current depends on the size of the die. Reference values of 75 mA to 116 mA are given for a 5 V target assuming typical die sizes from 60 mm² to 500 mm². This reduces to 45 mA to 70 mA for a 3 V CDM target. The actual peak current values depend on the capacitance of the die to the charging plate in the CDM test setup and the discharge impedance. The actual capacitance of the die is typically lower, but this requires additional investigation, determining this actual capacitance, and thus peak current, is essential to determine the optimum design solution.

To guarantee the safe manufacturing of components with low-level CDM D2D interfaces, a detailed process assessment must be performed of the process steps before and up to the point where wafers are bonded, die are bonded to a wafer, or die are attached to a package substrate (with or without D2D bridges). At this point, it is presumed the D2D interface is no longer exposed to an ESD risk. This is specific to each assembly process variant. American National Standards Institute (ANSI)/ESD SP17.1 describes methodologies to assess manufacturing facilities at low charging and discharging levels. Based on survey responses, it is felt that more information than is contained in ANSI/ESD SP17.1 is needed, but it should be noted that this will be difficult if not impossible to do. At these low target levels, critical process assessments must be completed on the tools used to handle die/wafers. There are no shortcuts based on a simple list of things to do. As these tools will vary from company to company, an ESD expert must leverage the process assessment techniques as discussed in ANSI/SP17.1 for assessing these tools. Even if the tool is of the same type, there may be differences in materials used or the process itself that could influence the charging or discharging risk. Assessment of materials that may contact these die/wafers is no different from what is discussed in ANSI/ESD S20.20.

Standard field-induced CDM testing of the chiplets according to ANSI/ESDA/JEDEC JS-002 does not apply to high-density D2D interfaces for three reasons:

- ANSI/ESDA/JEDEC JS-002 field-induced CDM (FICDM) testing gives meaningless results in the sub-100 V range.
- The tighter pitch (~10 µm and down to 1 µm in the future) is beyond the capabilities of today's most advanced systems.
- The high number of hybrid bonds or µbumps, which can be hundreds to millions, is beyond the scope of reasonable testing.

Fortunately, the overwhelming majority of D2D interfaces are exact copies of a few standard input/output (I/O) variants. The following approaches are therefore proposed:

- Perform the stress test on a test vehicle that contains the set of D2D interface variants.
- Include the design for test measurement capability for the SoC by providing contact points for a few representative D2D interfaces covering the used D2D interface variants.

The stress test can be executed using very-fast transmission line pulse (VF-TLP), capacitively-coupled TLP (cc-TLP), or low-impedance contact CDM (LICCDM) testing. A stress test of the D2D interfaces on the SoC is not required if a comprehensive test of the IP on a test chip has been performed.

During the sign-off, the verification tools must validate the correct integration of the D2D interface cells. Full coverage of all D2D I/Os must be guaranteed. This is especially critical because a later ESD qualification test on the D2D I/Os on a fully assembled SoC is not possible. This should pave the way to a correct-by-design qualification approach.

Introduction (cont'd)

In summary, a call to the industry is presented to prepare for low-level CDM robustness of D2D interfaces to account for area and power constraints. This opens the door for the wide use of D2D interfaces and, consequently, to the full capability of heterogeneous integration.

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A CASE FOR LOWERING COMPONENT-LEVEL CDM ESD SPECIFICATIONS AND REQUIREMENTS PART II: DIE-TO-DIE INTERFACES

(From JEDEC Board Ballot JCB-23-46, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This white paper presents an industry-wide survey on the relevance of industry-aligned D2D CDM targets and the currently used targets for D2D interfaces. The survey results emphasize the need for a common roadmap.

The three main aspects of the paper are the assessment of the status of electrostatic discharge (ESD) control of the process steps with ESD exposure for D2D interfaces, the stress test approach, and the roadmap of the target values. These recommendations outline the tasks for the industry to get prepared for the use of high-density D2D interfaces in the years to come. The white paper affects IP design, chiplet design, foundry, and the outsourced semiconductor assembly and test (OSAT) industry as well as EDA vendors.

2 References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

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3 Terms and Definitions

ANSI	American National Standards Institute
cc-TLP	capacitively-coupled transmission line pulse
CDM	charged device model
CoW	chip-on-wafer
CoWoS®	chip-on-wafer-on-substrate
D2D	die-to-die
DOE	design of experiments
EDA	electronic design automation
EOS	electrical overstress
ESD	electrostatic discharge
ESDS	ESD-sensitive
ESDA	Electrostatic Discharge Association; ESD Association; EOS/ESD Association
FA	failure analysis
FICDM	field-induced charged device model
FINFET	fin field-effect transistor
FPGA	field-programmable gate array
FWHM	full-width half maximum
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
HBM	high bandwidth memory
HBM	human body model
HVM	high-volume manufacturing
IC	integrated circuit
IDM	integrated device manufacturer
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
InFO	integrated fan-out
IP	intellectual property

3 Terms and Definitions (cont'd)

I/O	input/output
JEDEC	JEDEC Solid State Technology Association
LICCDM	low-impedance contact charged device model
LSI	local silicon interconnect
MCP	multichip package
MIM	metal-insulator-metal
OSAT	outsourced semiconductor assembly and test
PDK	process design kit
RC	resistor-capacitor network
RDL	redistribution layer
SP	standard practice
STM	standard test method
UCIe™	Universal Chiplet Interconnect Express
VF-TLP	very-fast transmission line pulsing
V_{charging}	the charging voltage in a real-world scenario
V_{CDM}	charging voltage of field plate in CDM test setup
W2W	wafer-to-wafer
WoW	wafer-on-wafer

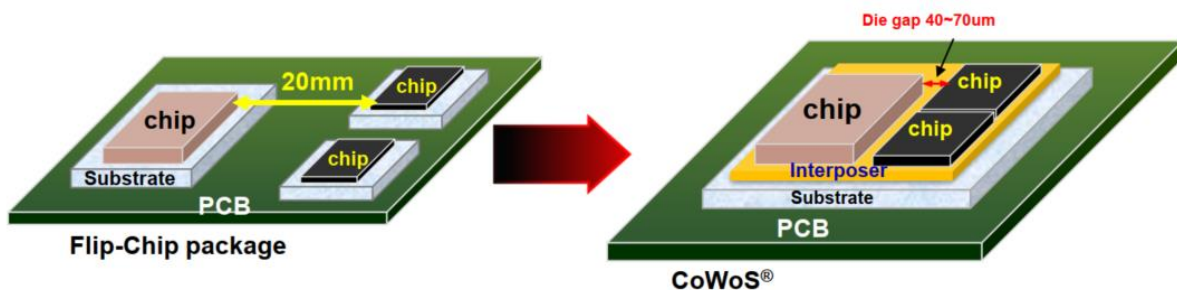
system-on-chip (SoC): Throughout this white paper, the term will commonly be used to refer to any 2.5D or 3D multi-chip package (MCP) or multi-chip module that contains D2D interconnects.

4 Overview of Heterogeneous Integration Technology

4.1 Introduction to Heterogeneous Integration

Heterogeneous integration is an assembly technology to integrate chiplets of similar (like memories) or diverse (like digital and analog) functions into one package. This realizes a much higher packing density and lowers the power consumption due to shorter interconnects (Figure 2).

There are various types of heterogeneous integration schemes in use [Wu2021]. This includes wafer-on-wafer (WoW) and chip-on-wafer (CoW) process variants as shown in Figures 3 and 4. The stacking schemes entail 2.5D and 3D stacking. Silicon, glass, and organic interposers are applied in 2.5D technologies. In addition, the organic interposer technology allows one to choose between a chip first or a chip last configuration in various implementations (Figure 5 and Figure 6) where a silicon interposer represents a more traditional lateral die communication in the metal routing in silicon and a redistribution layer (RDL) interposer has the lateral die communications routed in the RDL. The metal connections between the dies are implemented as μ bumps based on traditional solder bump technology or hybrid bonding with Cu-Cu connections. The 3D wafer stack can be found either as front-to-front or front-to-back configurations as shown in Figure 7. The different process variants create different exposure of D2D interfaces to ESD and have to be assessed individually. This requires detailed knowledge of the process and its effect on ESD. A general description of assessment methods is given in ANSI/ESD SP17.1. The aspects of a specific analysis of the D2D relevant process steps are discussed in Clause 6.



NOTE This reduces the wiring length between the chiplets and enables a higher integration density.

Figure 2 — 2.5D Chiplet Integration on an Interposer

4.1 Introduction to Heterogeneous Integration (cont'd)

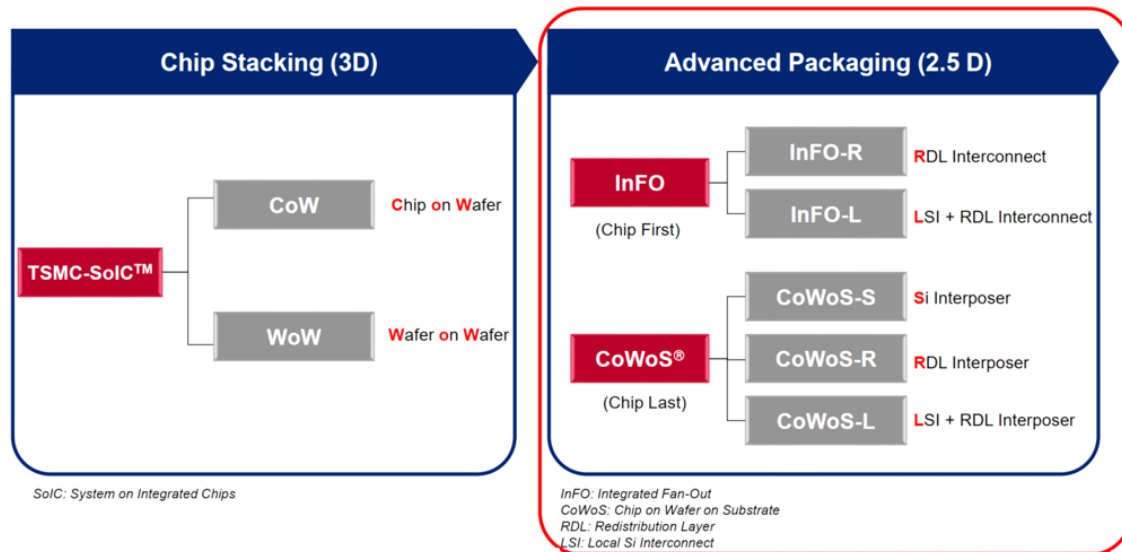
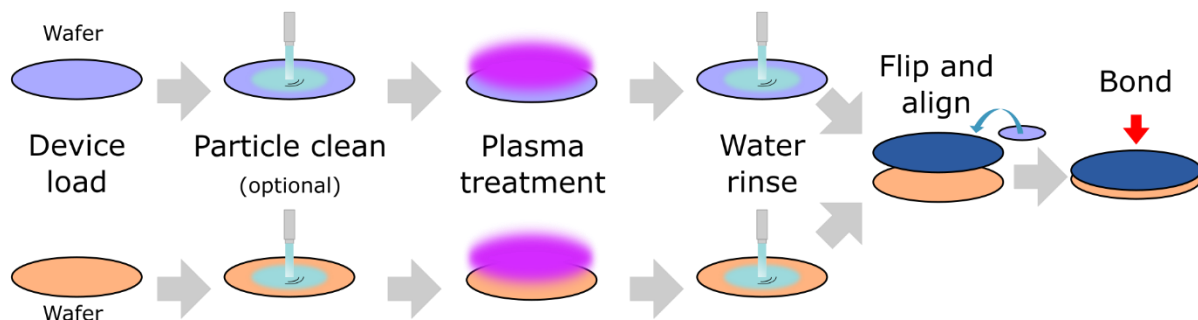


Figure 3 — Various Types of 3D and 2.5D Integration Schemes



NOTE Two wafers are loaded into the bonding tool. Both wafers undergo a plasma treatment to activate the dielectric. One wafer is flipped without touching the front side. All dies are collectively bonded in a single bonding step.

Figure 4 — Schematic of the Wafer-to-Wafer Hybrid Bonding Process

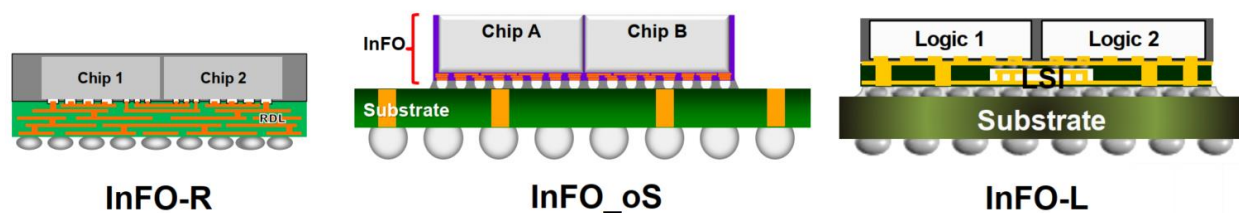
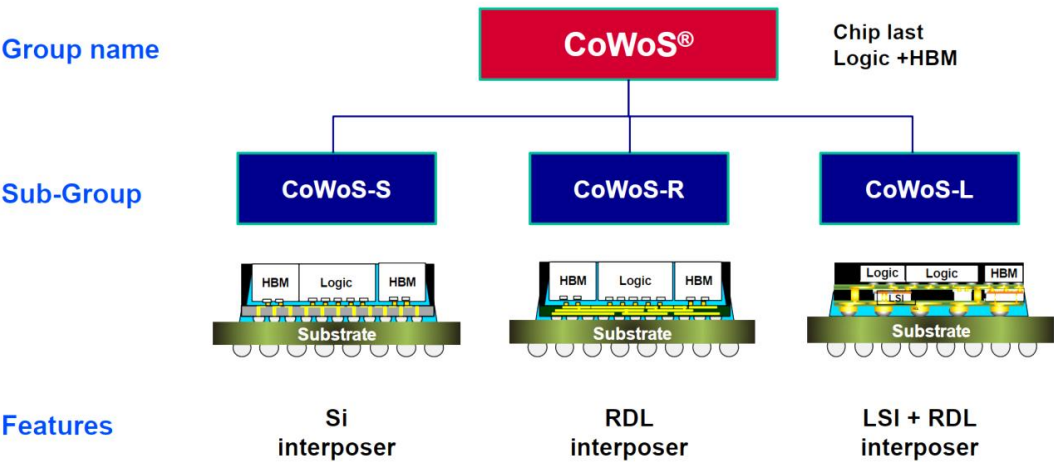


Figure 5 — Cross Section of Various 2.5D Integration Schemes w/o Interposer

4.1 Introduction to Heterogeneous Integration (cont'd)



NOTE RDL = redistribution layer, HBM = high bandwidth memory

Figure 6 — Various Interposer Technologies

WoW FtF & FtB Offerings Cross-section

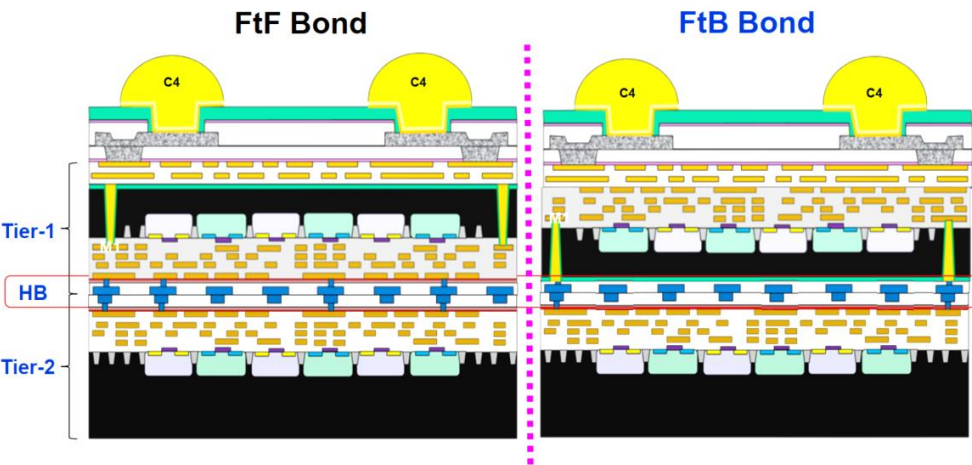


Figure 7 — Hybrid Bonding a) Front-to-Front b) Front-to-Back

4.2 Roadmap of μ bumping and Hybrid Bonding

The number of D2D interfaces is predicted to increase exponentially in the coming years. Thousands and even millions of D2D interconnect may be found in heterogeneous integration systems soon. It is expected that the interconnect pitch will drop below $10\ \mu\text{m}$ in the next 2-3 years, making direct probing for TLP evaluations nearly impossible. Research and development work has shown a hybrid bond pitch of less than $1\ \mu\text{m}$ as shown in Figure 8.

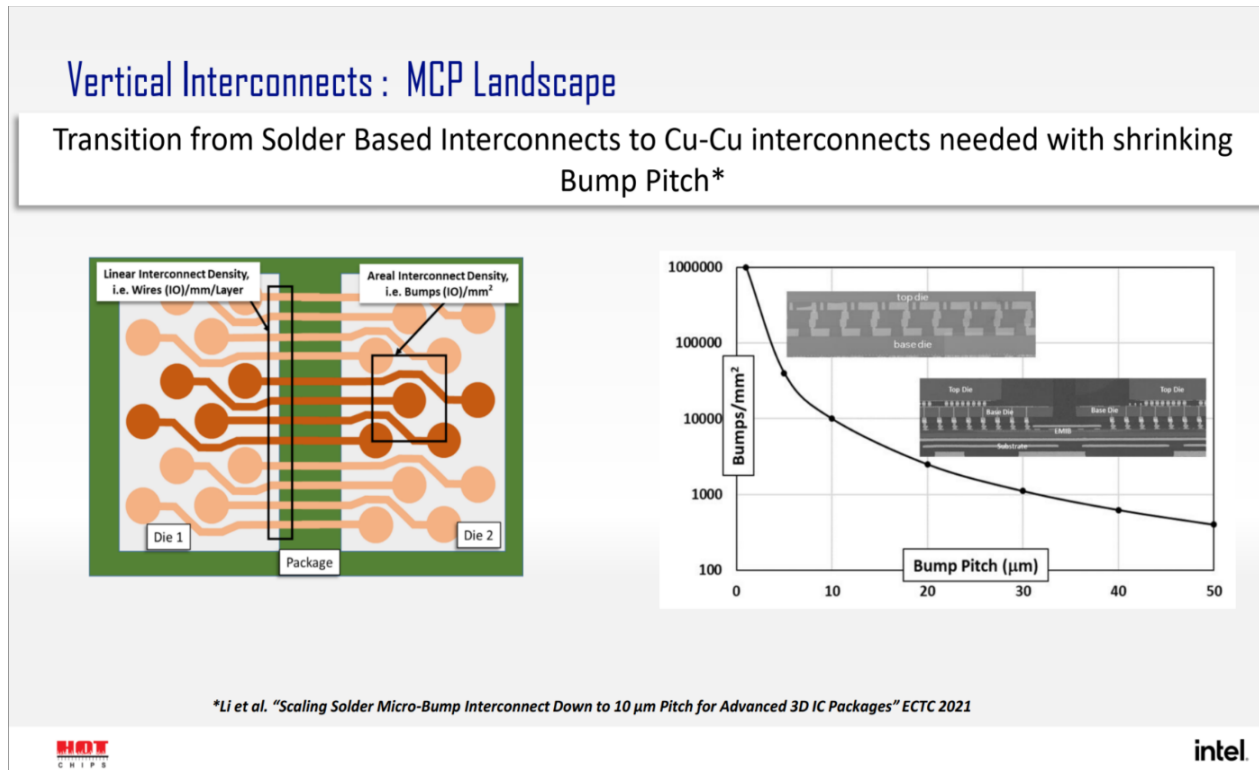


Figure 8 — Multi-Chip Package Landscape

4.3 Impact of ESD Protection Design of D2D Interfaces on Power, Performance, Area, and Cost

A typical dual diode protection concept in a fin field-effect transistor (FINFET) technology has a footprint of $0.05 - 0.1\ \mu\text{m}^2/\text{mA}$ and a capacitive load due to ESD protection of $\sim 0.1\ \text{fF}/\text{mA}$. For example, a CDM target level of $35\ \text{V}$ results in typical CDM peak currents of $150\ \text{mA} - 300\ \text{mA}$ depending on the size of the die. For a million D2D interfaces, the ESD-related area amounts to $8\ \text{mm}^2 - 30\ \text{mm}^2$ of chip area. The capacitive load of $15 - 30\ \text{nF}$ leads to excessive power consumption. This needs to be accounted for in the specification of a CDM target level.

5 Industry Survey on ESD Targets of Die-to-Die Interfaces

5.1 Set-up of Survey

The industry survey was designed by the working group focused on D2D interfaces for the Industry Council on ESD Target Levels. The survey was launched at the beginning of June 2022. The information presented here in this document results from the industry feedback collected after the survey ended in November 2022.

The survey addresses the need for specific CDM targets for D2D interfaces and dedicated ESD control measures for the heterogeneous integration process. In total, 30 questions were asked, either single-choice, multiple-choice, or text-based. The questionnaire could be completed leaving any number of questions unanswered. Answers left blank were ignored for the analysis. All questions for the survey are shown in Annex A and results are shown in Annex B.

Some of the answers given in text form have been paraphrased, and/or similar ones combined for the data presented in Clause 5.3 and Annex B.

5.2 Analytics of Participation

57 responses were received from the survey, spanning the Americas, East Asia, and Europe [Q02]. The responses came from a wide range of industries including silicon foundries, integrated device manufacturers (IDM), design houses, IP vendors, outsourced semiconductor assembly and test facilities (OSATs), contract manufacturers, and electronic systems manufacturers [Q01, Q03].

5.3 Trends and Conclusions

This clause will discuss the results of the survey starting with ESD design targets followed by ESD control standards for D2D processes.

5.3.1 ESD Design Targets for D2D Interfaces

- 51% of all respondents apply lower CDM targets for D2D than for external balls, while 25% don't apply lower targets for D2D interfaces. 24% indicated that it doesn't apply to them [Q04]. A majority of those who don't apply a D2D process in their workflow are e.g., system manufacturers, failure analysis (FA) labs, or distributors.

In some cases, different experts from the same company provided both the answer of reduced and non-reduced targets. This might depend on the types of products or designs they are addressing.

This means that 2/3 of the respondents who are exposed to the challenge of D2D interface design or processing, apply lowered targets. 1/3 of the respondents don't. It is suspected that their products only contain a low number of D2D interfaces, and the impact of the area does not affect the SoC design critically.

- 32% of all respondents apply different CDM targets for D2D depending on whether it is a 2.5D or 3D process [Q05]. A clear trend towards this practice is observed for foundries whereas the responses vary for the other sectors.

5.3.1 ESD Design Targets for D2D Interfaces (cont'd)

- 56% of all respondents see a need to lower the targets to satisfy the power, performance, and area requirements for future products [Q08]. Considering that 28% answered that the question doesn't apply to them, this means that 78% of the respondents that are exposed to the challenge of D2D interface design are looking into lowering the targets to meet critical product key performance indicators.
- 79% of all respondents see a need for an industry alignment on target levels [Q09]. As compared to previous questions, only a small group of 9% selected "n/a", indicating that even the companies not directly dealing with D2D interface designs and processes are in favor of an industry alignment.
- The currently applied target levels are widely spread and vary from 3 V to >70 V or 10 mA to >300 mA, respectively [Q11, Q12, Q13]. Possible explanations for the wide range of targets are:
 - correlation to the 2.5D and 3D hybrid bonding type of heterogeneous integration technology [Q05] as well as differing number and density of 2.5D and 3D interconnects for different product designs,
 - missing standards in the industry [Q09, Q10] and missing knowledge of manufacturing capabilities and limitations [Q21 – Q24, Q29, Q30],
 - limited experience with actual D2D fail limits, i.e., product/high-volume manufacturing (HVM) fails or design of experiments (DOEs) in production as can be seen from the responses to questions [Q17 – Q24],
 - different robustness levels of technology nodes,
 - different needs and pain points for different types of designs; different customer requests [Q12, Q13].
- A similar diversity is found for the implementation of ESD protection (diodes, local clamps, self-protection, or a combination thereof) [Q14, Q15], as well as the verification (simulation, static layout verification, silicon-data based, ...) of the D2D ESD protection [Q06, Q07].
- 48% of all respondents are detailing a timeline for products with reduced D2D targets going into volume production. Out of these, 44% report this taking place as early as 2022, and another 41% by 2024 [Q16].

Based on these responses, it can be concluded that dedicated D2D targets are relevant for design and standardization and are highly desired with 74% of respondents asking for a robustness target specified in current [Q25]. The product roadmap schedules illustrate the urgency of an alignment in the industry. However, the variety of currently applied targets and approaches presents a challenge for design and manufacturing to align on common metrics for success.

5.3.2 ESD Control Standards for D2D Processes

- 88% of all respondents see the need for ESD control standards [Q10], representing the broadest agreement to any question in this survey.
- 24% of respondents who answer the question stated that they have encountered ESD fails on D2D interfaces [Q17] with some of them having experienced them in more than one place. Of all detected fails, 73% of them were detected in HVM testing, 20% at the customer, and in one case (6%) at system level testing [Q18]. 38% of the observed failures could not be root caused while 23% occurred during testing and 15% during die stacking [Q19].