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Procedure for Reliability Characterization of Metal-Insulator-Metal Capacitors

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PROCEDURE FOR RELIABILITY CHARACTERIZATION OF METAL-INSULATOR-METAL CAPACITORS

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Foreword

The intent of this procedure is to provide comprehensive recommendations for assessing all aspects of Reliability (Intrinsic, Defect and Thermo-mechanical) pertinent to MIM (Metal-Insulator-Metal) Capacitor that are offered as technology features on process nodes. The procedure describes the testing methods such as Constant Voltage Stress for getting insights into conduction mechanisms and TDDB (Time Dependent Dielectric Breakdown) physics.

This procedure will also comprehend potential parametric shifts as part of intrinsic reliability. VRDB (Voltage Ramp Dielectric Breakdown) test is also described as a tool to estimate ‘extrinsic’/defect reliability and as a quick turn method for gaining insights into intrinsic reliability. Furthermore, conventional temperature cycle stresses (TCB, TCC) and HAST can be used to characterize the thermo-mechanical and environmental reliability of MIM Capacitors.

PROCEDURE FOR RELIABILITY CHARACTERIZATION OF METAL-INSULATOR-METAL CAPACITORS

(From JEDEC Board Ballot JCB-24-04, formulated under the cognizance of the JC-14.2 Subcommittee on Wafer-Level Reliability.)

1 Scope

This publication provides a complete framework and defines the standards for achieving Reliability certification and qualification of on-chip MIM capacitors or Trench capacitors (MIS Capacitor). The test methods and Merit definitions comprehend the full gamut of products across all market segments with respect to use condition and EOL targets. The scope covers all applications of MIMCAP, such as decoupling capacitor and signal capacitance usage.

2 Normative References

JEP001, *Foundry Process Qualification Guidelines – Backend of Line*

JEP159A, *Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity*.

3 Terms and Definitions

For the purpose of this publication, the following terms and definitions apply.

3.1 Abbreviations

MIM: Metal Insulator Metal

CVS: Constant Voltage Stress

DUT: Device Under Test

TDDB: Time Dependent Dielectric Breakdown

VRDB: Voltage Ramp Dielectric Breakdown

ESR: Equivalent Series Resistance

DCAP: Decoupling Capacitor

TTF: Time to Fail

TCB: Temperature Condition B

TCC: Temperature Condition C

HAST: Highly Accelerated Stress Test

RF: Radio Frequency

FOM: Figure of Merit

3.2 Symbols and Definitions

I_{meas} (A): Measured current

I_{comp} (A): Maximum current/compliance current limit for a particular test

V_{stress} (V): DUT stress voltage

V_{use} (V)/ V_{nom} (V): Use or Nominal voltage for a specific technology node; V_{nom} should include power supply tolerance (Range 5% to 10%)

C (F): Measured DUT capacitance

E_a (eV): Thermal activation energy

4 Technical Requirements

4.1 Test Structures

Test structures for MIM Capacitor can be a 2-plate or a multi-plate capacitor with dedicated bussing connection to each individual plate. The structure should have enough routing resources (lines/vias) to ensure that the voltage droop is minimal. Additional care should be taken with respect to routing if the MIM Capacitor is used for signal applications so as to minimize the resistive loss [ESR]. It is recommended to use RF pads for signal applications.

For intrinsic assessments, a minimum area of $10,000 \mu\text{m}^2$ capacitor area is recommended (or representative mission profile “area” of the product). In addition, area skews spanning at least 2 orders of magnitude (either higher or lower than $10,000 \mu\text{m}^2$) should be considered for extraction of TDDB dependence on area.

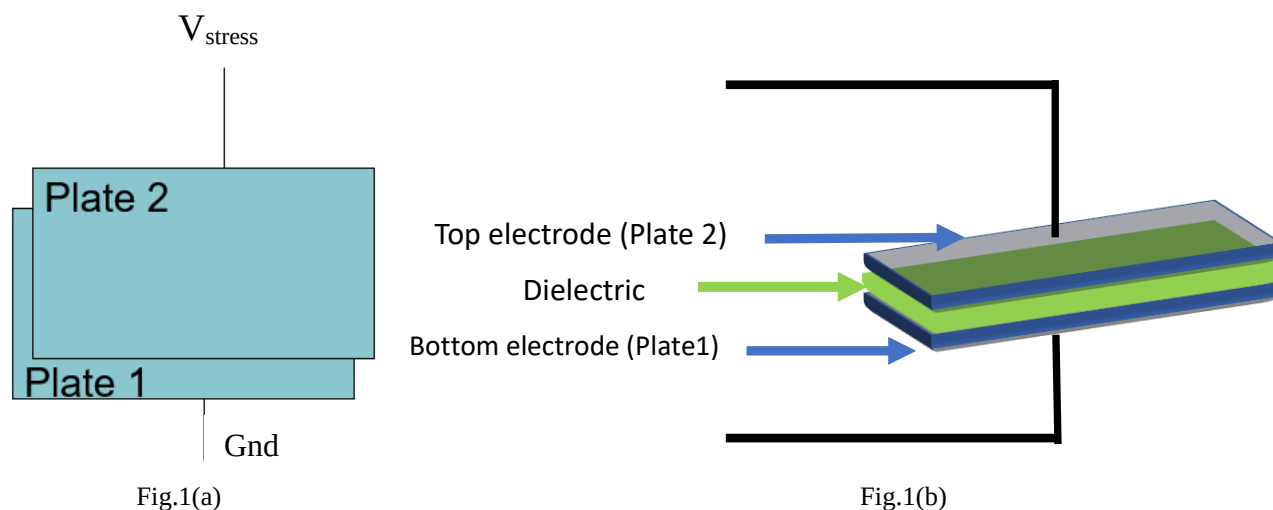


Figure 1 — Top View and Cross-sectional View of Metal-Insulator-Metal Capacitor

A larger area structure of at least $25,000 \mu\text{m}^2$ is recommended to be used for estimation of the ‘extrinsic’ / ‘defect’ reliability of the structure.