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TEST PROCEDURES FOR VERIFICATION OF
MAXIMUM RATINGS OF
POWER TRANSISTORS

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FOREWORD

This publication describes tests which are intended to represent only the verification of maximum ratings; they are not tests for performance or quality level. It is proposed that this material be used in conjunction with formats developed for device registration and defining data.

All values specified are nominal and should be maintained within equipment capabilities and good engineering practice.

The procedures in this document were prepared by the JS-6 Committee on Power Transistors and approved for publication by the JEDEC Semiconductor Device Council.

JS-6 - T1.1

Minimum Storage Temperature, Maximum Ratings T_{stg} min.

1. General

The minimum storage temperature shall be based on the capability of any individual transistor to meet the test described below.

2. Test Conditions

- a. T_{stg} as specified.
- b. Duration of the test to be one cycle, 6 hours at minimum specified storage temperature

3. Procedure

- a. Adjust the temperature in a temperature-controlled enclosure to the specified storage temperature.
- b. Place test transistors in the enclosure.
- c. The order of the procedure may be reversed.

4. Evaluation

- a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.
- b. The device shall still be capable of meeting all the Electrical Characteristics of the Registration.

JS-6 - T1.2

Maximum Storage Temperature, Maximum Ratings, $T_{stg\ max.}$

1. General

The maximum storage temperature shall be based on the capability of any individual transistor to meet the test described below.

2. Test Conditions

- a. T_{stg} as specified.
- b. Duration of the test to be one cycle, six hours at the maximum specified storage temperature.

3. Procedure

- a. Adjust the temperature in a temperature-controlled enclosure to the specified storage temperature.
- b. Place test transistors in the enclosure.
- c. The order of the procedure may be reversed.

4. Evaluation

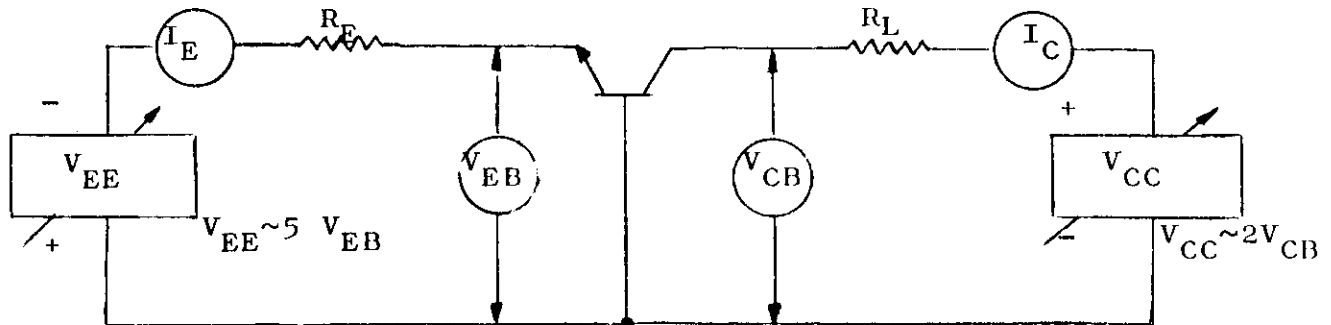
- a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.
- b. The device shall still be capable of meeting all the Electrical Characteristics of the Registration.

Maximum Operating Junction Temperature Rating, $T_{j \text{ max.}}$

1. General

The maximum operating junction temperature shall be based on the capability of any individual transistor to operate in the test circuit illustrated below:

2. Test Circuit and Conditions: (Polarity of transistor - PNP, NPN - must be observed)



a. V_{CB} and I_C must be specified.

b. The case temperature must be within 75 to 90 percent of the registered operating junction temperature, T_j .

c. The duration of the test shall be one hour.

3. Procedure

a. Adjust the bias conditions to achieve the specified I_C and V_{CB} . The temperature and power dissipation must be such that the junction temperature is equal to the maximum operating junction temperature calculated by:

$$T_J = T_C + \frac{P_d}{\text{Derating Factor (W/}^\circ\text{C)}}$$

T_C = Case temperature

$$P_d = \text{Total Power Dissipation} = V_{CB} I_C + V_{EB} I_E$$

b. Suitable precautions should be taken against transient spikes and oscillations.

Maximum Operating Junction Temperature Rating, $T_{j \max}$. (continued)

4. Evaluation

- a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.
- b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

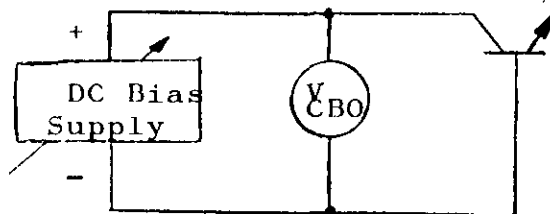
JS-6 - T3

Collector-Base Voltage, Maximum Ratings, V_{CBO}

1. General

The maximum collector-base voltage shall be based on the capability of any individual transistor to meet the test described below:

2. Test Circuit and Conditions: (Polarity of transistor - PNP, NPN - must be observed)



- a. The transistor case temperature must be $+ 25^{\circ}\text{C}$.
- b. Duration of the test to be one minute.

3. Procedure

- a. Adjust the bias supply to obtain the specified V_{CBO} .
- b. Suitable precautions should be taken against transient spikes and oscillations.

Collector-Base Voltage, Maximum Ratings, V_{CBO} (continued)

4. Evaluation

- a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.
- b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

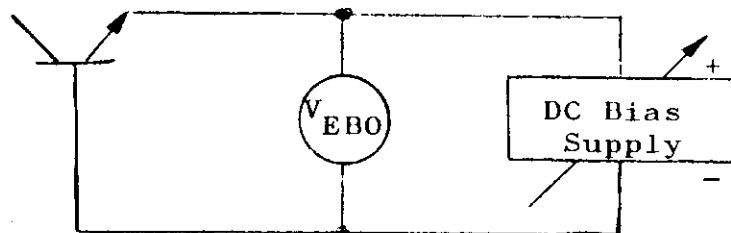
JS-6 - T4

Emitter-Base Voltage, Maximum Rating

1. General

The maximum emitter-base voltage shall be based on the capability of any individual transistor to meet the test described below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



- a. The transistor case temperature must be $+ 25^{\circ}\text{C}$.
- b. Duration of the test to be one minute.

3. Procedure

- a. Adjust bias supply to obtain the specified V_{EBO} .
- b. Suitable precautions should be taken against transient spikes and oscillations.

4. Evaluation

- a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.
- b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.