

JEDEC PUBLICATION

Guide to Standards and Publications Relating to Quality and Reliability of Electronic Hardware

JEP70C

(Revision of JEP70B, October 1999)

OCTOBER 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2013
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

GUIDE TO STANDARDS AND PUBLICATIONS RELATING TO QUALITY AND RELIABILITY OF ELECTRONIC HARDWARE

Contents

	Page
Foreword	ii
Introduction	ii
1 Scope	1
2 Normative references	1
3 Listing of quality and reliability standards and publications	2
3.1 Electrical tests - methods	2
3.2 ESD control - measurement, handling, symbol & label	3
3.3 Mark-pack-ship -container labeling/bar coding, tape & reel, dry	4
3.4 Process control - SPC, CPK, control charting, environmental controls, calibration	5
3.5 Qualification and reliability monitor - initial product/process qualification, ongoing reliability monitoring, qualification of product/process changes	6
3.6 Quality and reliability reporting -AOQ measurement, sampling methods, reliability data(fits), failure analysis, product/process change notification	7
3.7 Quality systems -general requirements, auditing, terminology, certification, supplier/subcontractor control	8
3.8 Reliability testing – methods	9
3.9 Visual and mechanical testing – methods	10
3.10 Component Application – Assembly, Soldering, Board Level Testing	12
Annex A (informative) Standards	13
Annex B (informative) Rescinded, cancelled, withdrawn, or replaced	50
Annex C (informative) Differences between JEP70C and JEP70B	54

Foreword

This document gathers and organizes common standards and publications relating to quality processes and methods relating to the solid-state, microelectronics, and associated industries. This is intended to facilitate access to the applicable documents when working with electronic hardware. This will have a positive effect on quality and reliability as users gain more access to proper methods in designing, producing, and testing parts.

The quality and reliability documents in this publication have been categorized into nine subsections. Each category is organized in a table format in Section 3 and a brief description of each of these documents is contained in Appendix A. The last section is an alphabetized listing of the sources for the standards with their addresses, phone numbers, and URL web sites. This publication will be periodically reviewed and updated as required.

Introduction

Due to the wide breadth of the subject matter and numerous standards bodies in existence this publication cannot, and does not seek to, contain all possible relevant material. It is not intended to recommend or imply the applicability of any standard for a specific purpose.

GUIDE TO STANDARDS AND PUBLICATIONS RELATING TO QUALITY AND RELIABILITY OF ELECTRONIC HARDWARE

(From JEDEC Board Ballot JCB-13-43, formulated under the cognizance of the JC-14.4 Subcommittee on Quality Processes and Methods.)

1 Scope

This publication contains a listing and description of commonly used quality and reliability related publications applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. The document revisions have not been included in this listing. The latest document revision shall be used when referencing this document. The web sites listed above are referred to for the latest and official documents for all standards.

<u>Reference</u>	<u>Name</u>	<u>Web Site</u>
AEC	Automotive Electronics Council	aecouncil.com
ANSI	American National Standards Institute:	ansi.org
ASQ	American Society for Quality:	asq.org
CEA	Consumer Electronics Association	ce.org
CECC	CENELEC Electronic Components Committee	coduss.co.uk/cecc
ESDA	ESD Association	esda.org
IEC	International Electrotechnical Commission	iec.ch
IPC	Institute for Interconnecting and Packaging Electronic Circuits	ipc.org
ISO	International Organization for Standardization	iso.org
JEDEC	Solid State Technology Association	jedec.org
JEITA	Japan Electronics and Information Technology Association	jeita.or.jp
MIL	US Military	
NIST	National Institute of Standards and Technology	nist.gov
SAE	SAE International	sae.org
TECHAMERICA		techamerica.org
UL	Underwriters Laboratories	ul.com

3 Listing of Quality and Reliability Standards and Publications

This list is the number and title of standards and publication relating to the manufacture and testing of hardware components. They are grouped by category and sorted alphabetically. There is a description of each one found in Annex A.

3.1 Electrical Tests – Methods

Number	Title
JEDEC EIA318	Measurement of Reverse Recovery Time for Semiconductor System Diodes
JEDEC EIA397	Recommended Standard for Thyristors
JEDEC EIA397-1	Addendum No. 1 to EIA-397
JEP121	Requirement for Microelectronic Scanning and Test Optimization
JEP128	Guide for Standard Probe Pad Sizes and Layouts for Wafer-Level Electrical Testing
JEP154	Guideline For Characterizing Solder Bump Electromigration Under Constant Current And Temperature Stress
JESD30	Measurement of Small-Signal HF, VHF, and UHF Power Gain of Transistors
JESD78	IC Latch-Up Test
JESD86	Electrical Parameters Assessment
JESD89	Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
JESD89-1	Test Method For Real-Time Soft Error Rate
JESD89-2	Test Method For Alpha Source Accelerated Soft Error Rate
JESD89-3	Test Method For Beam Accelerated Soft Error Rate
JESD282	Silicon Rectifier Diodes
JESD284	Test Methods for the Collector - Base Time Constant and for the Resistive Part of the Common Emitter Input Impedance
JESD286	Standard for Measuring Forward Switching Characteristics of Semiconductor Diode
JESD307	Voltage Regulator Diode Noise Voltage Measurements:
JESD311	Measurement of Transistor Noise Figure at MF, HF and VHF
JESD313	Thermal Resistance Measurements of Conductive Cooled Power Transistor
JESD320	Thermal Equilibrium Conditions for Measurement of Diode Static Parameters
JESD353	The Measurement of Transistor Noise Figure at Frequencies up to 20 KHz by Sinusoidal Signal Generator Method
JESD354	Measurement of Transistor Equivalent Noise Voltage and Equivalent Noise Current at Frequencies of up to 20 KHz

3.1 Electrical Tests – Methods (cont'd)

JESD371	Measurement of Small-Signal VHF-UHF Transistor Short-Circuit Forward Current Transfer Ratio
JESD372	Measurement of Small-Signal VHF-UHF Transistor Admittance Parameters
JESD381	Method of Diode "Q" Measurements
JESD398	Measurement of Small Values of Transistor Capacitance
MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-750	Test Method Standard Test Methods for Semiconductor Devices
MIL-STD-883	Test Method Standard, Microcircuits

3.2 ESD Control – Measurement, Handling, Symbol and Label

Number	Title
AEC-Q100-002	Human Body Model (HBM) Electrostatic Discharge Test (IC)
AEC-Q100-004	IC Latch-Up Test (IC)
AEC-Q100-011	Charged Device Model (CDM) Electrostatic Discharge Test (IC)
AEC-Q101-001	Human Body Model (HBM) Electrostatic Discharge Test (Discreet)
AEC-Q101-005	Charged Device Model (CDM) Electrostatic Discharge Test (Discreet)
AEC-Q200-002	Human Body Model (HBM) Electrostatic Discharge Test (Discreet)
ESD ADV1.0	Glossary for Electrostatic Discharge Terminology
ESD S1.1	Wrist Straps
ESD STM3.1	Ionization
ESD S4.1	Work Surfaces - Resistive
ESD S5.3.1	Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Component Level
ESD S6.1	Grounding - Recommended Practice
ESD S7.1	Resistive Characterization of Materials -Floor Materials
ESD S8.1	Symbols–ESD Awareness
ESD S20.20	Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)
ESD S541	Packaging Materials for ESD Sensitive Items
ESD STM11.11	Surface Resistance Measurement of Static Dissipative Planar Materials
JEP113	Symbols and Labels for Moisture Sensitive Devices
JEP130	Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing
JESD22-A114	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

3.2 ESD Control – Measurement, Handling, Symbol and Label (cont'd)

<u>JESD22-C101</u>	Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components
<u>JESD30</u>	Descriptive Designation System for Semiconductor-Device Packages
<u>JESD471</u>	Symbol and Label for Electrostatic Sensitive Devices
<u>JESD625</u>	Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices
<u>JS-001</u>	Electrostatic Discharge Sensitivity Test - Human Body Model (Hbm) - Component Level

3.3 Mark-Pack-Ship – Container Labeling/Bar Coding, Tape and Reel, Dry-Packing

Number	Title
<u>CEA-556</u>	Outer Shipping Container Bar Code Label Standard
<u>ECA EIA-296</u>	Lead Taping of Components in Axial Lead Configuration for Automatic Handling
<u>ECA EIA-468</u>	Lead Taping Of Components In The Radial Configuration For Automatic Handling
<u>ECA EIA-481</u>	8 Mm Through 200 Mm Embossed Carrier Taping And 8 Mm & 12 Mm Punched Carrier Taping Of Surface Mount Components For Automatic Handling
<u>EIA-476</u>	Date Code Marking
<u>EIA-763</u>	Bare Die and Chip Scale Packages Taped in 8 mm & 12 mm Carrier Tape for Automatic Handling
<u>JEITA ED-7303</u>	Name and Code for Integrated Circuits Package
<u>JEP160</u>	Long-Term Storage Guidelines For Electronic Solid-State Wafers, Dice, And Devices
<u>JESD22-B114</u>	Mark Legibility
<u>J-STD-033</u>	Joint Ipc/Jedec Standard For Handling, Packing, Shipping, And Use Of Moisture/Reflow Sensitive Surface-Mount Devices
<u>MIL-DTL-19491</u>	Packaging of Semiconductor Devices

3.4 Process Control – SPC, Cpk, Control Charting, Environmental Controls, Calibration

Number	Title
ASQC B1-B3	Guide for Quality Control Charts Control Chart Method of Analyzing Data Control Chart Method for Controlling Quality During Production
ASQ H1197	Glossary & Tables for Statistical Quality Control
ASQ- M1	Calibration System
IPC-9191	General Guidelines for Implementation of Statistical Process Control (SPC)
ISO 2859	Sampling Procedures for Inspection by Attributes - Part 1: Sampling Schemes Indexed by Acceptance Quality Limit (AQL) for Lot-by-Lot Inspection
ISO 3534-2	Statistics -- Vocabulary and symbols -- Part 2: Applied statistics
ISO 3951-1	Sampling procedures for inspection by variables Part 1: Specification for single sampling plans indexed by acceptance quality limit (AQL) for lot-by-lot inspection for a single quality characteristic and a single AQL
ISO 3951-2	Sampling procedures for inspection by variables Part 2: General specification for single sampling plans indexed by acceptance quality limit (AQL) for lot-by-lot inspection of independent quality characteristics
JEP132	Process Characterization Guideline
JESD46	Customer Notification Of Product/Process Changes By Semiconductor Suppliers
JESD48	Product Discontinuance
JESD50	Special Requirements For Maverick Product Elimination And Outlier Management
MIL-HDBK-1331	Handbook for Parameters to be Controlled for the Specification of Microcircuits
TECHAMERICA EIA-557	Statistical Process Control Systems
TECHAMERICA EIA-738	Guideline on the Use and Application of Cpk
TECHAMERICA RB9	Failure Mode and Effect Analyses

3.5 Qualification and Reliability Monitoring – Initial Product/Process Qualification, Ongoing Reliability Monitoring, Qualification of Product/Process Changes

Number	Title
AEC-Q100 base	Stress Qualification For Integrated Circuits (base document only with no test methods)
AEC-Q101 base	Stress Test Qualification For Discrete Semiconductors (complete document with test methods)
AEC-Q200	Stress Test Qualification For Passive Components (complete document with test methods)
JEP143	Solid State Reliability Assessment Qualification Methodologies
JEP148	Reliability Qualification Of Semiconductor Devices Based On Physics Of Failure Risk And Opportunity Assessment
JEP158	3d Chip Stack With Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions
JESD22-A121	Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes
JESD22-B118	Semiconductor Wafer And Die Backside External Visual Inspection
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD49	Procurement Standard for Known Good Die (KGD)
JESD69	Information Requirements For The Qualification Of Silicon Devices
JESD72	Test Methods And Acceptance Procedures For The Evaluation Of Polymeric Materials
JESD659	Failure Mechanism Driven Reliability Monitoring of Silicon Devices
JS9702	Monotonic Bend Characterization of Board-Level Interconnects (IPC/JEDEC-9702)
JS9704	Printed Wiring Board (PWB) Strain Gage Test Guideline
MIL-HDBK-175	Microelectronic Devices
MIL-PRF-19500	General Specification for Semiconductor Devices
MIL-PRF-38534	General Specification for Hybrid Microcircuits
MIL-PRF-38535	General Specification for Integrated Circuits (Microcircuits) Manufacturing
SAE J1879	Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
TECHAMERICA SSB-1.001	Qualification and Reliability Monitors

3.6 Quality and Reliability Reporting -AOQ Measurement, Sampling Methods, Reliability Data (FITS), Failure Analysis, Product/Process Change Notification

Number	Title
ASQ- E2	Guide to Inspection Planning
ASQ Q3	Sampling Procedures and Tables for Inspection of Isolated Lots by Attributes
ASQ S1	An Attribute Skip-Lot Sampling Program
ASQ Z1.4	Sampling Procedures and Tables for Inspection by Attributes
ASQ Z1.9	Sampling Procedures and Tables for Inspection by Variables for Percent Nonconforming
ISO 3534-1	Statistics -- Vocabulary and symbols -- Part 1: General statistical terms and terms used in probability
JEP122	Failure Mechanisms and Model for Silicon Semiconductor Devices
JEP131	Process Failure Mode and Effects Analysis (FMEA)
JEP134	Guidelines for Preparing Customer-Supplied Background Information Relating to a Semiconductor Device Failure Analysis
JESD38	Standard For Failure Analysis Report Format
JESD46	Customer Notification of Product/Process Changes by Semiconductor Suppliers
JESD48	Product Discontinuance
JESD85	Methods For Calculating Failure Rates In Units Of Fits
MIL-PRF-38535	General Specification for Integrated Circuits (Microcircuits) Manufacturing
TECHAMERICA EIA-554	Method Selection for Assessment of Nonconforming Levels in Part Per Million (PPM)
TECHAMERICA EIA-555	Lot Acceptance Procedure for Verifying Compliance with the Specified Quality Levels (SQL) in PPM
TECHAMERICA EIA-584	Zero Acceptance Numerical Sampling Procedure and Tables for Inspection by Attributes of a Continuous Manufacturing Process
TECHAMERICA EIA-585	Zero Acceptance Numerical Sampling Procedure and Tables for Inspection by Attributes of Isolated Lots
TECHAMERICA SSB-1.004	Failure Rate Estimating

3.7 Quality Systems -General Requirements, Auditing, Terminology, Certification, Supplier/Subcontractor Control

Number	Title
ASQ C1	Specifications of General Requirements for a Quality Program
ISO 9000	Quality management systems - Fundamentals and vocabulary
ISO 9001	Quality management systems - Requirements
ISO 9004	Managing for the sustained success of an organization -- A quality management approach
ISO 19011	Guidelines for quality and/or environmental management systems auditing
ISO14001	Environmental Management System:
ISO 1011	Guidelines for quality and/or environmental management systems auditing
JEP146	Guidelines For Supplier Performance Rating
JESD31	General Requirements for Distributors of Commercial and Military Semiconductor Devices
JESD99	Terms, Definitions, and Symbols for Microelectronics Devices
JESD100	Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits
JESD670	Quality System Assessment
JESD671	Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems)
MIL- PRF-19500	General Specification for Semiconductor Devices
MIL- PRF-38534	General Specification for Hybrid Microcircuits
MIL- PRF-38535	General Specification for Integrated Circuits (Microcircuits) Manufacturing
NIST Malcolm Baldrige	National Quality Award Criteria
TECHAMERICA EIA681	Assessment Guide for Process Certification

3.8 Reliability Testing – Methods

Number	Title
ECA 186	Passive Electronic Component Parts, Test Methods for; General Instructions and Index of Tests
IEC-60068	Basic Environmental Testing Procedures
EIAJ ED-4701	Environmental and Endurance Test Methods for Semiconductor Devices
IEC-60721	Classification of Environmental Conditions
JEP79	Life Test Methods for Photoconductive Cells
JEP110	Guidelines for the Measurement of Thermal Resistance of GaAs FETS
JEP119	Procedure for Executing SWEAT
JEP121	Requirement for Microelectronic Screening and Test Optimization
JEP122	Failure Mechanisms and Models for Silicon Semiconductor Devices
JEP150	Stress-Test-Driven Qualification Of And Failure Mechanisms Associated With Assembled Solid State Surface-Mount Components
JEP153	Characterization And Monitoring Of Thermal Stress Test Oven Temperatures
JESD22-A100	Cycled Temperature Humidity Bias Life Test
JESD22-A101	Steady State Temperature Humidity Bias Life Test
JESD22-A102	Accelerated Moisture Resistance - Unbiased Autoclave
JESD22-A103	High Temperature Storage Life
JESD22-A104	Temperature Cycling
JESD22-A105	Power and Temperature Cycling
JESD22-A106	Thermal Shock
JESD22-A107	Salt Atmosphere
JESD22-A108	Temperature, Bias, and Operating Life
JESD22-A109	Hermeticity
JESD22-A110	Highly Accelerated Temperature and Humidity Stress Test (HAST)
JESD22-A113	Preconditioning of Plastic Surface-Mount Devices prior to Reliability Testing
JESD28	A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress
JESD33	Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line
JESD35	Procedure for Wafer-Level Testing of Thin Dielectrics
JESD37	Standard Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method
JESD60	A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation at Maximum Gate Current Under DC Stress

3.8 Reliability Testing – Methods (cont'd)

JESD61	Isothermal Electromigration Test Procedure
JESD63	Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature
JESD74	Early Life Failure Rate Calculation Procedure For Semiconductor Components
J-STD-020	Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices
MIL-HDBK-814	Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices FSC 59GP
MIL-STD-750	Test Methods for Semiconductor Devices FSC 5961
MIL-STD-790	Established Reliability and High Reliability Qualified products List (QPL) System for Electrical, Electronic, and Fiber Optic Part Specification
MIL-STD-883	Test Methods Standard Microcircuits
TECHAMERIC A SSB-1.002	Environmental Tests and Associated Failure Mechanisms

3.9 Visual and Mechanical Testing – Methods

Number	Title
AE -Q100-001	Wire Bond Shear Test
AEC-Q100-005	Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test
AEC-Q100-006	Electro-Thermally Induced Parasitic Gate Leakage Test (GL)
AEC-Q100-007	Fault Simulation and Test Grading
AEC-Q100-008	Early Life Failure Rate (ELFR)
AEC-Q100-009	Electrical Distribution Assessment
AEC-Q100-010	Solder Ball Shear Test
AEC-Q100-012	Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems
AEC-Q101-003	Wire Bond Shear Test
AEC-Q101-004	Miscellaneous Test Methods
AEC-Q101-006	Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems
AEC - Q200-001	Flame Retardance Test
AEC - Q200-003	Beam Load (Break Strength) Test
AEC - Q200-004	Measurement Procedures for Resettable Fuses
AEC - Q200-005	Board Flex / Terminal Bond Strength Test

3.9 Visual and Mechanical Testing – Methods (cont'd)

AEC - Q200-006	Terminal Strength (SMD) / Shear Stress Test
AEC - Q200-007	Voltage Surge Test
IEC 60695-1-11	Fire Hazard Testing
IPC J-STD-004	Requirements for Soldering Fluxes
IPC J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
JEITA ED-4702	Mechanical Stress Test Methods for Semiconductor Surface Mounting Devices
JEP84	Recommended Practice for Measurement of Transistor Lead Temperature
JEP110	Guidelines for the Measurement of Thermal Resistance of GaAs FETS
JEP114	Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification
JEP121	Requirement for Microelectronic Screening and Test Optimization
JEP156	Chip-Package Interaction Understanding, Identification And Evaluation
JESD9	Metal Package Specification for Microelectronic Packages and Covers
JESD22-B100	Physical Dimensions
JESD22-B101	External Visual
JESD22-B102	Solderability
JESD22-B103	Vibration, Variable Frequency
JESD22-B104	Mechanical Shock
JESD22-B105	Lead Integrity
JESD22-B106	Resistance to Solder Shock for Through-Hole Mounted Devices
JESD22-B107	Marking Permanency
JESD22-B108	Coplanarity Test for Surface-Mount Semiconductor Devices
JESD22-B111	Board Level Drop Test Method of Components for Handheld Electronic Products
JESD22-B115	Solder Ball Pull
JESD22-B116	Wire Bond Shear Test
JESD22-B117	Solder Ball Shear
MIL-STD-750	Test Methods for Semiconductor Devices
MIL-STD-883	Test Methods and Procedures Microcircuits
UL 94	Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
UL1694	UL Standard for Safety Tests for Flammability of Small Polymeric Component Materials

3.10 PB Component Application – Assembly, Soldering, Board Level Testing

Number	Title
<u>IPC A-600</u>	Acceptability of Printed Boards
<u>IPC A-610</u>	Acceptability of Electronic Assemblies
<u>JEP154</u>	Guideline For Characterizing Solder Bump Electromigration Under Constant Current And Temperature Stress
<u>JESD201</u>	Environmental Acceptance Requirements For Tin Whisker Susceptibility Of Tin And Tin Alloy Surface Finished
<u>JESD22-A121</u>	Measuring Whisker Growth On Tin And Tin Alloy Surface Finishes
<u>JP002</u>	Current Tin Whiskers Theory And Mitigation Practices Guideline
<u>J-STD-001</u>	Requirements for Soldered Electrical and Electronic Assemblies
<u>J-STD-002</u>	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
<u>J-STD-005</u>	Requirements for Soldering Pastes
<u>J-STD-075</u>	Classification of Non-IC Electronic Components for Assembly Processes
<u>TECHAMERICA GEIA-GE0-0002</u>	Reducing the Risk of Tin Whisker-Induced Failures in Electronic Equipment
<u>TECHAMERICA GEIA-HB-0005-1</u>	Program Management/Systems Engineering Guidelines For Managing The Transition To Lead-Free Electronics
<u>TECHAMERICA GEIA-HB-0005-2</u>	Reducing the Risk of Tin Whisker-Induced Failures in Electronic Equipment
<u>TECHAMERICA GEIA-HB-0005-3</u>	Rework/Repair Handbook to Address the Implications of Lead-Free Electronics and Mixed Assemblies in Aerospace and High Performance Electronic Systems
<u>TECHAMERICA GEIA-STD-0005-1</u>	Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder
<u>TECHAMERICA GEIA-STD-0005-2</u>	Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems
<u>TECHAMERICA GEIA-STD-0005-3</u>	Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes
<u>TECHAMERICA GEIA-STD-0006</u>	Requirements for Using Solder Dip to Replace the Finish on Electronic Piece Parts

Annex A (informative) Standards

The standards referenced in this document are in alpha-numeric order with a brief description. They are grouped by the currently maintaining body and do not include revision numbers. Documents beginning with JEP, J-STD, JESD, JS, JEDEC-EIA are JEDEC or joint JEDEC documents.

AEC - Q100**Stress Qualification For Integrated Circuits:**

This document contains a set of failure mechanism based stress tests and defines the minimum stress test driven qualification requirements and references test conditions for qualification of integrated circuits (ICs). These tests are capable of stimulating and precipitating semiconductor device and package failures. The objective is to precipitate failures in an accelerated manner compared to use conditions.

AEC - Q100-001**Wire Bond Shear Test:**

This test establishes a procedure for determining the strength of the interface between a gold ball bond and a package bonding surface, or an aluminum wedge/stitch bond and a package bonding surface, on either pre-encapsulation or post-encapsulation devices. This strength measurement is extremely important in determining two features:

- 1) the integrity of the metallurgical bond which has been formed.
- 2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces.

AEC - Q100-002**Human Body Model (HBM) Electrostatic Discharge Test:**

The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for electronic devices.

AEC - Q100-004**IC Latch-Up Test:**

The purpose of this specification is to establish a reliable and repeatable procedure for performing an IC Latch-Up Test.

AEC - Q100-005**Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test:**

This test is intended to evaluate the ability of the memory array of a standalone Non-volatile Memory (NVM) integrated circuit or an integrated circuit with a Non-volatile Memory module (such as a microprocessor Flash Memory) to: sustain repeated data changes without failure (Program/Erase Endurance), retain data for the expected life of the Non-volatile Memory (Data Retention), and withstand constant temperature with an electrical bias applied (Operating Life).

AEC - Q100-006**Electro-Thermally Induced Parasitic Gate Leakage Test (GL):**

The purpose of this specification is to establish a reliable and repeatable procedure for determining surface mount integrated circuit susceptibility to Electro-Thermally Induced Parasitic Gate Leakage (GL). This specification may also be used as an evaluation tool for determining the susceptibility of circuit designs, molding compounds, fabrication processes, and post mold cure processes to GL.