JEDEC STANDARD

Terms, Definitions, and Letter Symbols for Microelectronic Devices

JESD99B

(Revision of JESD99-A, February 2000)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES

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Foreword

This standard will prove to be a useful guide for users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronic devices. It lists and defines the most common physical and electrical terms applicable to these devices and shows the industry-standard symbols and abbreviations that have been established for such terms.

Where applicable, reference is made to standardization documents of the following organizations:

American National Standards Institute, Inc. (ANSI)
Electronic Industries Association (EIA and JEDEC)
Institute of Electrical and Electronics Engineers (IEEE)
International Electrotechnical Commission (IEC)
National Institute of Standards and Technology (NIST)

The material contained in this standard was formulated under the cognizance of EIA/JEDEC Committee JC-10 on Terms, Definitions, and Symbols and approved by the JEDEC Solid State Technology Council.

The text of this standard is based on JESD99-A dated February 2000, which it replaces, and JEDEC Board ballot JCB-04-48. Annex A briefly shows entries that have been changed.

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SECTION 1: PHYSICAL TERMS

1.1 Definitions of physical terms applicable to integrated circuits in general

ac test: The process of verifying the specified timing of a device.

NOTE Testing of propagation delays, minimum setup and hold times, minimum pulse durations, etc., can be performed by using test vectors applied at specified operating frequency of the device. Propagation delays of critical logic paths for system operation can be measured individually. (Ref. JESD12-1B.)

active device: A device in which at least one circuit element is an active circuit element.

application-specific integrated circuit (ASIC): An integrated circuit developed and produced for a specific application or function and for a single customer.

NOTE ASICs generally use standard cell or gate array design methodology.

application-specific standard product (ASSP): An integrated circuit developed and produced for a specific application or function but made available for multiple customers.

artwork: The original, accurately scaled, oversize drawings and plastic overlays of the microcircuit topological layout that are used to produce the master mask plates.

NOTE Artwork has largely been supplanted by computer-produced drawings and masks.

assembly, microelectronic: An assembly of unpackaged (uncased) microcircuits and/or packaged microcircuits, which may also include discrete devices, so constructed on a packaging interconnect structure that for the purpose of specification, testing, commerce, and maintenance, the package is considered to be an indivisible component. (Ref. JESD30-B.)

NOTE 1 The passive and/or active discrete and microelectronic devices may be mounted on either one or two sides of the packaging interconnect structure, and the external terminals usually exit from one side of the assembly.

NOTE 2 Many package sizes, shapes, and external terminal forms are possible.

asynchronous circuit: A circuit whose changes of state are not controlled by a single clock. (Ref. JESD12-1B.)

autodoping: The introduction of impurities from the substrate into the epitaxial layer during the process of epitaxy.

base (of a package): The part of a package that includes the surface on which a chip is intended to be mounted.

beam lead: A thick-film lead formed on and attached to the chip interconnection pattern and projecting cantilevered beyond the chip periphery for attachment to a substrate.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

bipolar-and-CMOS (BiCMOS) technology: A technology for combining bipolar transistors and silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

bipolar-and-CMOS-and-DMOS (BCD) technology: A technology for combining bipolar transistors, silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices, and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.

bipolar-and-FET (BiFET) technology: A technology for combining bipolar transistors and junction-gate field-effect transistors (JFET) in a single-chip integrated circuit.

bipolar-and-MOS (BiMOS) technology: A technology for combining bipolar transistors and metal-gate metal-oxide-semiconductor (MOS) or metal-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

bipolar technology: A technology for producing devices in which electrical conduction depends on the flow of both majority and minority carriers.

body (of a semiconductor device): The semiconductor portion of a device limited by the physical extent of the crystalline or amorphous semiconductor material and including any associated oxide layers and metallization.

bond, ball: A thermocompression bond in which the attachment wire has been fed through a capillary tube and its exposed end melted into a ball that has been attached under pressure to the bonding pad.

bond, chip: The attachment of the circuit chip to a hybrid or package substrate.

NOTE The attachment serves as a mechanical support, a thermal path, and sometimes an electrical contact.

bond, die: Synonym for “semiconductor chip bond”.

bond, face: A bond directly between a chip bonding pad and a mounting substrate for the purpose of making electrical contact.

bond, stitch: A thermocompression bond in which a capillary tube is used for both feeding the wire and forming the bond.

bond, thermocompression: A bond in which two members are joined through the combined application of heat and pressure.

bond, ultrasonic: A bond in which two members are joined through the combined application of pressure and an ultrasonic oscillatory lateral motion.

bond, wedge: A thermocompression bond in which a wedge-shaped tool is used to apply pressure to the wire being attached.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

bond, wire: The attachment between a bonding wire and a chip bonding pad or package terminal.

bonding wire: A wire that is bonded to a chip bonding pad in order to connect the chip to any other point within the device package.

boundary scan: A design methodology in which the I/O buffers of a circuit or functional block are observed and controlled by scan cells. (Ref. JESD12-1B.)

NOTE The boundary scan standard was developed by the Joint Test Action Group (JTAG) and is embodied in ANSI/IEEE Std 1149-1.

case: Synonym for “package”.

channel: A region of semiconductor material in which current flow is influenced by a transverse electrical field.

NOTE 1 A channel may physically be an inversion layer, a diffused layer, or bulk material.

NOTE 2 The type of channel, i.e., p-channel or n-channel, is determined by the type of majority carrier during conduction.

charge pump: (1) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected in series with that source to make available a voltage greater than that of the source.

NOTE This type of dc-to-dc converter is sometimes called a voltage doubler or, when several stages are cascaded, a voltage multiplier.

(2) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected to make available a voltage whose polarity is opposite to that of the source.

chip: A separated part of a wafer (or, in some cases, a whole wafer) intended to perform a function or functions in a device.

chip, beam-lead: A chip employing electrical terminations in the form of tabs extending beyond the edge of the chip for direct bonding to a mounting substrate.

chip carrier: A package whose chip cavity or mounting area occupies a major fraction of the package area and whose terminals consist of metal pad surfaces (on leadless versions) or leads formed around the sides and under the package or out from the package (on leaded versions).

NOTE The term “chip carrier” has been replaced by “quad flatpack” (for terminals on three or four sides) and “small-outline package” (for terminals on one or two sides).

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

chip, face-down: A chip whose electrical terminations are on the side that is intended to be attached to the mounting substrate.

chip, face-up: A chip whose electrical terminations are on the side opposite the one that is intended to be attached to the mounting substrate.

chip, flip: A chip with bump contacts spaced around the device and intended for face-down mounting.

circuit element: Any constituent part of a circuit that contributes directly to its operation and performs a definable function.

NOTE 1 Examples include transistors, resistors, capacitors, inductors, and interconnections.

NOTE 2 The definition in JESD12-1B excludes interconnections.

circuit element, active: A circuit element that contributes qualities to a circuit function other than those contributed by a passive circuit element, e.g., rectification, switching, gain, or conversion of energy from one form to another.

NOTE 1 Examples include diodes, transistors, active integrated circuits, and light-sensing or light-emitting devices.

NOTE 2 Active physical circuit elements may also be used to act as passive physical circuit elements, e.g., to provide resistance and/or capacitance to a circuit function.

circuit element, parasitic: A circuit element that is an unavoidable adjunct of one or more other circuit elements.

circuit element, passive: A circuit element primarily contributing resistance, capacitance, inductance, ohmic interconnection, or a combination of these to a circuit function.

NOTE Examples include resistors, capacitors, inductors, passive filters, and interconnections.

clock distribution network: The structure by which clock signals are distributed within a device. (Ref. JESD12-1B.)

clock skew: The difference in the arrival times of a common clock edge at any two circuit elements. (Ref. JESD12-1B.)

CMOS-and-DMOS (C/DMOS) technology: A technology for combining complementary metal-oxide-semiconductor (CMOS) field-effect devices and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

complementary integrated circuit technology: The technology, as applied to integrated circuits, whereby active elements of both polarities are fabricated as single-chip elements on or within the same substrate.

NOTE For example, a complementary bipolar semiconductor integrated circuit is one that employs both npn and pnp bipolar transistors in the same semiconductor substrate, and a complementary MOS integrated circuit is one that employs both n-channel and p-channel field-effect transistors in the same semiconductor substrate.

complementary metal-oxide semiconductor (CMOS) technology: A technology for combining p-channel and n-channel metal-oxide-semiconductor field-effect transistors in a single-chip integrated circuit.

component (of a hybrid integrated circuit): A part that is mounted within the package and that contributes to the composition of the circuit.

NOTE For electronic components, a distinction is made between integrated components and discrete components.

component, active (of a hybrid integrated circuit): A component in which at least one circuit element is an active circuit element.

component, discrete (of a hybrid integrated circuit): A discrete device that serves as a component of a hybrid integrated circuit.

component, integrated (of a hybrid integrated circuit): An integrated circuit, completed or partially completed, that serves as a component of a hybrid integrated circuit.

component, passive (of a hybrid integrated circuit): A component in which all circuit elements are passive.

connection, electrical (within a semiconductor device): An electrically conducting element that functions as a pathway between other elements, including terminals, and whose primary purpose is to conduct electric current in a confined manner.

NOTE The connection may either consist of a separate conductive entity such as a wire or metallic film or be an integral part of the body.

contact, bump; ball contact; raised pad; pedestal: (1) A contacting pad that rises substantially above the surface level of the chip.

(2) A raised pad on the substrate that contacts a flat land area of the chip.

critical path: A signal path that determines the performance of a design.

crossover: A crossing where a portion of an interconnect pattern passes over a portion of another interconnect pattern and is separated from it by a thin dielectric layer.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

crossunder: A crossing where a conductive path fabricated into the active substrate for the sole purpose of interconnection passes under a portion of an interconnect pattern and is separated from it by a thin dielectric layer.

customer-specific standard product (CSSP): An integrated circuit developed and produced for a single customer but for multiple applications or functions.

custom integrated circuit: An integrated circuit developed or produced to conform to unique requirements.

NOTE The terms “full custom” and “semicustom” refer to layout methodologies. The choice of term is subjective, depending on the interpretation of the ratio of unique layouts to standard macrocell layouts from a library.

dc test: A test during which only steady-state voltages and currents are applied to the device.

NOTE DC tests are generally used to determine input levels, output levels, or dissipation characteristics of devices.

deposition: The process of applying a material to a substrate by means of vacuum, electrical, chemical, screening, or vapor methods.

deposition, vapor-phase: The deposition of conductive, resistive, insulating, or semiconductor films onto a substrate from a source material in the vapor phase by physical deposition or chemical reaction.

die (pl. dice): Synonym for “chip”.

diffusion, impurity: A process used to introduce desired impurities into a semiconductor crystal to alter its electrical properties; it is accomplished by introducing suitable dopants to the surface of the semiconductor wafer under precisely controlled conditions, usually at high temperatures.

diode, barrier: Synonym for “diode, Schottky”.

diode, hot-electron: Synonym for “diode, Schottky”.

diode, Schottky: A diode formed by depositing a metal film on a semiconductor surface of sufficiently high resistivity to form an energy barrier.

NOTE A Schottky diode is sometimes used as part of a bipolar transistor structure.

diode, semiconductor: In its simplest form, any p-n junction but, in microcircuits, often a modified bipolar transistor.

NOTE Modifications include shorting the base to the collector, shorting the emitter to the collector, using the emitter-base diode with the collector open, or using the collector-base diode with the emitter open.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

discrete (semiconductor) device: A semiconductor device that is specified to perform an elementary electronic function and is not divisible into separate components functional in themselves.

NOTE 1 Diodes, transistors, rectifiers, thyristors, and multiple versions of these devices are examples. Other semiconductor structures having the physical complexity of integrated circuits but performing elementary electronic functions (e.g., complex Darlington transistors) are usually considered to be discrete semiconductor devices.

NOTE 2 If a semiconductor device is not considered to be an integrated circuit in both complexity and functionality, it is considered to be a discrete device.

discretionary wiring: A technique for interconnecting subarrays on a single wafer in which each subarray is electrically tested by probing and the desired array function is attained by the use of a metallization pattern that connects only usable subarrays.

dislocation: An atomic imperfection or fault in the crystalline lattice structure.

NOTE 1 The two types are edge dislocations (if a row of atoms is removed or displaced and the slippage is at right angles to the displacement) and screw dislocations (if the slippage is parallel).

NOTE 2 If dislocations appear at the surface of the crystal, they are sometimes referred to as surface dislocations.

dopant: A chemical element that is introduced into the lattice structure as an impurity to form desired properties.

NOTE Examples are phosphorus and boron used to create n- and p-regions, respectively, in silicon.

double-diffused MOS (DMOS) technology: A technology for producing silicon-gate metal-oxide semiconductor field-effect transistors such that 1) the threshold voltage, V_T, is determined by the intersection of two doping profiles, and 2) the device channel length is defined by the diffusion characteristics rather than by a photolithographic self-aligned gate structure.

electrode (of a semiconductor device): An element that performs one or more functions of emitting or collecting electrons or holes, or of controlling their movements by an electric field.

electrostatic-discharge-sensitive device: A discrete device or integrated circuit that may be permanently damaged by electrostatic potentials encountered in routine handling, testing, and shipping.

NOTE In documents of the IEC and CENELEC, the abbreviation ESDS stands for “electrostatic-discharge-sensitive device”; in the USA, ESDS stands merely for “electrostatic discharge sensitive” or “electrostatic discharge sensitivity”, and “ESDS device” is not further abbreviated. The abbreviation ESD stands for “electrostatic discharge”.

element, distributed circuit: The physical realization of an element incorporating more than one primary electrical characteristic (resistance, capacitance, inductance, gain, etc.) dispersed along the length of the element.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

embedding: A process using polymers or similar materials that can be hardened to produce a body enclosing, and in contact with, the electronic assembly, for example, casting, potting, dip-coating, and transfer molding.

epitaxial layer: A monocrystalline layer formed by epitaxy, which is normally of a different conductivity type or resistivity from the substrate material.

epitaxial peak: An irregular raised point of epitaxial material on an epitaxial surface.

epitaxy: Deposition of a monocrystalline layer of material on a substrate material such that the layer thus formed has the same crystal orientation as the substrate.

NOTE Examples are silicon on silicon and silicon on sapphire.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

etch pit: A small peak or hole produced by chemical etching at the site of an imperfection in a semiconductor or other surface and caused by the differing etch rate at the point of imperfection.

etchant: A solution used for etching.

etching: A process in which a controlled quantity or thickness of material is removed (often selectively) from a surface by chemical reaction, electrolysis, or other means.

etching, plasma: A process in which material is removed by a reaction with chemically active radicals created by an ion bombardment in a glow discharge.

NOTE A mask is usually used in order to remove only selected areas.

fan-in: The number of output ports on a net. (Ref. JESD12-1B.)

fan-out: The number of input ports on a net. (Ref. JESD12-1B.)

fault coverage: The percentage of possible faults detected by a set of test vectors. (Ref. JESD12-1B.)

fault simulation: The process of applying test vectors to a circuit or circuit model to obtain fault-coverage information. (Ref. JESD12-1B.)

film (of a film integrated circuit): A layer of solid material formed by any deposition process upon the substrate or upon other films deposited on the substrate.

film, plated: A film obtained through chemical and/or electrochemical deposition.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

film technology, thick-: The technology with which electronic circuits or elements are formed by applying a liquid, solid, or paste coating through a screen or mask in a selective pattern onto a supporting material.

NOTE This technology also includes films deposited by any other means when the films so formed are five micrometers or greater in thickness.

film technology, thin-: The technology with which electronic circuits or elements are formed by vapor deposition, vacuum deposition, or sputtering of films onto a supporting material.

NOTE This technology also includes similar techniques when the films so formed are less than five micrometers in thickness.

film, thick (of a film integrated circuit): A film produced by a printing process, serigraphy, or other related techniques.

film, thin (of a film integrated circuit): A film produced by an accretion process such as vapor-phase deposition or sputtering.

firing: A process of thick-film formation whereby the screened film is subjected to a precisely controlled high-temperature condition that oxidizes and vaporizes organic binders and modifies the film microstructure to achieve desired properties, including adherence to the substrate.

fixed interconnect pattern: A metallization pattern that interconnects circuit elements and is defined by a single, predesigned mask.

flatpack: A package whose leads project parallel to, and are designed primarily to be attached parallel to, the seating plane. (Ref. JESD30C.)

NOTE The term “flatpack” has been replaced by “quad flatpack” (for terminals on three or four sides) and “small-outline package” (for terminals on one or two sides).

floating node: A signal line that is not actively forced to a defined high or low level. (Ref. JESD12-1B.)

NOTE In a high-impedance state, the charge (or lack of charge) is trapped at the node with no path to supply or ground voltages.

foil: A relatively thin layer of solid material that can be handled independently of a substrate.

functional block: A part of a circuit having a defined function that can be designated by a single symbol in a schematic representation. (Ref. JESD12-1B.)

functional density: The number of gates used divided by the entire chip area. (Ref. JESD12-1B.)

NOTE Units are gates used per unit area.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

functional simulation: The process of exercising a particular netlist and functional models by applying input stimuli to observe the functional responses without regard to timing. (Ref. JESD12-1B.)

functional test: The process of verifying the specified functions of a device without regard to timing. (Ref. JESD12-1B.)

gate equivalency of a function (GEF): The number of gate equivalents used to implement a function. (Ref. JESD12-1B.)

gate equivalent (for CMOS): The minimum circuitry necessary to implement a two-input NAND gate. (Ref. JESD12-1B.)

gate equivalent (for ECL): One-eleventh of the minimum circuitry necessary to implement a single-bit full-adder. (Ref. JESD12-1B.)

gate, (logic): A combinational logic function consisting of a number of inputs and outputs and performing one of the Boolean functions AND, OR, exclusive OR, NAND, NOR, or exclusive NOR.

NOTE For the purpose of specifying complexity, (1) buffers and inverters are counted as gates and (2) exclusive OR and exclusive NOR gates, some high-input-count gates, and memory functions are counted as multiple gates.

geometry, process: The minimum allowable drawn dimensions for designing an integrated circuit using a specified technology. (Ref. JESD12-1B.)

heat sink; heat dissipator: A separable element or integral part of the package that aids in dissipating the heat produced within the package.

integrated circuit (IC): A circuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purposes of construction and commerce. (Ref. IEC 748-1.)

NOTE 1 JEDEC and IEC standards on semiconductor integrated circuits generally refer to integrated circuits that are designed as microcircuits.

NOTE 2 To further define the nature of an integrated circuit, additional qualifiers may be prefixed. Examples include

– single-chip integrated circuit,

– multichip integrated circuit,

– thin-film integrated circuit,

– thick-film integrated circuit,

– hybrid film integrated circuit, and

– hybrid semiconductor integrated circuit.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

integrated circuit, active hybrid film: A hybrid film integrated circuit in which at least one circuit element is active.

integrated circuit, analog: A type of linear integrated circuit intended to be used so that the output is a continuous mathematical function of the input.

NOTE An operational amplifier is an example of an analog integrated circuit.

integrated circuit, application-specific: See “application-specific integrated circuit”.

integrated circuit, binary: A digital integrated circuit limited to two logic states at each of its input and output terminals.

NOTE The high-impedance state of a three-state output is not considered to be a logic state.

integrated circuit, custom: See “custom integrated circuit”.

integrated circuit, digital: A type of integrated circuit that is intended to accept particular logic states, changes between logic states, or sequences of logic states at its input terminals, and convert these to logic states at its output terminals according to a set of logic equations or function tables.

integrated circuit, film (FIC): An integrated circuit whose circuit elements, including the interconnections, are exclusively film elements formed on the surface of an insulating substrate.

integrated circuit, hybrid (HIC): An integrated circuit that contains two or more of a single type or a combination of types of the following elements, with at least one of the elements being active: film microcircuit, monolithic microcircuit, discrete semiconductor device, passive chip, or passive element printed or deposited on a substrate. (Ref. JESD93.)

integrated circuit, hybrid film: A film integrated circuit in which the main parts of the circuit elements are produced as film elements on a substrate and that is completed by mounting additional components on the substrate or elsewhere in the package.

integrated circuit, hybrid semiconductor: A semiconductor integrated circuit in which the main parts of the circuit elements are produced as semiconductor circuit elements and that is completed by mounting additional components in the package.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

integrated circuit, interface: An integrated circuit that accomplishes the linkage of two systems or parts of a system that would otherwise be incompatible.

NOTE The signals present at the inputs and the outputs of the interface integrated circuit may take any one of the following forms:

a) digital inputs, analog outputs;

b) analog inputs, digital outputs;

c) analog inputs, analog outputs; or

d) digital inputs, digital outputs. (In this case, the levels of the digital signals at the inputs and the outputs are dissimilar.)

Some circuits of types a, b, and c may also be classified as linear integrated circuits.

integrated circuit, linear: Through common usage, an integrated circuit that is not purely digital.

NOTE Some circuits of this type may also be classified as interface integrated circuits.

integrated circuit, monolithic (semiconductor): Deprecated synonym for “integrated circuit, single-chip”.

integrated circuit, multichip: A semiconductor integrated circuit containing two or more chips (dice).

NOTE The use of the term “polylithic semiconductor integrated circuit” is deprecated.

integrated circuit, pad-limited: An integrated circuit whose chip size is determined by the number of pads required. (Ref. JESD12-1B.)

integrated circuit, passive hybrid film: A hybrid film integrated circuit in which all circuit elements are passive.

integrated circuit, semiconductor: A semiconductor device designed as an integrated circuit.

integrated circuit, silicon-compiled: An integrated circuit generated entirely by a silicon compiler. (Ref. JESD12-1B.)

integrated circuit, single-chip: An integrated circuit or microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate. (Ref. JESD93.)

integrated circuit, thick-film: A film integrated circuit whose circuit elements are thick-film elements.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

integrated circuit, thin-film: A film integrated circuit whose circuit elements are thin-film elements.

NOTE Usually, thin-film elements are formed by vacuum-deposition techniques, possibly supplemented by other deposition techniques.

integrated circuit, very-high-speed (VHSIC): An integrated circuit meeting the following goals for speed and density established by the U.S. Department of Defense:

Goal	Phase 1	Phase 2
Minimum product of operating frequency and equivalent gate density	5×10^{11} Hz C gates / cm^2	1×10^{13} Hz C gates / cm^2
Minimum clock frequency	25 MHz	100 MHz

interconnect layer: A conductive layer used for electrical interconnection of circuit elements on an integrated circuit. (Ref. JESD12-1B.)

ion implantation: A method for doping semiconductors wherein the desired dopant is ionized and accelerated by an electric field, penetrates the surface, and is deposited within the semiconductor material.

isolation, dielectric: Electrical isolation of one or more elements of a single-chip semiconductor integrated circuit, achieved by surrounding the elements with an insulating barrier such as semiconductor oxide.

isolation, junction: Electrical isolation of one or more elements of a single-chip semiconductor integrated circuit, achieved by surrounding the element(s) with a region of the conductivity type that forms a junction and reverse-biasing that junction.

layer, accumulation: A surface region of a semiconductor device whose conductivity type is the same as that produced by the net fixed charge density of ionized donors and acceptors and whose net carrier density is higher than that necessary for neutralization due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

layer, buried: A distinguishable region introduced under a semiconductor circuit element, for example, under the collector region of a transistor to reduce the series collector resistance.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

layer, depletion (associated with a surface): A surface region of a semiconductor device whose conductivity type is the same as that produced by the net fixed charge density of ionized donors and acceptors but whose net carrier density is insufficient for neutralization due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

layer, depletion (associated with a p-n semiconductor junction): A region whose conductivity type on each side of the junction is the same as that produced by the net fixed charged density of ionized donors and acceptors but whose net carrier density is insufficient for neutralization due to the built-in potential barrier of the p-n junction and, if present, an applied reverse bias.

layer, diffused: The region of a semiconductor into which impurity dopants have been diffused to a concentration of at least the background concentration.

NOTE The region is often delineated by a p-n junction.

layer, enhancement: Synonym for “accumulation layer”.

layer, inversion: A surface region of a semiconductor device whose conductivity type has been reversed from that produced by the net fixed charge density of ionized donors and acceptors due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

lead frame (of a package): A metal frame providing external terminals and mechanical support to align them.

load, input: The load (usually specified in unit loads) represented by a given input. (Ref. JESD12-1B.)

load, output: The load on an output (usually specified in unit loads). (Ref. JESD12-1B.)

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

logic feedback: A circuit configuration in which the output of a logic circuit controls an input signal to the same circuit. (Ref. JESD12-1B.)

LSI: Large-scale integration.

mask: A patterned screen of any of several materials and types used in shielding selected areas of a semiconductor, photosensitive layer, or substrate from radiation during processing, so that the unshielded areas can be further processed to reproduce the chosen pattern.

NOTE The type of mask can be designated either by type (e.g., oxide mask or metal mask) or by function (e.g., diffusion mask or vapor-deposition mask).

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

master slice: An unmetalized wafer containing arrays of circuit elements as determined by subsystem requirements.

NOTE These circuit elements can be interconnected in a variety of ways to achieve different functions.

metal-insulator-semiconductor (MIS) technology: A technology for producing circuits and circuit elements having the form of a semiconductor-insulator-metal layered structure.

NOTE Field-effect transistors, capacitors, varactors, nonlinear resistors, variable-threshold diodes, and similar circuit elements can be produced with this technology.

metallization: A thin-film conductor or network of such conductors used to interconnect microcircuit elements.

metallization, bottom: The metallization on the bottom surface of a chip that permits bonding it to a mounting substrate.

metallization, multilayer: A metallization pattern in which the conductive network is fabricated in more than one plane and separated, except at desired contact points, by thin dielectric films.

metal-nitride-oxide-semiconductor (MNOS) technology: A subcategory of metal-insulator-semiconductor (MIS) technology in which the insulation employed is a nitride-oxide layer.

metal-oxide-semiconductor (MOS) technology: A subcategory of metal-insulator-semiconductor (MIS) technology in which the insulator employed is an oxide of the semiconductor substrate material.

NOTE The term MOS is often misused to include other categories of insulated-gate technology such as MNOS (metal-nitride-oxide-semiconductor) and SIS (silicon-gate-insulator-semiconductor).

microcircuit: A microelectronic device that has a high circuit-element and/or component density and that is considered to be a single unit. (Ref. IEC 748-1.) (See also “integrated circuit”.)

microcircuit, analog: Synonym for “integrated circuit, analog”.

microcircuit, binary: Synonym for “integrated circuit, binary”.

microcircuit, digital: Synonym for “integrated circuit, digital”.

microcircuit, film: Synonym for “integrated circuit, film”.

microcircuit, hybrid: Synonym for “integrated circuit, hybrid”.

microcircuit, interface: Synonym for “integrated circuit, interface”.

microcircuit, linear: Synonym for “integrated circuit, linear”.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

microcircuit, logic: Synonym for “integrated circuit, digital”.

microcircuit module: An assembly of microcircuits, or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions and so constructed that, for the purpose of specification, testing, commerce, and maintenance, it is considered to be indivisible.

microcircuit, multichip: Synonym for “integrated circuit, multichip”.

microelectronics: That field of science and engineering that deals with highly miniaturized electronic components and their use. (Ref. IEC 748-1.)

minimization: The process of eliminating redundancy in logic implementation. (Ref. JESD12-1B.)

model: A representation of an electronic circuit. (Ref. JESD12-1B.)

morphology, integrated: The structural characterization of an electronic component in which the current- or signal-modifying areas, patterns, or volumes have lost their identities in the integration of electronic materials, in contrast to an assembly of devices performing the same function.

morphology, translational: The structural characterization of an electronic component in which the areas or patterns of resistive, conductive, dielectric, and active materials in or on the surface of the structure can be identified in a one-to-one correspondence with devices assembled to perform an equivalent function.

MSI: Medium-scale integration.

multilayer(-connection) film circuit: A circuit having more than one layer of film interconnections separated by at least one insulating film or gap.

no (internal) connection (NC): A terminal that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of the wiring) does not exceed the highest supply voltage rating of the circuit.

NOTE 1 If higher voltages are acceptable, this should be stated.

NOTE 2 The IEC equivalent term is “blank terminal”; nevertheless, the IEC abbreviation is NC.

nonusable terminal (NU): A terminal that is not to be used in normal applications and that may or may not have an internal connection.

optimization (of logic): The process by which a given logic representation is reduced to a superior equivalent functional representation with respect to some system or chip-level design objective such as speed, device utilization, level of logic, etc. (Ref. JESD12-1B.)

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

oxide, deposited: An oxide layer formed on a surface by methods not requiring the substrate to participate in the reaction.

NOTE Various methods such as pyrolysis, evaporation, or sputtering may be employed.

oxide, grown: An oxide layer formed on a semiconductor surface by the reaction of the semiconductor material with oxygen.

oxide step: A sharp variation of the plane of the oxide on the surface of a planar device.

package (of a semiconductor device): An enclosure for one or more semiconductor chips (dice), film elements, or other components, that allows electrical connection and provides mechanical and environmental protection.

pad, bonding: An area on a chip to which a connection can be made.

pad cell area: The physical area available for external electrical and mechanical interface. (Ref. JESD12-1B.)

parametric test: The process of verifying the specified dc parameters of a device. (Ref. JESD12-1B.)

passivation: The formation of an insulating layer directly over a semiconductor surface to protect the surface from contaminants, moisture, and particles.

NOTE Usually an oxide of the semiconductor is used; however, deposition of other materials is also used.

passive device: A device in which all circuit elements are passive.

photoresist: A photosensitive film used in conjunction with photolithography forming a protective mask on a wafer or substrate surface to effect selective process action (e.g., diffusion, etching, etc.).

pinhole: An imperfection in the form of a small hole that penetrates through a layer of material. (Ref. IPC-T-50.)

planar (device and **process):** A type of semiconductor device and the process technology used to fabricate it, in which all of the p-n junctions terminate at approximately the same geometric plane on the surface of the semiconductor.

NOTE Devices using similar technologies, but having one or more diffused areas lying in a slightly different, parallel plane, are also considered planar (e.g., buried collector).

protective coating: A layer of insulating material applied over the circuit elements for the purpose of mechanical and environmental protection and prevention of contamination.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

radiation hardening: (1) Increasing the ability of a device to survive one or more types of radiation.

(2) The process whereby the ability of a device to survive one or more types of radiation is increased.

reactive ion etching (RIE): A plasma etching process using a relatively low gas pressure and high electric field, in which material is removed primarily by chemical reaction with active radicals although some material may also be removed physically by ion bombardment.

NOTE 1 A mask is usually used in order to remove only selected areas.

NOTE 2 By convention the wafer is mounted on the “hot” RF electrode.

registration mark; alignment mark; fiducial mark: A mark, on a wafer or substrate, that is used for aligning successive processing masks.

resistor, bulk-collector: A semiconductor resistor formed by isolating a region of the epitaxial material that, in other regions, forms the collectors of the transistors.

resistor, diffused: The normal semiconductor resistor formed by diffusing a junction-isolated region of proper length, width, and sheet resistance to provide the desired resistance value.

resistor, film: A resistor formed by deposited films, usually metal, on an insulating substrate or the semiconductor oxide on an integrated-circuit chip surface.

resistor, pinch: A semiconductor resistor formed by diffusing the opposite conductivity type, normally during the emitter diffusion, into a portion of the diffused resistor length in order to obtain a very high sheet resistance.

scan cell: A bistable element that includes one or more ports used to observe and control that element's state when the port or ports are enabled. (Ref. JESD12-1B.)

scan, full: A methodology of design in which every bistable element is a scan cell. (Ref. JESD12-1B.)

scan, partial: A methodology of design in which some, but not all, bistable elements are scan cells. (Ref. JESD12-1B.)

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

Schmitt trigger: A digital circuit designed to have significant hysteresis, i.e., the difference between the positive-going and negative-going input threshold voltages, and usually having only one input.

NOTE Schmitt triggers have one hysteresis-causing mechanism. Sometimes this mechanism is applied to a single transistor having multiple inputs and performing a basic logic function as in a TTL NAND gate. These gates have been called NAND Schmitt triggers. It is necessary for all their inputs to be simultaneously above the positive-going threshold voltage to cause the output to go high.

Other integrated circuits have one or more inputs each having its own hysteresis-causing mechanism. These are not usually called Schmitt triggers per se. A NAND gate each of whose inputs separately has hysteresis might be called a NAND gate with Schmitt-trigger inputs.

The latter device differs from the NAND Schmitt triggers in that one input at a time can reach its positive-going threshold voltage, then drop back staying above the negative-going threshold voltage. When the last input reaches its positive-going threshold voltage, the output goes low.

screen-printing (of a thick-film circuit): The deposition of conductive, resistive, or insulating films onto a substrate by pressing pastes (“inks”) through screens.

semiconductor device (general term)**:** A device whose essential characteristics are due, in whole or in part, to the flow of charge carriers within a semiconductor.

NOTE For specification purposes, a semiconductor device must be considered to be either a discrete semiconductor device or an integrated circuit.

semiconductor (material) (within a semiconductor device): A material in which the electric current is made up of both negative and positive mobile charge carriers (conduction electrons and holes).

semiconductor (nonspecific)**:** A substance whose conductivity due to the charge carriers of both signs is normally in the range between that of metals and insulators and in which the charge carrier density can be changed by external means.

sheet resistance: The electrical resistance of a diffused layer or of a thin sheet of material with uniform thickness as measured across opposite sides of a square pattern.

NOTE Sheet resistance is usually expressed in ohms per square.

signal, analog: A signal that is used in such a manner that any change in magnitude of some characteristic conveys information.

NOTE The characteristic may be the amplitude, phase, frequency, etc., of a quantity such as voltage, current, impedance, etc.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

signal, digital: A signal that is used in such a manner that changes between ranges in a finite set of nonoverlapping ranges of the magnitude of some characteristic convey information.

NOTE 1 The characteristic may be the amplitude, phase, frequency, etc., of a quantity such as voltage, current, impedance, etc.

NOTE 2 For convenience, each range of values can be represented by a single value, i.e., the nominal value.

silicon-gate-insulator-semiconductor (SIS) technology: A technology similar to metal-insulator-semiconductor (MIS) technology except that the gate is silicon instead of metal.

silicon-nitride-oxide-semiconductor (SNOS) technology: A subcategory of silicon-gate-insulator-semiconductor (SIS) technology in which the insulation employed is a nitride-oxide layer.

silicon-on-sapphire (SOS) technology: The technology whereby monocrystalline films of silicon are epitaxially deposited onto a single-crystal sapphire substrate to provide the basic structure for the fabrication of dielectrically isolated active and/or passive elements.

silicon-oxide-nitride-oxide-semiconductor (SONOS) technology: A subcategory of silicon-gate-insulator-semiconductor (SIS) technology in which the insulation employed is an oxide-nitride-oxide layer.

space-charge region (of a semiconductor device): A functional region in which the net charge density is significantly different from zero. (Ref. ANSI/IEEE Std 100.)

NOTE 1 The net charge is caused by electrons, holes, and ionized acceptors and donors.

NOTE 2 The space-charge regions of a semiconductor device include accumulation (enhancement), depletion, and inversion layers.

sputter cleaning; back sputtering: A process in which material is physically removed from a designated surface by bombardment of ions generated in a plasma.

NOTE The gas used is generally inert or nonreactive, e.g., argon or helium.

sputtering: A process for forming thin films in which ion bombardment is used to free particles from a solid source that are then deposited onto another nearby surface.

SSI: Small-scale integration.

standard product, (integrated circuit): An integrated circuit developed and produced for multiple applications or functions and made available for multiple customers.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

subelement: A distinguishable portion of a microcircuit element.

EXAMPLE The emitter, collector, and base of an integrated bipolar transistor are subelements of an integrated circuit.

substrate (of a film integrated circuit): A piece of material forming a supporting base for film circuit elements and possibly additional components.

substrate (of a semiconductor device): (1) The part of the original material that remains essentially unchanged when the device elements are formed upon or within the original material.

NOTE 1 The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

(2) The original semiconductor material being processed.

NOTE 2 The intended meaning will usually be clear from the context in which the term is used. If necessary, distinction can be made between the “original substrate” and the “remaining substrate”.

substrate, active: A substrate in which active elements are implemented within the substrate material.

substrate, passive: A substrate that serves primarily as a structural support or mounting surface for functional circuit elements.

surface state: The energy levels associated with charge that resides on the surface of a semiconductor.

surface-state charge density: The net charge density on the surface of a semiconductor.

NOTE Both the charge density and the energy levels may be influenced by such factors as the insulation layer, surface discontinuities, chemicals, ultraviolet radiation, and electrical or magnetic fields.

synchronous circuit: A circuit whose changes of state are controlled by a single clock signal. (Ref. JESD12-1B.)

terminal (of a semiconductor device): An externally available point of connection.

NOTE The use of the term “termination” as a synonym is deprecated because that term denotes the external elements connected to the terminal.

tester strobe time: The time interval from the beginning of a test clock cycle to the instant when an output of a device is observed and compared to an expected result. (Ref. JESD12-1B.)

test pattern: A circuit or elements processed in the semiconductor wafer to act as test sites for monitoring fabrication processes.

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

three-state bus: A bus on which each output port can be placed at a logic high level or a logic low level or in a high-impedance state. (Ref. JESD12-1B.)

topology: The surface layout design of a microcircuit, applied chiefly to the preparation of the masks used in fabrication.

transistor, bipolar: A transistor in which electrical conduction depends on the flow of both majority and minority carriers.

transistor, collector field-effect: A modified junction field-effect transistor, used as a constant-current source, whose gate is connected to the substrate.

NOTE The channel is formed from the epitaxial material that in other regions forms the collectors of the bipolar transistors.

transistor, field-effect (FET): A transistor in which the conduction is due entirely to the flow of majority carriers and can be varied by an electric field produced by an auxiliary source.

transistor, insulated-gate field-effect (IGFET): A field-effect transistor having one or more gate electrodes that are electrically insulated from the channel.

transistor, junction-gate field-effect (JFET): A field-effect transistor having one or more gates that form p-n junctions with the channel.

transistor, lateral: A transistor whose emitter-base and collector-base junctions are formed in separate topological areas of a microcircuit and in which the charge carriers flow between these junctions in a plane parallel to the surface.

transistor, metal-oxide-semiconductor field-effect (MOSFET): An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material.

transistor, substrate pnp: A pnp transistor formed from the base and collector regions of a normal npn bipolar transistor and the substrate.

transistor, unipolar: A transistor in which the electrical conduction is due entirely to the flow of majority carriers.

undercut: The reduction of the cross section of a material caused by etching action spreading beneath the edge of the photoresist or other masking films.

unipolar technology: A technology for producing devices in which electrical conduction is due entirely to the flow of majority carriers.

untestable circuit: A circuit that contains logic functions that cannot be tested because of the lack of controllability or observability. (Ref. JESD12-1B.)

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1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

via: An electrically conducting path that passes through an insulating material and connects conducting layers in two or more planes.

VLSI: Very-large-scale integration.

wafer: A slice or flat disk, either of semiconductor material or of such a material deposited on a substrate, in which circuits or devices are simultaneously processed and subsequently separated into chips if there is more than one device.

window: A hole formed by etching through an oxide or insulating layer on a semiconductor for the purpose of diffusion into or deposition onto a selected area of the semiconductor.

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits

array density (of a gate array): The number of available gates divided by the entire chip area. (Ref. JESD12-1B.)

NOTE Units are gates per unit area.

array, logic: Synonym for “gate array integrated circuit”.

available gates (in a gate array): The total number of potentially usable, unconnected gate equivalents in a given array area. (Ref. JESD12-1B.)

behavioral description: The algorithms or equations defining a function. (Ref. JESD12-1B.)

cell-based integrated circuit: An integrated circuit fabricated with a unique full set of mask information and comprising one or more macrocells that can be selectively placed and interconnected to perform an electrical function. (Ref. JESD12-1B.)

cell compiler: A tool that automatically generates the physical layout to meet the specified parameters and that may generate a symbol and timing and functional models. (Ref. JESD12-1B.)

channeled gate array: A gate array configuration that contains a predetermined and dedicated area for logic interconnection. (Ref. JESD12-1B.)

channelless gate array: A gate array configuration that contains no predetermined and dedicated area for logic interconnection. (Ref. JESD12-1B.)

core-limited integrated circuit: An integrated circuit whose chip size is determined by the gate core area required for functional implementation. (Ref. JESD12-1B.)

design module: A software description of a functional block describing its function and performance. (Ref. JESD12-1B.)

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1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

device-level description: A structural description using circuit elements as primitives. (Ref. JESD12-1B.)

distributed delay model: A model constructed from primitive models, each having specified delay. (Ref. JESD12-1B.)

embedded gate array: A gate array masterslice in which some of the array circuit elements are replaced by one or more cell-based functions. (Ref. JESD12-1B.)

field-programmable gate array (FPGA): A gate array integrated circuit that can be electrically programmed. (Ref. JESD12-1B.)

field-programmable logic array (FPLA): Synonym for “programmable logic array”.

field-programmable logic sequencer (FPLS): Synonym for “programmable logic sequencer”.

flattened [nonhierarchical] layout: A geometric description in which all geometrics are contained at the lowest hierarchical level. (Ref. JESD12-1B.)

flattened [nonhierarchical] netlist: A netlist in which all logic elements are connected at the lowest hierarchical level. (Ref. JESD12-1B.)

floorplanning: The process of defining the physical placement of circuit elements. (Ref. JESD12-1B.)

functional library: The functional models of a set of macros. (Ref. JESD12-1B.)

gate array integrated circuit: A digital integrated circuit containing a fixed topology of circuit elements used to form macrocells and macro functions that are or can be interconnected to implement a logic function. (Ref. JESD12-1B.)

gate capacity (of a gate array): Synonym for “usable gates”. (Ref. JESD12-1B.)

gate core area (of a cell-based integrated circuit): The physical area occupied by the logic gates and intercell routing excluding the pad cell area. (Ref. JESD12-1B.)

gate core area (of a gate array): The physical area occupied by the available logic gates and intercell routing excluding the pad cell area. (Ref. JESD12-1B.)

gate core density (of a cell-based integrated circuit): The number of gates in the gate core area divided by the gate core area. (Ref. JESD12-1B.)

NOTE Units are gates per unit area.

gate core density (of a gate array): The number of available gates in the gate core area divided by the gate core area. (Ref. JESD12-1B.)

NOTE Units are gates per unit area.

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1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

gate-level description: A structural description using logic gates as primitives. (Ref. JESD12-1B.)

gate utilization (in a gate array): The ratio of the number of used gates to available gates.

NOTE Gate utilization is usually expressed as a percentage.

geometric description: A representation of a function in terms of its physical implementation. (Ref. JESD12-1B.)

hard macro: Synonym for "macrocell".

hardware accelerator: A system using software-configurable hardware to speed up software models that are used to model the network being simulated. (Ref. JESD12-1B.)

NOTE The objective is to achieve faster simulation than can be achieved with software simulators.

hierarchical description: A description containing two or more nested levels of primitives. (Ref. JESD12-1B.)

hierarchical layout: The layout of a design that exists in multiple hierarchical levels. (Ref. JESD12-1B.)

interactive layout: The manual modification or influence used in the pattern layout, cell placement, or interconnect routing in an otherwise automatic layout tool. (Ref. JESD12-1B.)

logic synthesis: The process of transforming behavioral, structural, or register-transfer-level descriptions into structural descriptions based on a given set of implementation criteria. (Ref. JESD12-1B.)

macrocell: A characterized fixed layout and interconnection of primitives that implement an electrical function. (Ref. JESD12-1B.)

NOTE Characterization may be done either by measurement of fabricated devices or by computer simulation or by both. Characterization may include the following aspects: physical dimensions, logic functionality, testability, layout-rule compliance, ac and dc electrical performance, and reliability.

macrocell area: The physical cell area contained within a polygon (often a rectangle) that circumscribes the cell. (See also "unit gate size".) (Ref. JESD12-1B.)

macro function: An interconnection of primitives and/or macrocells that implements an electrical function but has no predetermined physical layout. (Ref. JESD12-1B.)

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1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

module generator: A tool that, when given a high-level description of a desired function and relevant parameters, produces a specified implementation (for example, behavioral, structural, or geometric description, etc.) of the function to be used within an integrated circuit design. (Ref. JESD12-1B.)

NOTE Some functions commonly produced by module generators are RAM, ROM, ALU, and datapath.

net (of a circuit): A unique interconnection of specific circuit elements. (Ref. JESD12-1B.)

NOTE The primary inputs and primary outputs are considered to be circuit elements.

netlist: A list of all nets of a circuit. (Ref. JESD12-1B.)

netlist translation: The conversion of a netlist from one format to another. (Ref. JESD12-1B.)

parameterized macrocell: A macrocell produced by a module generator. (See also “module generator”.) (Ref. JESD12-1B.)

parameterized macro function: A macro function produced by a module generator. (See also “module generator”.) (Ref. JESD12-1B.)

partition: The process by which a design is mapped into multiple components or functional blocks within a device. (Ref. JESD12-1B.)

pin-to-pin delay model: A model for which delays are specified from input pin(s) to output pin(s). (Ref. JESD12-1B.)

primary input: An input driven from outside of the circuit boundary. (Ref. JESD12-1B.)

primary output: An output driving outside the circuit boundary. (Ref. JESD12-1B.)

primitive (building block): A basic building block for a specified level of design hierarchy. (Ref. JESD12-1B.)

process-programmable gate array: A gate array integrated circuit that is programmed as part of the integrated circuit manufacturing process. (Ref. JESD12-1B.)

NOTE Process-programmable gate arrays are characterized by the ability to inventory partially fabricated wafers prior to interconnection.

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1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

programmable logic array (PLA): (1) An integrated circuit consisting of an array of combinational logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions. (Ref. IEC 748-2.)

NOTE The PLA is typically a large set of AND gates driving several OR gates.

(2) A cell that emulates a programmable logic array that has been programmed in a custom integrated circuit.

programmable logic sequencer (PLS): (1) An integrated circuit consisting of an array of combinational and sequential logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions.

(2) A cell that emulates a programmable logic sequencer that has been programmed in a custom integrated circuit.

register-transfer-level (RTL) description: A hybrid between a behavioral description and a structural description at the level of clocked registers. (Ref. JESD12-1B.)

scan insertion: The conversion of bistable elements into scan cells. (Ref. JESD12-1B.)

schematic capture: Use of a computer system to enter a graphical representation of the functional blocks and the interconnections of a circuit. (Ref. JESD12-1B.)

silicon compiler: A design automation system that, when given a high-level description (behavioral, register transfer level, etc.) of desired functionality, will generate sufficient information for manufacture and verification of an integrated circuit design. (Ref. JESD12-1B.)

soft macro: Synonym for “macro function”.

standard cell: A macrocell used in the context of cell-based integrated circuits. (Ref. JESD12-1B.)

structural description: A definition of a function in terms of an interconnection of primitives. (Ref. JESD12-1B.)

switch-level description: A structural description using switches as primitives. (Ref. JESD12-1B.)

symbol library: The graphical symbols for a set of macrocells and/or macro functions. (Ref. JESD12-1B.)

test synthesis: Creation and insertion of test circuitry to improve testability of a design.

timing library: The timing models of a set of macrocells and/or macro functions. (Ref. JESD12-1B.)

timing simulation: The process of exercising the functional and timing models of a particular netlist by applying input stimuli to observe the timing responses. (Ref. JESD12-1B.)

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1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

tool: A program that performs a function within a design automation system. (Ref. JESD12-1B.)

top-down design: The process of designing a circuit hierarchically starting at the highest level followed by detailed design at a lower level. (Ref. JESD12-1B.)

uncommitted logic array: Synonym for “gate array integrated circuit”.

unit gate size (of a gate array): A physical space occupied by a single gate equivalent, including any area allocated to power connections, signal connections, and isolation requirements. (Ref. JESD12-1B.)

unit load: A measure of load (usually capacitance) equal to that presented by a specified input of a specified primitive. (Ref. JESD12-1B.)

used gate (in a gate array): A single gate equivalent that has been interconnected and is employed in the functioning of the circuit. (Ref. JESD12-1B.)

usable gates (in a gate array): The typical number of gate equivalents that can be used in a given gate array size. (Ref. JESD12-1B.)

wire length: The total amount of interconnect of a net (specified in units of either length or capacitance). (Ref. JESD12-1B.)

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