

JEDEC SPECIFICATION

Transistor, Gallium Arsenide Power Fet, Generic Specification

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ELECTRONIC INDUSTRIES ASSOCIATION

ENGINEERING DEPARTMENT



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TRANSISTOR, GALLIUM
ARSENIDE POWER FET, GENERIC SPECIFICATION

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TRANSISTOR, GALLIUM
ARSENIDE POWER FET, GENERIC SPECIFICATION
(From JEDEC JCB-89-32 Council Ballot, formulated under
the cognizance of JC-50, Committee on Gallium Arsenide)

1. SCOPE

1.1 General

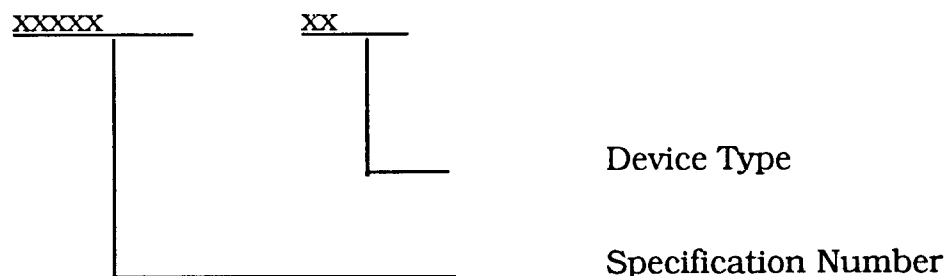
This specification establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also known as MESFETs) designed for use in high-reliability space applications such as spacecraft communications transmitters. The specification identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance inspection tests pertinent to power GaAs FETs. For the purposes of this specification, a power GaAs FET is defined as one used as an RF amplifier which is operated in compression. The specification is intended to be applicable to packaged and chip-carrier parts; consequently portions of the specification may not be applicable to unpackaged and unmounted chips.

The intent of this specification is to serve as a guideline for transistor manufacturers and users (purchasers) to use in the development of their own specifications for power GaAs FETs for applications requiring high reliability. The specific applications and device designs will define the values for parameters left undefined in this specification.

It is expected that the manufacturer, prior to acceptance of this specification, will have generated reliability data which indicate to the purchaser that they can fulfill the reliability goals of the specification and can identify the most probable failure mechanism.

1.2 Part Number

The complete part number shall be as follows:



1.2.1 Device Type and Package or Chip-Carrier Outline

The device type and package or chip-carrier outline shall be as follows:

Device Type Package or Chip-Carrier Outline

xx

Figure 1

1.3 Absolute Maximum Ratings (see MIL-S-19500, Appendix A, Paragraph 20.1)

The device shall have the maximum rating at $T_A = 25 \pm 3^\circ\text{C}$ unless otherwise specified.

PARAMETER	SYMBOL	VALUE	UNIT
Minimum breakdown voltage drain to source	$V_{(BR)DS0}$		volts
Minimum breakdown voltage gate to source	$V_{(BR)GS0}$		volts
Minimum breakdown voltage gate to drain	$V_{(BR)GD0}$		volts
Maximum continuous drain current	I_{DM}		amps
Maximum power dissipation at 25°C base ^{1,2}	P_T		watts
Maximum thermal resistance (channel to base) ¹	R_{CC}		$^\circ\text{C}/\text{W}$
Storage temperature range	T_{STG}	-65 to 175	$^\circ\text{C}$
Operating temperature range (channel) ³	T_{OP}	-65 to 175	$^\circ\text{C}$
Maximum RF input power	P_{INMAX}		watts or dBm
Maximum gate current range under RF operation	I_{GMAX}, I_{GMIN}		mA

Notes:

1. The word "base" called out in this specification refers to the mounting fixture's surface. This rating is for a channel temperature of 175°C .
2. The total power dissipation shall be derated linearly from P_T watts at 25°C base temperature to 0 watts at 175°C base temperature.
3. The operating channel temperature will directly affect the MESFET MTTF (Mean Time To Failure). For maximum life, it is recommended that the channel temperature be maintained at the lowest possible level.

1.4 Handling Precautions

This device may be sensitive to electrostatic discharge (ESD), and proper care (see MIL-STD-1547) in packaging, handling, testing, and use must be exercised to prevent either immediate failure or degradation and reduced life of the device due to this cause. The leads (e.g., gate or drain) of packaged devices can be damaged by bending stress. Therefore, exercise care in handling and test; do not handle packaged devices by their leads. Chip-carrier devices are extremely vulnerable to contamination and physical damage to the chip metallization and

wire or ribbon bonds. Consequently, do not handle the devices without proper tools or open their containers outside an appropriate clean area.

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. In case of conflict the requirements of this specification shall take precedence. Date of issue shall be the latest date prior to start of contract unless otherwise specified.

MILITARY SPECIFICATIONS

MIL-S-19491 Semiconductor, Devices, Packaging of

MIL-S-19500 Semiconductor Devices, General Specification for

MIL-G-45204 Gold Plating, Electro Deposited

MIL-M-38510 Microcircuits, General Specification for

MILITARY STANDARDS

MIL-STD-129 Marking for Shipment and Storage

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-STD-750 Test Methods for Semiconductor Devices

MIL-STD-883 Test Methods for Microelectronic Devices

MIL-STD-1276 Leads; Weldable for Electronic Component Parts

MIL-STD-1285 Marking of Electrical and Electronic Parts

MIL-STD-1547 Parts, Materials, and Processes for Space and Launch Vehicles

MIL-STD-45662 Calibration Systems Requirements

APPENDICES

1

Test Procedure for RF Power, Gain, Efficiency and Impedance

3. REQUIREMENTS

3.1 General

Devices supplied to this specification shall meet the requirements as specified herein. Depending on the application the device may be mounted in hermetic packages or unsealed chip-carriers.

3.2 Design, Construction, and Physical Dimensions

The design, construction, and physical dimensions shall be as specified herein.

3.2.1 Package (Chip Carrier) Outline

The package (chip carrier) outline shall be as specified in Figure 1.

3.2.2 Hermetic Package

The package design must have been qualified as hermetic for space applications, e.g., metal-ceramic construction is qualified.

3.2.3 Chip Carriers

Chip carriers may be required for mounting higher frequency devices. Such carriers are intended for use only in hermetically sealed circuits.

3.2.3.1 Chip Carrier Construction

Chip carriers may be constructed of a combination of metallized ceramic and metal to provide a mounting surface for the device and a thermal path for heat dissipation. Metal parts and metallized surfaces shall be gold plated (50 to 100 micro-inches) over nickel plate per MIL-G-45204.

3.3 Materials

3.3.1 Substrate Quality

Gallium arsenide substrates used in the production of the devices shall meet or exceed a minimum specification for quality. The specification on substrate quality prepared by the manufacturer, and any proposed change to the specification, must be approved by the purchaser. The results of tests on the substrates shall be available for examination by the purchaser.

3.3.2 External Metal Surfaces

External metal surfaces shall be plated with 50 to 100 microinches of gold except that ends of leads may be unplated.

3.3.3 Magnetic Materials (application related guideline)

Minimal use of magnetic materials in the construction of the GaAs FET should be considered to prevent magnetic interference with surrounding experiments and circuits.

3.3.4 Matching or Combining Circuit Components

The microstrip substrates and lumped element capacitors or resistors used in the production of matching or combining circuits internal to the device package or chip carrier shall meet or exceed a minimum specification for quality. These

specifications, prepared by the manufacturer, and any proposed change to the specifications must be approved by the purchaser. The results of tests on the subject parts shall be available for examination by the purchaser. Any metallization where die bonding or wire bonding is to be performed on the substrates or lumped element capacitors shall be gold. Any metal wires, ribbons or foils used for inductances or circuit interconnection shall be gold.

3.3.5 Fungus Resistance

External materials used in the construction of the device shall be non-nutrient to fungus.

3.4 Wafer Lot Control

All parts supplied to the requirements of this specification shall be: (1) from a single wafer, or (2) from wafers from the same wafer lot, or (3) from a minimum number of lots (in the order of preference shown). Each wafer lot shall be assigned a unique identifier that provides traceability to all processing steps. If the wafer lot consists of more than one wafer, the wafers within the lot shall be processed in a manner that requires every wafer to be subjected to each and every process step as a group through metal and dielectric deposition, etching, and annealing processes. A lot shall consist of devices originating from a given group of wafers from a common ingot and processed (under equivalent epitaxial or ion implantation conditions) in the same epitaxial growth or ion implantation run.

3.4.1 Wafer Acceptance Inspection

Each wafer designated for devices supplied to this specification shall conform to the requirements of paragraph 4.4.

3.5 Surface Passivation or Protection

The device shall be glassivated to preclude particles undetected by the PIND test from causing an internal short.

3.6 Surface Metallization

The top surface of the die metallization shall be gold with gold wire, ribbon, or foil attachments between the die and package or internal circuitry terminals. This does not preclude the use of aluminum for the gate metallization if the manufacturer can demonstrate the quality, uniformity, and reliability of their barrier metal system per MIL-STD-1547, Section 1400.

3.7 Electrical Characteristics and Ratings

3.7.1 Ratings

The ratings shall be as specified in paragraph 1.3.

3.7.2 Electrical Characteristics

The electrical characteristics shall be as specified in Table I. The RF electrical characteristics are to be measured as indicated in Appendix 1. Unless otherwise noted, the mounting fixture temperature shall be $TBD^{\circ}C \pm 3^{\circ}C$.

3.8 Process Conditioning, Testing and Screening

All devices shall be subjected to the process-conditioning, testing, and screening as specified in Table II.

3.9 Qualification

Devices supplied to this specification shall be a product which has been tested and passed the qualification tests specified herein.

3.10 Lot Quality Conformance

Devices supplied to this specification shall be a product which has passed lot quality conformance as specified in Table V.

3.11 Traceability

A device supplied to this specification shall be traceable to a given wafer, wafer position in a given implantation or epitaxial run and wafer position in a given crystal ingot. The device package or chip carrier shall also be traceable through the various processing steps back to the original package production lot. Device lots shall conform to the requirements of paragraph 4.3.

3.12 Serialization

Each item shall be assigned a serial number that identifies the wafer from which the part was obtained and uniquely identifies the part from all other parts assembled within the lot.

3.13 Marking

Marking shall be in accordance with MIL-STD-1285 and shall consist of the following items (where size or other design considerations will not allow full marking of part, marking for each part shall be in accordance with the following precedence):

- a. Part Number
- b. Serial Number/Lot Code
- c. Date Code
- d. Manufacturer's Name or Symbol

Configuration or polarity of leads must always be indicated either by package marking or variation in lead geometry for the various leads.

3.13.1 Marking Permanence

Marking shall remain legible after brushing when the device is subjected to tests of MIL-STD-202, Method 215.

3.13.2 Date Code

All parts supplied to the requirements of this specification on a single purchase order shall be from a minimum number of lots and date codes. Each assembly lot shall be assigned a lot date code identifying the year and the week of the

year in which assembly of the part was completed (this is usually the assembly seal date for packaged parts).

3.14 Destructive Physical Analysis

A sample of devices shall be evaluated by the purchaser for conformance to the requirements of internal and external materials, construction, process and workmanship as specified herein. Destructive Physical Analysis (DPA) shall be performed by the purchaser in accordance with the purchaser's practices for acceptance. Lots failing the specified criteria shall be rejected. Scanning Electron Microscope (SEM) analysis should be part of DPA.

3.14.1 Sample Size

The sample size for the DPA shall consist of a minimum of two devices from each wafer randomly selected from the quantity received from a given purchase order. Two samples selected before burn-in and three afterward are recommended.

3.15 Radiation Survivability

The manufacturer shall supply the purchaser with a sample of five devices from each wafer lot for survivability radiation test. Radiation survivability testing imposes no lot jeopardy liability on the manufacturer.

The samples shall be immediately pulled from a lot after completion of the screening sequence specified in Table II.

3.16 Workmanship

Devices shall be manufactured and processed in a careful and workmanlike manner (in accordance with good design and sound engineering practice) with the requirements of this specification and the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of a product assurance program in accordance with paragraph 4.0.

3.17 Abbreviations, Symbols and Definitions

The abbreviations, symbols and definitions used herein shall be as defined in MIL-S-19500 or as they appear.

3.18 Record-Keeping and Data

The manufacturer shall maintain complete records and data, accessible to the purchaser, for the construction and test history of each device manufactured under a given purchase order for a period of 10 years after shipment. This requirement includes substrate, die, wafer, lot, package part, matching component and combining component processing and test histories. The information should be complete enough to show device yield at each step and allow construction of identical parts in the future without having to relearn the processing techniques involved. Proprietary information must be available for examination at the vendor's facility by the purchaser.

3.19 Inspectability

Device construction shall be such as to not preclude the processes of measuring, examining, gauging or otherwise comparing the article with the requirements of this specification. This requirement is not intended to exclude the use of air bridge technology.

3.20 Incoming Inspection

The manufacturer shall perform pertinent incoming inspection, in accordance with paragraph 4.11, of each delivery lot of component parts supplied by vendors.

4. QUALITY ASSURANCE PROVISIONS

Manufacturers making devices in accordance with this document shall maintain a Quality Assurance System in accordance with MIL-M-38510, Appendix "A" (or one approved by the purchaser).

4.1 General

Devices supplied to this specification shall meet the quality assurance provisions specified herein. Unless otherwise specified the manufacturer is responsible for the performance of all inspection requirements specified herein.

4.2 Classification of Inspection

The examination and testing of devices shall be classified as follows:

- a. Lot Quality Conformance
- b. Screening
- c. Qualification

4.3 Lot Traceability

Lot size shall be defined per paragraph 3.4 at the process wafer level.

4.4 Lot Quality Conformance

In general, these tests shall be in accordance with the conditions specified in MIL-STD-883, METHOD 5007 entitled "Wafer Lot Acceptance," except that gold backing thickness may be up to 200,000 Å and wafer thickness may be as small as 0.001 inch. In particular, each wafer lot designated for supplying devices to this specification shall meet the requirements of Table V on a sampling basis. If one or more dies from the wafer fail to meet the SEM inspection requirements specified, the wafer shall be deemed a reject. Devices shall not be fabricated from wafers failing to meet the acceptance criteria.

All data results shall be made available for review by the purchaser. In case of conflict in interpretation of the results, the purchaser reserves the right of disapproval when the review of the results indicates unacceptable material.

4.4.1 Wafer SEM Inspection

The sample die from each wafer shall be subjected to scanning electron microscope (SEM) examination in accordance with MIL-STD-883, Method 2018 (or a purchaser-approved manufacturer's SEM inspection document), as described in Table V. A minimum of five dies shall be evaluated from each wafer. The metallization shall be examined with the surface glassivation coating in place and then removed or reduced in thickness to 500 angstroms or less on the die selected for SEM. If one or more dies from the wafer fail to meet the acceptable criteria, the wafer shall be deemed a reject. The SEM inspection die shall be kept in storage under controlled conditions for 5 years by the manufacturer or purchaser at purchaser's option.

4.4.2 Electrical Parameter Evaluation

The sample of devices used in Table V in the electrical tests (Accelerated Life, Device Impedance, and Temperature Sensitivity of RF Performance) shall be selected from those successfully completing the screening indicated in Table II and shall satisfy the limits of Table I. The samples used in the Device Impedance test may be used as part of the deliverable devices or, alternatively, in the Temperature Sensitivity of RF Performance test.

4.5 Quality Conformance Inspection and Screening

In general, Quality Conformance Inspection and Screening shall be in accordance with MIL-M-38510, Para. 4.5, entitled "Quality Conformation Inspection." In particular, screening shall be performed on all devices supplied to this specification in accordance with Table II.

4.5.1 Screening Reject Criteria

4.5.1.1 Device Failure

Any device which fails screening at any point shall be deemed a reject and shall not be delivered under this specification.

4.5.1.2 Screening Lot Failure (For the purposes of this paragraph, a screening lot is defined as a group of devices undergoing burn-in simultaneously in the same burn-in facility.)

If more than 20% of the devices subjected to burn-in fail to remain within the electrical drift limits of Table III, the screening lot shall be rejected. If less than 10% fail, the lot is accepted. If more than 10% but less than 20% fail, a second burn-in may be applied. If more than 5% fail in the second burn-in, the lot is rejected. The purchaser shall be notified within 2 working days of the lot rejection, and disposition of the lot shall not occur without the concurrence of the purchaser.

4.5.2 Data Requirements

The manufacturer shall supply one reproducible copy of the variables data from pre and post burn-in electrical measurements, including deltas. A summary of the electrical requirements in Table II identifying the serial number, test, number of parts tested, number accepted and number rejected shall be provided.