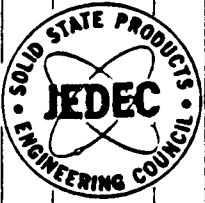


FEBRUARY 1986



JEDEC STANDARD No. 12-2

STANDARD

FOR

CELL-BASED INTEGRATED CIRCUIT

BENCHMARK SET

JEDEC

Solid State Products Engineering Council



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STANDARD
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TABLE OF CONTENTS

<u>Paragraph</u>		<u>Page</u>
1.0	PURPOSE	1
2.0	RELATED DOCUMENTS	1
3.0	REASONS FOR REQUIREMENT	1
4.0	VENDOR PRESENTATION OF DATA	2
4.1	Performance Data	2
4.2	Performance Results	2
4.3	Specified Parameters	2
5.0	INDEX OF BENCHMARKS	3
NOTE:	BENCHMARKS #1 - #9 can be found in JEDEC Standard No. 12.	
	BENCHMARKS #10 - #16 are contained in this Standard as listed below:	
BENCHMARK #10	256 x 4 and 256 x 9 R/W Random Access Memory similar to 2101	5
BENCHMARK #11	16 X 4 ROM Patch	6
BENCHMARK #12	2K x 4 and 2K x 9 Read Only Memory	7
BENCHMARK #13	Small and Large PLA's	8
BENCHMARK #14	2:1 Analog Multiplexer	9
BENCHMARK #15	Comparator	22
BENCHMARK #16	8 Bit D/A	28

STANDARD
FOR
CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET

(From JEDEC Council Ballot JCB-85-14, formulated under the cognizance of JC-44.2 Committee on Cell-Based Integrated Circuits.)

1.0 PURPOSE

The purpose of these benchmarks is to provide a common set of high-level functions to serve as vehicles for comparing the performance of cell-based IC's implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of vendors' ability to implement a desired complex function at a known level of performance.

2.0 RELATED DOCUMENTS

In addition to this Standard, the following related JEDEC Standards are available:

JEDEC Standard No. 12
Semicustom Integrated Circuits, (May 1985);

JEDEC Standard No. 12-1
Semicustom Integrated Circuits - Terms and Definitions for Gate Arrays and Cell-Based Integrated Circuits (August 1985).

3.0 REASONS FOR REQUIREMENT

Users of cell-based technology encounter a great deal of difficulty in developing estimates of realistic performance measures for potential designs. This is because most performance data currently specified by industry vendors exists at SSI level (viz NAND, NOR, INVERTER). Users need to know in advance of beginning a design the estimated performance of some commonly used MSI functions such as counters, decoders, octal flip-flops, small ALU's, etc. From this data they are able to construct an estimate of performance of critical portions of their designs and check the feasibility of building that circuit using a specified cell-based technology.

4.0 VENDOR PRESENTATION OF DATA

While it is by no means mandatory that cell-based IC vendors provide this data, a JEDEC standard benchmark inherently provides more consistency and structure in the marketplace, which is advantageous to both vendors and users.

4.1 Performance Data

Vendors may choose to provide their customers with such performance data based purely on simulated designs or alternatively choose to implement macro element portions of test chips which they may then characterize and/or make available to customers for evaluation.

4.2 Performance Results

In all cases these performance results and parameters must specify the conditions and methods under which they are derived. Wherever multiple ac paths are possible from an input to an output, the vendor will specify the characteristics of the slowest path.

4.3 Specified Parameters

Parameters specified should include, but are not limited to:

- (1) Two-input gate equivalents or, where appropriate, component count used;
- (2) area, width, height;
- (3) worst-case dynamic power at vendor-specified frequency(ies) and fanout;
- (4) dc static power with inputs at levels specified by vendor and at vendor-specified power supply voltage and temperature;
- (5) worst-case ac performance parameters for each benchmark cell, under vendor-specified power supply voltage, temperature and driving pulse edge rates;
- (6) method of implementation (hard macro or soft macro);

4.3 Specified Parameters (continued)

- (7) number of feedthroughs included in cell;
- (8) separate derating factors for voltage, temperature and fanout;
- (9) degree of characterization (simulation [specify whether with or without layout parasitics included], fabricated and measured silicon).

NOTE 1: All benchmark cells must be implementable in a single IC process feasible for commercial introduction.

CAUTION: For an actual chip design, total chip area is a function of both cell area and routing area. Routing area is dependent on chip architecture, layout and specific application software.

5.0 INDEX OF BENCHMARKS

- #1 4 Bit ALU, similar to 74S381
See Benchmark No. 1, JEDEC Standard No. 12.
- #2 16 Bit ALU, similar to 74S381
See Benchmark No. 2, JEDEC Standard No. 12.
- #3 4 Bit Rotator
See Benchmark No. 3, JEDEC Standard No. 12.
- #4 16 Bit Rotator
See Benchmark No. 4, JEDEC Standard No. 12.
- #5 8 Bit Register, similar to 74S374
See Benchmark No. 5, JEDEC Standard No. 12.
- #6 8 Bit Up/Down Counter
See Benchmark No. 6, JEDEC Standard No. 12.
- #7 3 to 8 Decoder, similar to 74S138
See Benchmark No. 7, JEDEC Standard No. 12.
- #8 16x4 RAM, similar to 74S189
See Benchmark No. 8, JEDEC Standard No. 12.
- #9 9 Bit Parity Generator, similar to 74S280
See Benchmark No. 9, JEDEC Standard No. 12.

5.0 INDEX OF BENCHMARKS (continued)

This Standard, No. 12-2, contains the below listed Benchmarks:

#10 256 x 4 and 256 x 9 RAM, similar to 2101

#11 16 x 4 ROM Patch

#12 2K x 4 and 2K x 9 ROM

#13 Small and Large PLA's

#14 2:1 Analog Multiplexer

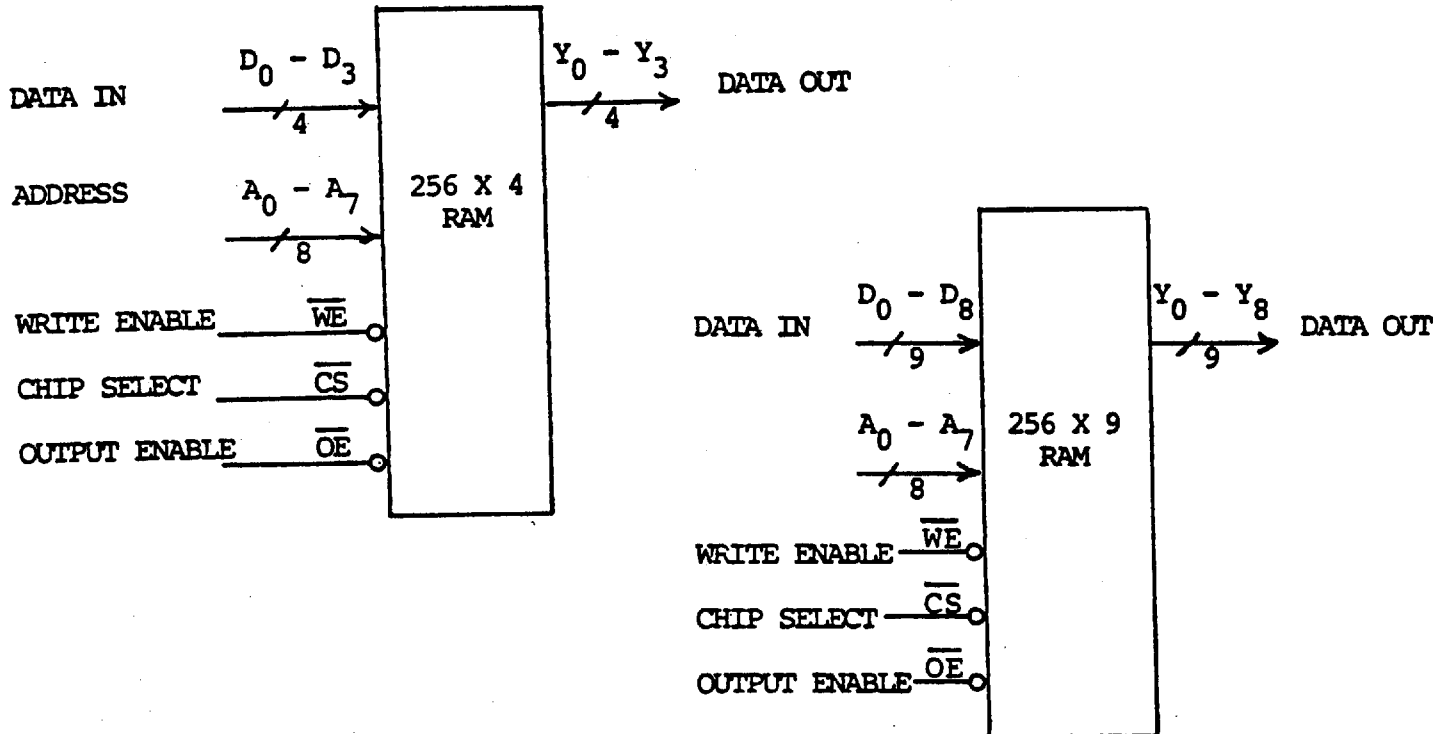
#15 Analog Comparator

#16 8 Bit Digital/Analog Converter.

BENCHMARK #10

256 x 4 and 256 x 9 R/W RANDOM ACCESS MEMORY
SIMILAR TO 2101

Tests the cost/efficiency of nibble and byte (plus parity) wide memory functions.



The minimum performance parameters to be specified are:

Max Delay	Any A to Any Y
Max Delay	$\overline{CS}$ to Any Y
Max Delay	$\overline{OE}$ to Any Y
Minimum Setup	$\overline{CS}$ before $\overline{WE}$ Low
Minimum Setup	A before $\overline{WE}$ Low
Minimum Hold	A after $\overline{WE}$ Rising Edge
Minimum Setup	D before $\overline{WE}$ Rising Edge
Minimum Hold	D after $\overline{WE}$ Rising Edge

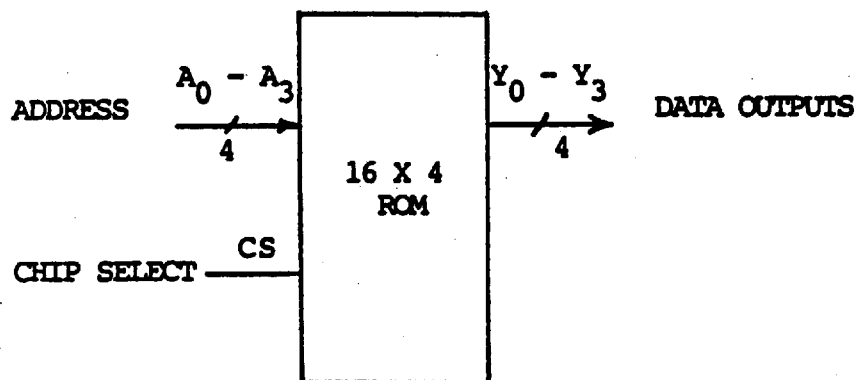
Minimum $\overline{WE}$ Pulse Width

Total cells used/area/derating factor for layout.

BENCHMARK #11

16 x 4 ROM PATCH

Tests cost/efficiency of a small ROM that would be used for logic patch purposes and would be programmed at the interconnect level.



The minimum performance parameters to be specified are:

Max Delay Any A to Any Y

Max Delay CS to Any Y

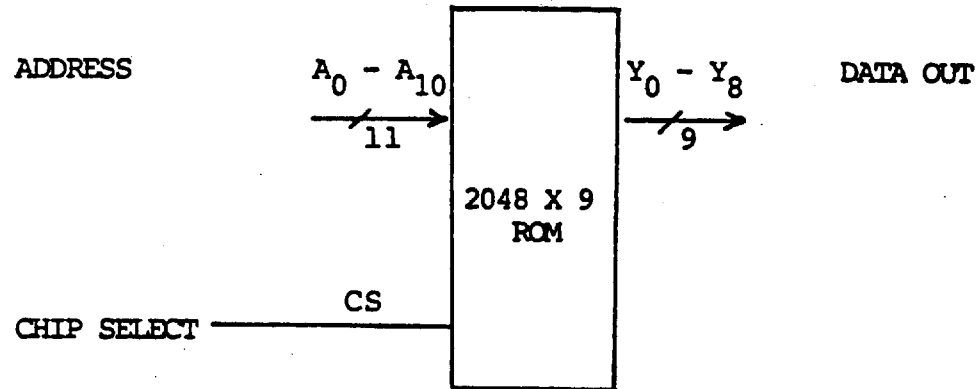
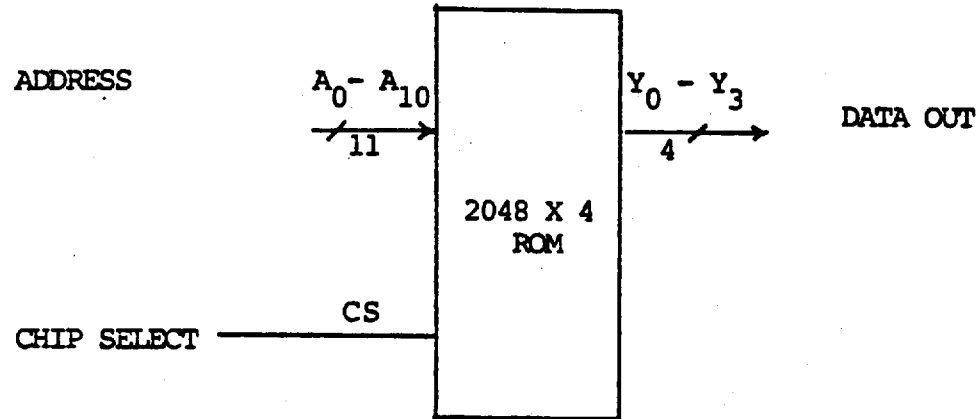
Minimum Hold Any A Change to Any Y Change

Total cells used/area used/derating factor for layout.

BENCHMARK #12

2K x 4 and 2K x 9 READ ONLY MEMORY

Tests the cost/efficiency of program ROM that may be programmed either at the diffusion or interconnect level.



The minimum performance parameters to be specified are:

Max Delay	Any A to Any Y
Max Delay	CS to Any Y
Minimum Hold	Any A Change to Any Y Change

Total cells used/area used/derating factor for layout

Level at which the ROM is programmed (i.e. diffusion or interconnect).

BENCHMARK #13
SMALL AND LARGE PLA's

REQUIREMENTS

<u>Inputs</u>	<u>Product Terms</u>	<u>Outputs</u>	<u>Programming Level</u>
16	48	8	Metal
32	256	20	Early (e.g. diffusion)

No Folding

Non-Registered

No Partitioning

Specify in addition to standard parameters:

Static or synchronous operation;

Speed on slowest path.