

JEDEC STANDARD

STANDARD FOR DESCRIPTION OF
54/74ACXXXXX AND 54/74ACTXXXXX
ADVANCED HIGH-SPEED CMOS
DEVICES

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ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT



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STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX
ADVANCED HIGH-SPEED CMOS DEVICES

(From JEDEC Council Ballot JCB-89-37, formulated under the cognizance of JC-40.2 Committee on CMOS Logic Devices.)

SECTION 1

1. 54/74ACXXXXX STANDARD

1.1 Purpose and Scope

1.2 Purpose

The purpose of this standard is to develop a standard of "54/74ACXXXXX" series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1.3 Scope

This standard covers standard specifications for description of the "54/74ACXXXXX" series advanced high-speed CMOS devices.

2. DEFINITIONS

54ACXXXXX

Indicates that the devices are specified over the temperature range from -55°C to 125°C .

74ACXXXXX

Indicates that the devices are specified over the temperature range from -40°C to 85°C .

54/74ACXXXXX Series

Includes devices whose input logic levels are defined herein for V_{IH} and V_{IL} . Input switching thresholds are nominally one half the supply voltage. For driving CMOS input logic levels, incident wave-line-driving is specified for 50 ohm (74ACXXXXX) and 75 ohm (54ACXXXXX) lines.

Low Voltage Operation

In accordance with the latest revision of JEDEC Standard No. 8 "Standard for Reduced Operating Voltages and Interface Levels for Integrated Circuits" (March 1984).

3. STANDARD SPECIFICATIONS

All voltages listed are referenced to ground except where noted.

3.1 Absolute Maximum Continuous Ratings (Notes 1 and 2):

Supply Voltage, V_{CC}		-0.5 V to 6 V
DC Input Diode Current, I_{IK}	($V_I < 0$)	-20 mA
	($V_I > 0$)	20 mA
or		
DC Input Voltage, V_I		-0.5 V to $V_{CC} + 0.5$ V
DC Output Diode Current, I_{OK}	($V_O < 0$)	-50 mA
	($V_O > 0$)	50 mA
or		
DC Output Voltage, V_O		-0.5 V to $V_{CC} + 0.5$ V
DC Output Source or Sink Current per output pin, I_O		± 50 mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (for up to 4 outputs per device, Note 3)		± 100 mA
Storage Temperature, T_{stg}		-65°C to 150°C

NOTE 1: Absolute Maximum Continuous Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

NOTE 2: Under transient conditions, these ratings may be exceeded as defined elsewhere in this specification.

NOTE 3: For devices with more than four outputs, the maximum rating equals the number of outputs multiplied by ± 25 mA.

Table 1-1
Recommended Operating Conditions

Symbol	Parameter	54ACX000X			74ACX000X			Unit
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (Notes 1 & 2)	3	5	5.5	3	5	5.5	V
V_I	Input voltage	0		V_{CC}			V_{CC}	V
V_O	Output voltage	0		V_{CC}			V_{CC}	V
$\Delta V/\Delta t$	Input transition rise or fall rate (Except for Schmitt inputs) (Note 3)	0		8	0		8	ns/V
T_A	Operating free-air temperature range	-65		125	-40		85	°C

NOTE 1: Unless otherwise specified.

NOTE 2: Parameters are specified from 3 V to 5.5 V. Data retention from 2 to 3 volts is for compatibility with battery backup systems.

NOTE 3: For V_I between $0.3V_{CC}$ and $0.7V_{CC}$.

Table 1-2
DC Specifications
54/74AC Family Specifications

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C		74ACXXXX		54ACXXXX		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{HI}	High-level input voltage		3.0	2.10		2.10		2.10		V
			4.5	3.15		3.15		3.15		V
			5.5	3.85		3.85		3.85		V
V _{LI}	Low-level input voltage		3.0		0.90		0.90		0.90	V
			4.5		1.35		1.35		1.35	V
			5.5		1.65		1.65		1.65	V
V _{OHI}	High-level output voltage (Notes 1 & 2)	V _I = V _{HI} or V _{LI} , I _{OH} = -50 µA	3.0	2.90		2.90		2.90		V
			4.5	4.40		4.40		4.40		V
		V _I = V _{HI} or V _{LI} , I _{OH} = -4 mA	3.0	2.66		2.46		2.40		V
		V _I = V _{HI} or V _{LI} , I _{OH} = -24 mA	4.5	3.86		3.76		3.70		V
		V _I = V _{HI} or V _{LI} , I _{OH} = -50 mA	5.5					3.85		V
		V _I = V _{HI} or V _{LI} , I _{OH} = -75 mA	5.5			3.85				V
V _{OLI}	Low-level output voltage (Note 2)	V _I = V _{HI} or V _{LI} , I _{OL} = 50 µA	3.0		0.10		0.10		0.10	V
			4.5		0.10		0.10		0.10	V
		V _I = V _{HI} or V _{LI} , I _{OL} = 12 mA	3.0		0.36		0.44		0.50	V
		V _I = V _{HI} or V _{LI} , I _{OL} = 24 mA	4.5		0.36		0.44		0.50	V
		V _I = V _{HI} or V _{LI} , I _{OL} = 50 mA	5.5						1.65	V
		V _I = V _{HI} or V _{LI} , I _{OL} = 75 mA	5.5				1.65			V
I _I	Input leakage current (Note 3)	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±1.0	µA
I _{OZ}	3-state output off-state current (Note 4)	V _I = V _{HI} or V _{LI} , V _O = V _{CC} or GND	5.5		±0.5		±5.0		±10.0	µA
I _{CC}	Quiescent supply current (Note 5)	V _I = V _{CC} or GND I _O = 0	5.5		4		40		80	µA
			5.5		8		80		160	µA

NOTE 1: Not applicable to open-drain outputs.

NOTE 2: Test one output at a time for a 10 ms maximum duration. It is recommended that the measurement be made by forcing a current and measuring a voltage to minimize power dissipation. This applies to the V_{CC} = 5.5 V test only and verifies a minimum 50 ohm transmission line drive capability for 74ACXXXX series; 75 ohms for 54ACXXXX series.

NOTE 3: For I/O pins, I_I = I_I + I_{OZ}.

NOTE 4: Also applicable to open-drain outputs.

NOTE 5: See Appendix B.

SECTION 2

1. 54/74ACTXXXXX STANDARD

1.1 Purpose and Scope

1.2 Purpose

The purpose of this standard is to develop a standard of "54/74ACTXXXXX" series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1.3 Scope

This standard covers standard specifications for description of the "54/74ACTXXXXX" series advanced high-speed CMOS devices.

2. DEFINITIONS

54ACTXXXXX

Indicates that the devices are specified of the temperature range from -55°C to 125°C .

74ACTXXXXX

Indicates that the devices are specified over the temperature range from -40°C to 85°C .

54/74ACTXXXXX Series

Includes devices whose input logic levels are identical to TTL input levels. For driving CMOS input logic levels, incident wave-line-driving is specified for 50 ohm, (74ACTXXXXX) and 75 ohm (54ACTXXXXX) lines.

3. STANDARD SPECIFICATIONS

All voltages listed are referenced to ground except where noted.

3.1 Absolute Maximum Continuous Ratings (Notes 1 & 2):

Supply Voltage, V_{CC}		-0.5 V to 6 V
DC Input Diode Current, I_{IK}	($V_I < 0$)	-20 mA
	($V_I > 0$)	20 mA
or		
DC Input Voltage, V_I		-0.5 V to $V_{CC} + 0.5$ V
DC Output Diode Current, I_{OK}	($V_O < 0$)	-50 mA
	($V_O > 0$)	50 mA
or		
DC Output Voltage, V_O		-0.5 V to $V_{CC} + 0.5$ V
DC Output Source or Sink Current per output pin, I_O		± 50 mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (for up to 4 outputs per device, Note 3)		± 100 mA
Storage Temperature, T_{stg}		-65°C to 150°C

NOTE 1: Absolute Maximum Continuous Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

NOTE 2: Under transient conditions, these ratings may be exceeded as defined elsewhere in this specification.

NOTE 3: For devices with more than four outputs, the maximum rating equals the number of outputs multiplied by ± 25 mA.

Table 2-1
Recommended Operating Conditions

Symbol	Parameter	54ACTXXXXX			74ACTXXXXX			Unit
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (Note 1)	4.5	5	5.5	4.5	5	5.5	V
V_I	Input voltage	0		V_{CC}			V_{CC}	V
V_O	Output voltage	0		V_{CC}			V_{CC}	V
$\Delta V/\Delta V$	Input transition rise or fall rate (Except for Schmitt inputs) (Note 2)	0		8	0		8	ns/V
T_A	Operating free-air temperature range	-55		125	-40		85	°C

NOTE 1: Unless otherwise specified.

NOTE 2: For V_I between 0.8 V and 2.0 V.

Table 2-2
DC Specifications
54/74ACT FAMILY SPECIFICATIONS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C		74ACTXXXXX		54ACTXXXXX		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH}	High-level input voltage		4.5	2.0		2.0		2.0		V
			5.5	2.0		2.0		2.0		V
V _{IL}	Low-level input voltage		4.5	0.8		0.8		0.8		V
			5.5	0.8		0.8		0.8		V
V _{OH}	High-level output voltage (Notes 1 & 2)	V _I = V _{IH} or V _{IL} , I _{OH} = -50 µA	4.5	4.40		4.40		4.40		V
		V _I = V _{IH} or V _{IL} , I _{OH} = -24 mA	4.5	3.86		3.76		3.70		V
		V _I = V _{IH} or V _{IL} , I _{OH} = -50 mA	5.5					3.85		V
		V _I = V _{IH} or V _{IL} , I _{OH} = -75 mA	5.5			3.85				V
V _{OL}	Low-level output voltage (Note 2)	V _I = V _{IH} or V _{IL} , I _{OL} = 50 µA	4.5	0.10		0.10		0.10		V
		V _I = V _{IH} or V _{IL} , I _{OL} = 24 mA	4.5	0.36		0.44		0.50		V
		V _I = V _{IH} or V _{IL} , I _{OL} = 50 mA	5.5					1.65		V
		V _I = V _{IH} or V _{IL} , I _{OL} = 75 mA	5.5			1.65				V
I _I	Input leakage current (Note 3)	V _I = V _{CC} or GND	5.5	±0.1		±1.0		±1.0		µA
I _{OZ}	3-state output off-state current (Note 4)	V _I = V _{IH} or V _{IL} , V _O = V _{CC} or GND	5.5	±0.5		±5.0		±10.0		µA
I _{CC}	Quiescent supply current (Note 5)	V _I = V _{CC} or GND I _O = 0	5.5	4		40		80		µA
			5.5	8		80		160		µA
ΔI _{CC}	Supply current, TTL inputs high	One input at 3.4 V, other inputs at V _{CC} or GND	5.5	Note 6		Note 6		Note 6		mA

NOTE 1: Not applicable to open-drain outputs.

NOTE 2: Test one output at a time for a 10 ms maximum duration. It is recommended that the measurement be made by forcing a current and measuring a voltage to minimize power dissipation. This applies to the V_{CC} = 5.5 V test only and verifies a minimum 50 ohm transmission line drive capability for 74ACTXXXXX series; 75 ohms for 54ACTXXXXX series.

NOTE 3: For I/O pins, I_I = I_I + I_{OZ}.

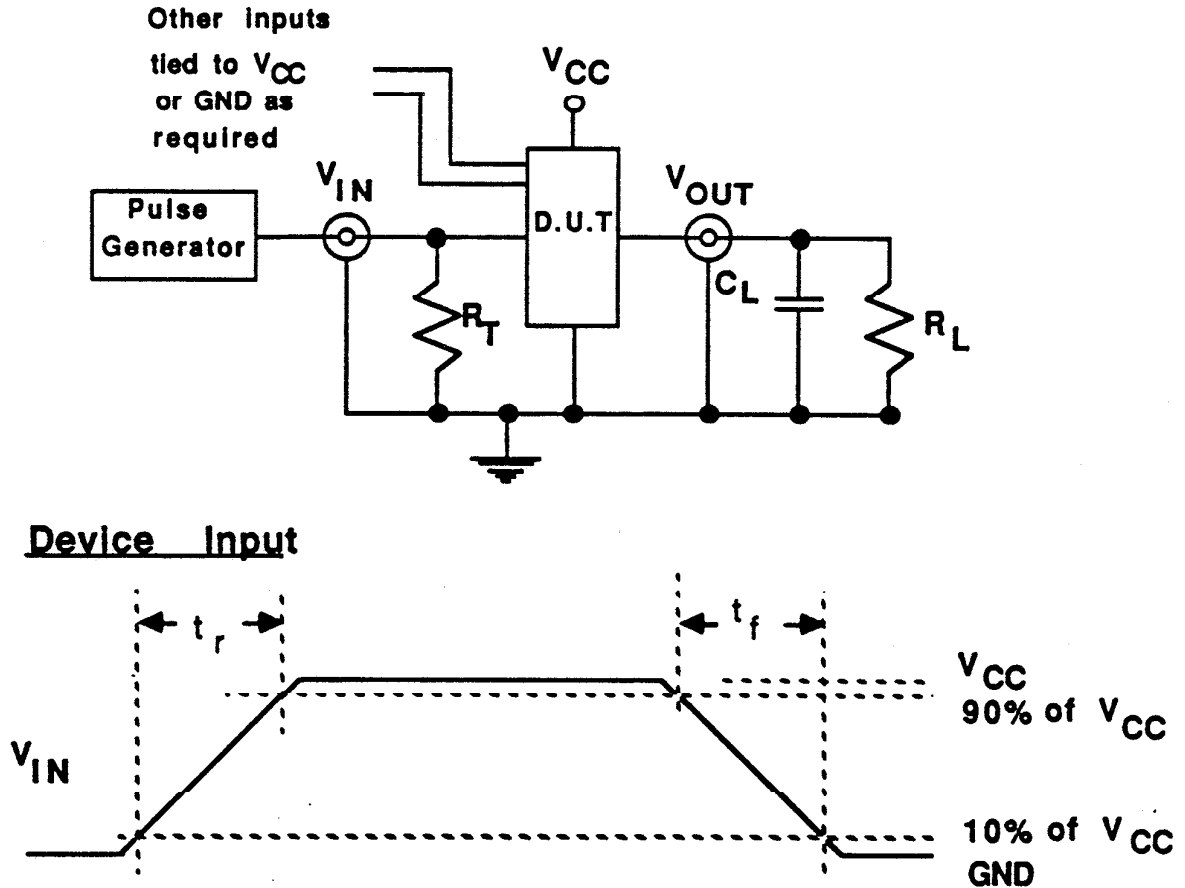
NOTE 4: Also applicable to open-drain outputs.

NOTE 5: See Appendix B.

NOTE 6: Refer to individual manufacturers' datasheets for ΔI_{CC} limits.

SECTION 3

SWITCHING WAVEFORMS FOR 54/74AC



DEFINITIONS:

C_L = 50 pF or equivalent (includes jig and probe capacitance).

R_L = 500 Ω or equivalent.

R_T = Termination should be equal to Z_{OUT} of the pulse generator
(Typically 50 Ω)

V_{IN} = 0V to V_{CC}

INPUT: $t_r = t_f = 3.0\text{ns}$ (10% to 90%) unless otherwise specified

Figure 3-1
Test Circuit

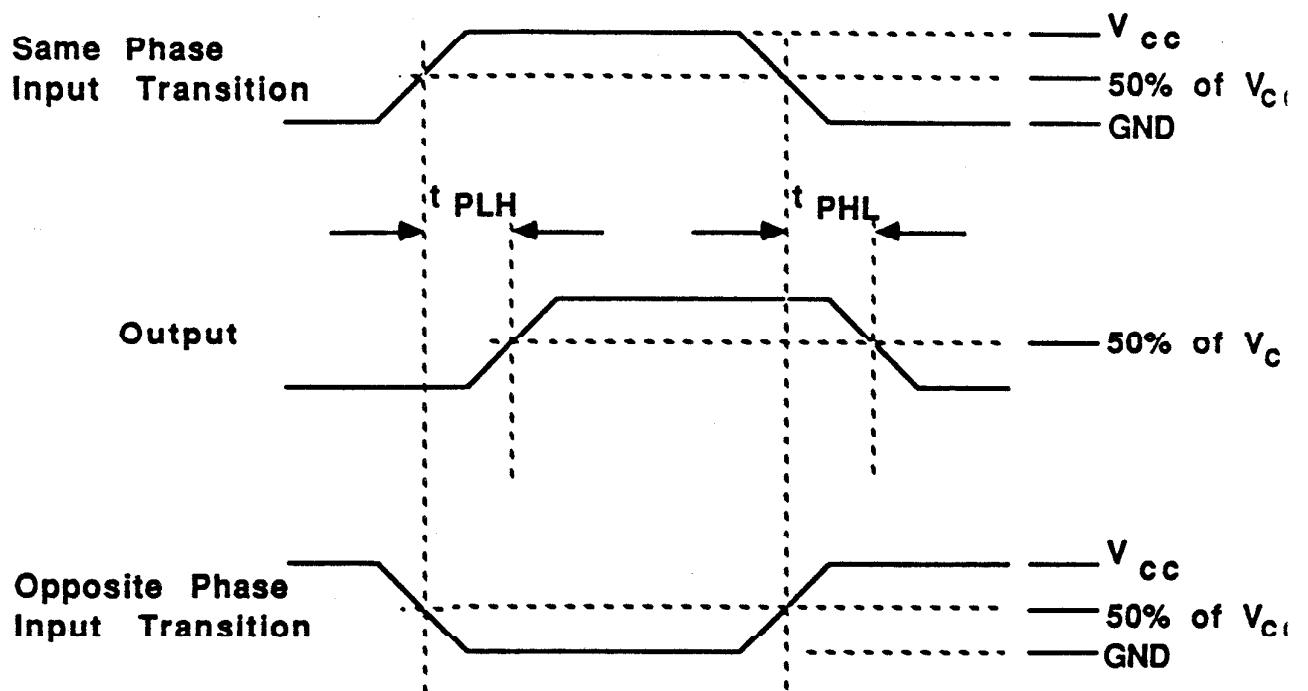
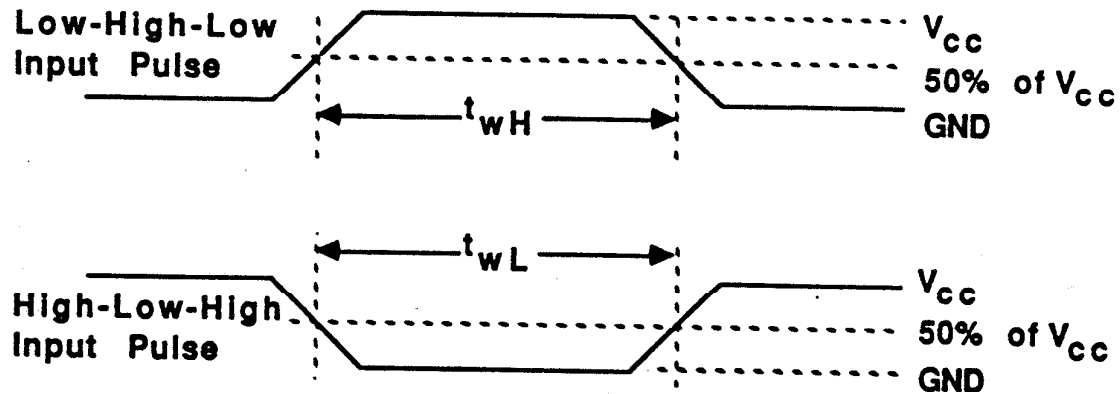


Figure 3-2
Propagation Delay Waveforms



t_r and t_f shall be as fast as required for f_{max} and pulse width being measured.

Outputs must be switching from 10% V_{cc} to 90% V_{cc} in accordance with device truth table. For f_{max} , input duty cycle = 50%.

Figure 3-3
54/74AC Input Pulse Width Waveforms

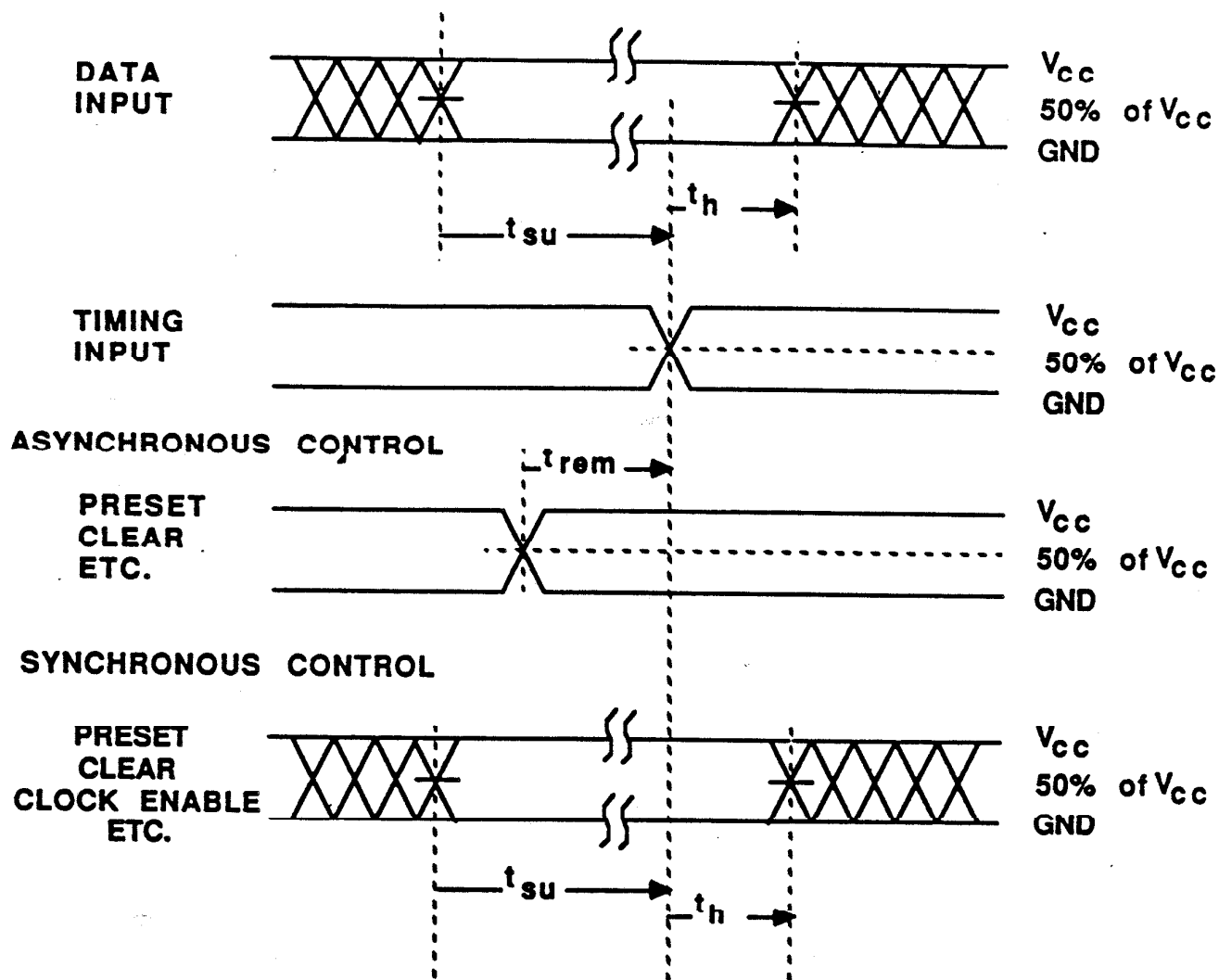
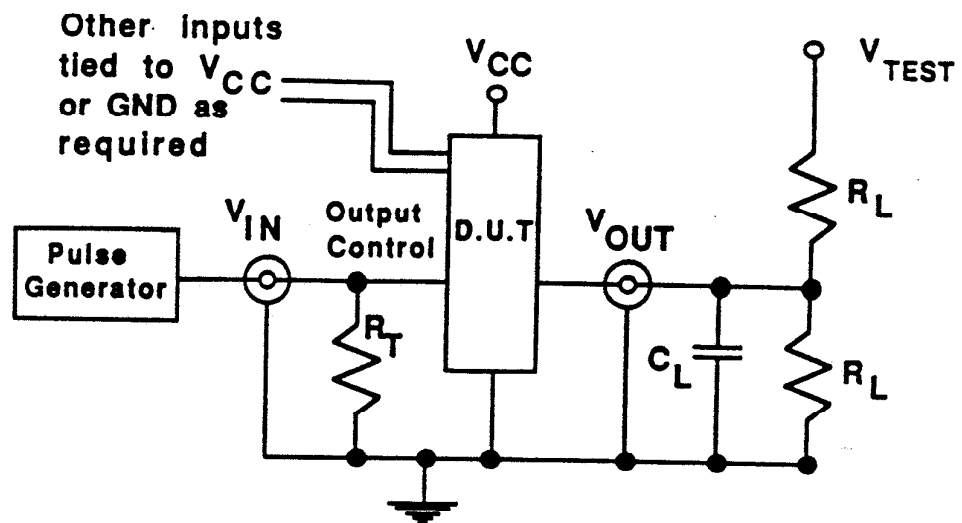


Figure 3-4
54/74AC Set-Up, Hold and Removal Waveforms



PREFERRED METHOD

When measuring t_{PHZ} or t_{PZH} : $V_{TEST} = GND$

When measuring t_{PLZ} or t_{PZL} : $V_{TEST} = \text{Two times } V_{CC}$

ALTERNATE METHOD

When measuring t_{PHZ} or t_{PZH} : $V_{TEST} = OPEN$

When measuring t_{PLZ} or t_{PZL} : $V_{TEST} = \text{Two times } V_{CC}$

DEFINITIONS:

$C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance).

$R_L = 500 \Omega$ or equivalent.

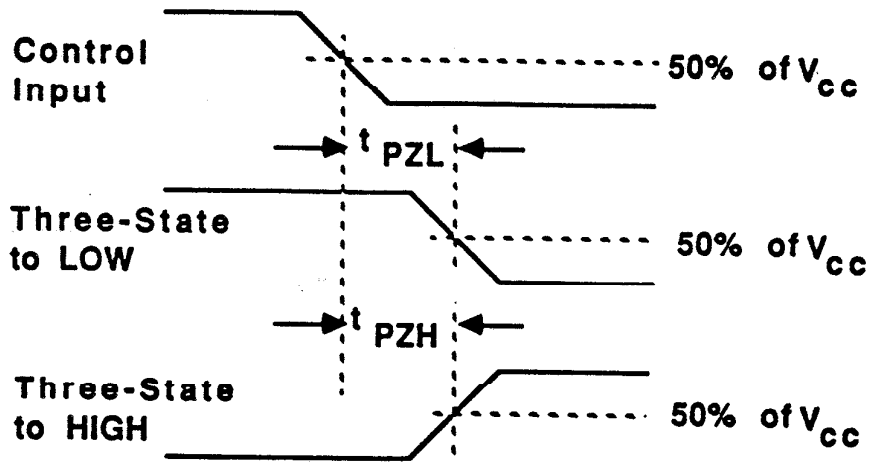
R_T - Termination should be equal to Z_{OUT} of the pulse generator
(Typically 50Ω)

$V_{IN} = 0 \text{ V to } V_{CC}$

INPUT: $t_r = t_f = 2.5 \text{ ns}$ (10% to 90%) unless otherwise specified

Figure 3-5
54/74AC Three-State Propagation Delay Test Circuit

ENABLE TIMES



DISABLE TIMES

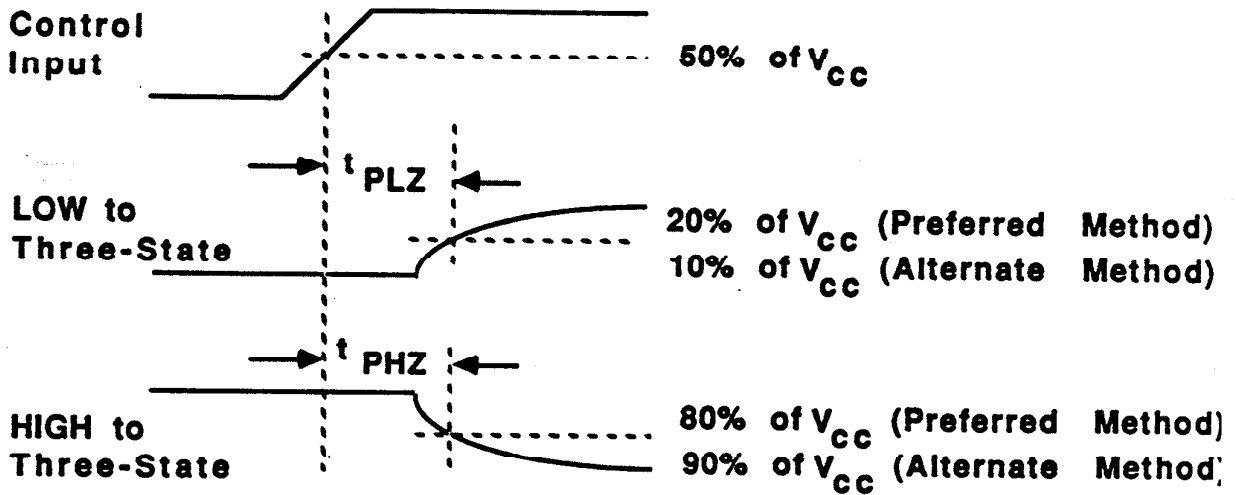
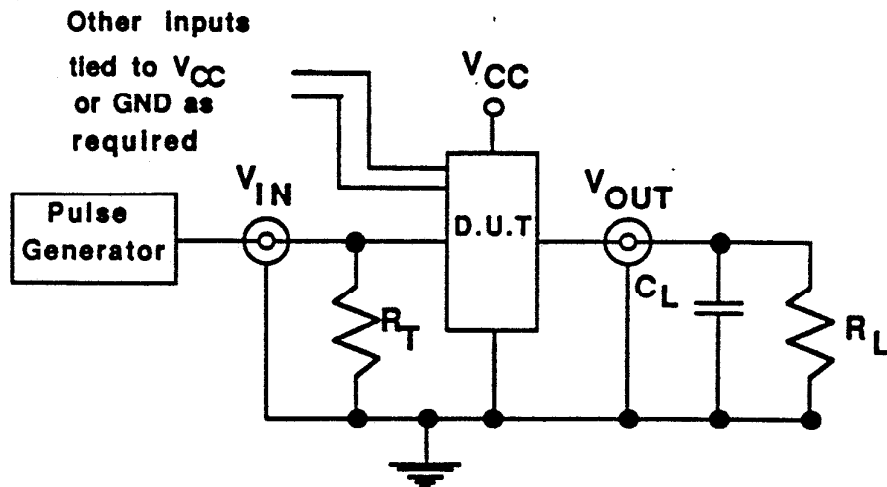


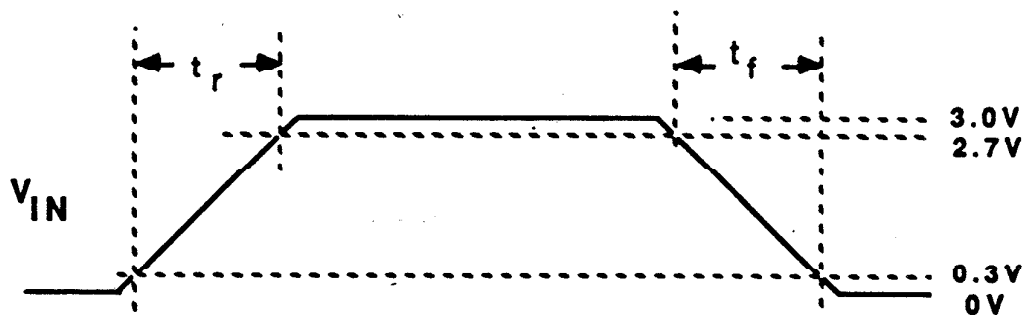
Figure 3-6
54/74AC Three-State Waveforms

SECTION 4

SWITCHING WAVEFORMS FOR 54/74ACT



Device Input



DEFINITIONS:

C_L = 50 pF or equivalent (includes jig and probe capacitance).

R_L = 500 Ω or equivalent.

R_T = Termination should be equal to Z_{OUT} of the pulse generator
(Typically 50 Ω).

V_{IN} = 0V to 3.0V

INPUT: $t_r = t_f = 3.0\text{ns}$ (10% to 90%) unless otherwise specified.

Figure 4-1
Test Circuit

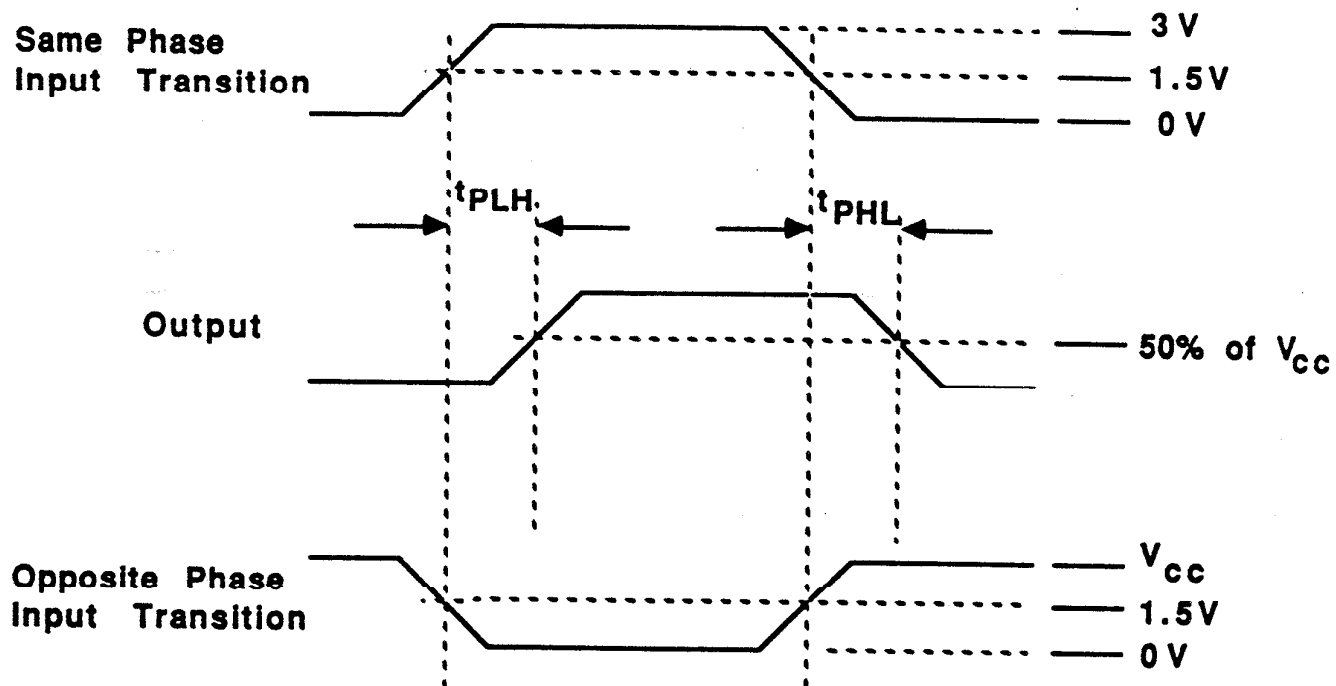
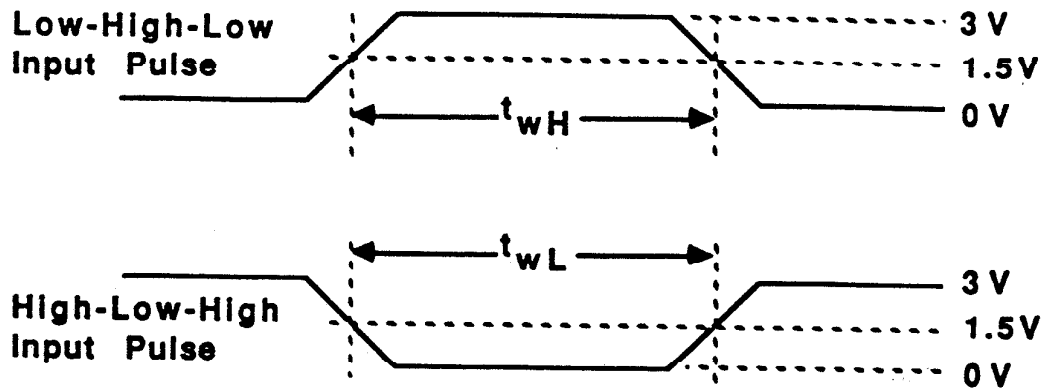


Figure 4-2
54/74ACT Propagation Delay Waveforms



t_r and t_f shall be as fast as required for f_{max} and pulse width being measured.

Outputs must be switching from 10% V_{cc} to 90% V_{cc} in accordance with device truth table. For f_{max} , input duty cycle = 50%.

Figure 4-3
54/74ACT Input Pulse Width Waveforms

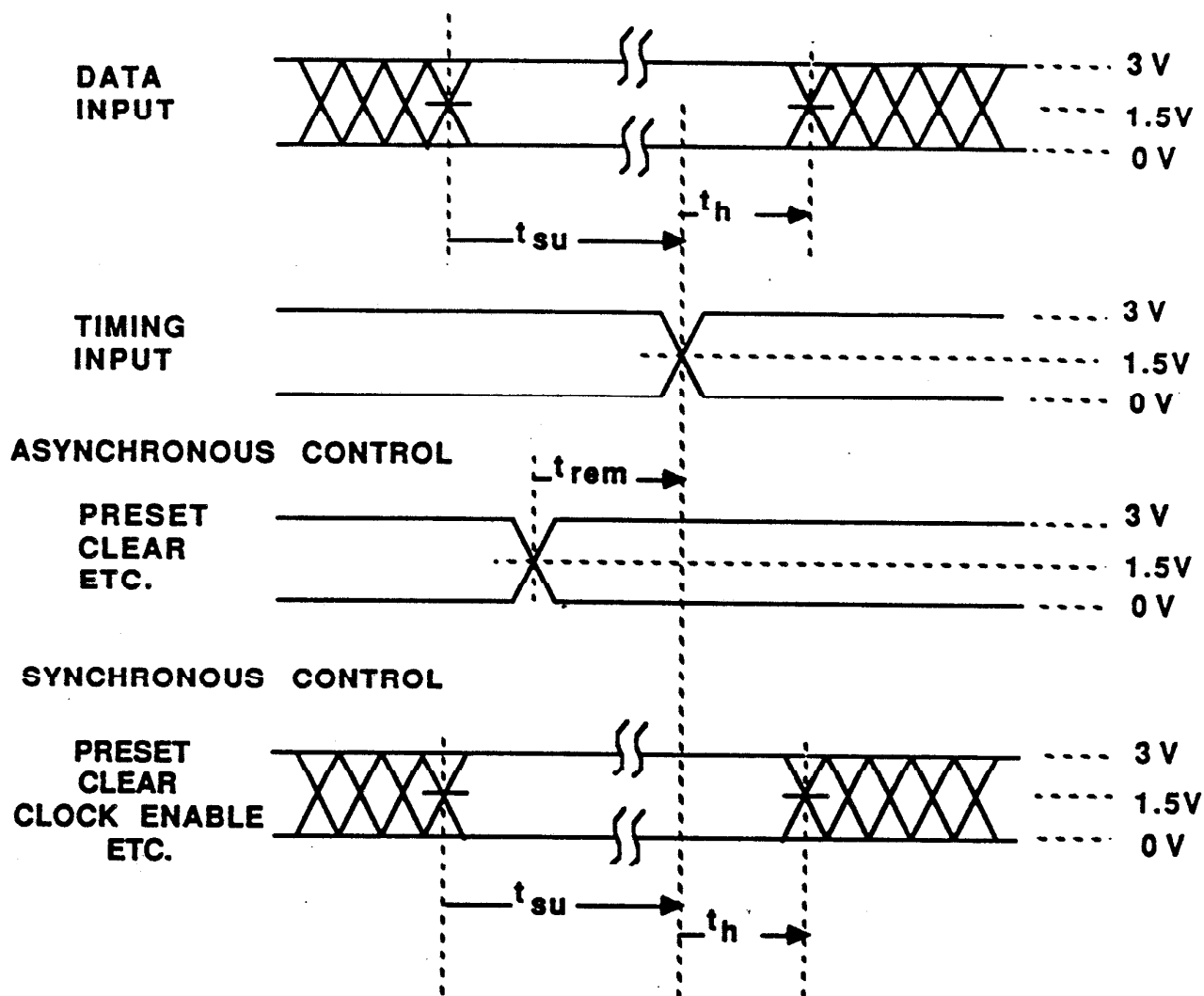
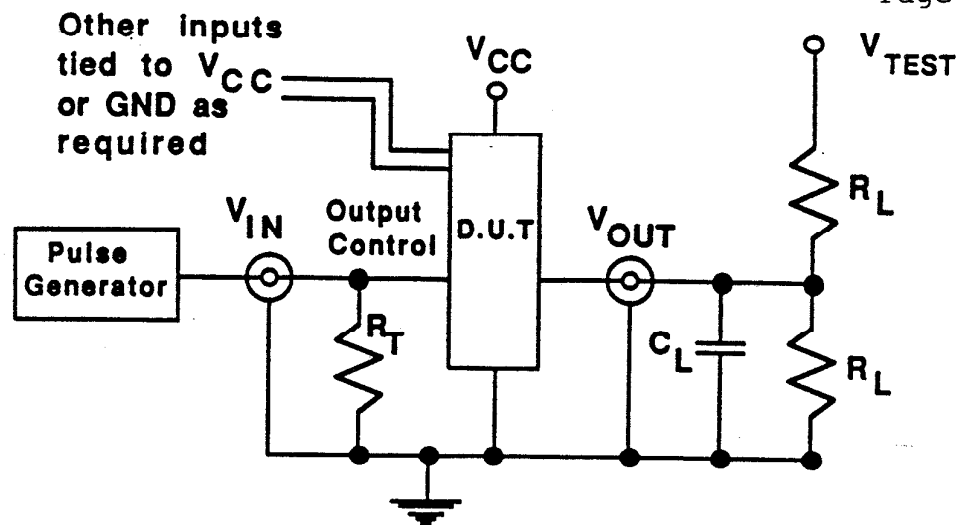


Figure 4-4
54/74ACT Set-Up, Hold and Removal Waveforms



PREFERRED METHOD

When measuring t_{PHZ} or t_{PZH} : $V_{TEST} = GND$

When measuring t_{PLZ} or t_{PZL} : $V_{TEST} = \text{Two times } V_{CC}$

ALTERNATE METHOD

When measuring t_{PHZ} or t_{PZH} : $V_{TEST} = OPEN$

When measuring t_{PLZ} or t_{PZL} : $V_{TEST} = \text{Two times } V_{CC}$

DEFINITIONS:

C_L = 50 pF or equivalent (includes jig and probe capacitance).

R_L = 500 Ω or equivalent.

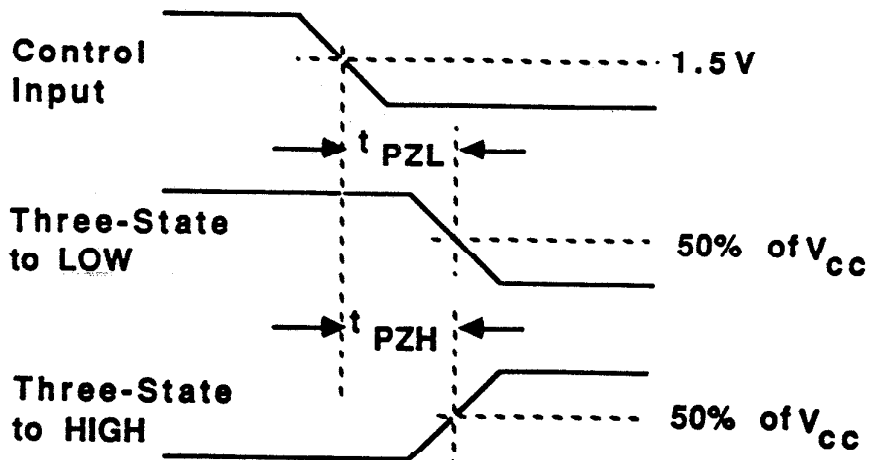
R_T = Termination should be equal to Z_{OUT} of the pulse generator
(Typically 50 Ω)

$V_{IN} = 0 \text{ V to } V_{CC}$

INPUT: $t_r = t_f = 2.5 \text{ ns}$ (10% to 90%) unless otherwise specified

Figure 4-5
54/74ACT Three-State Propagation Delay Test Circuit

ENABLE TIMES



DISABLE TIMES

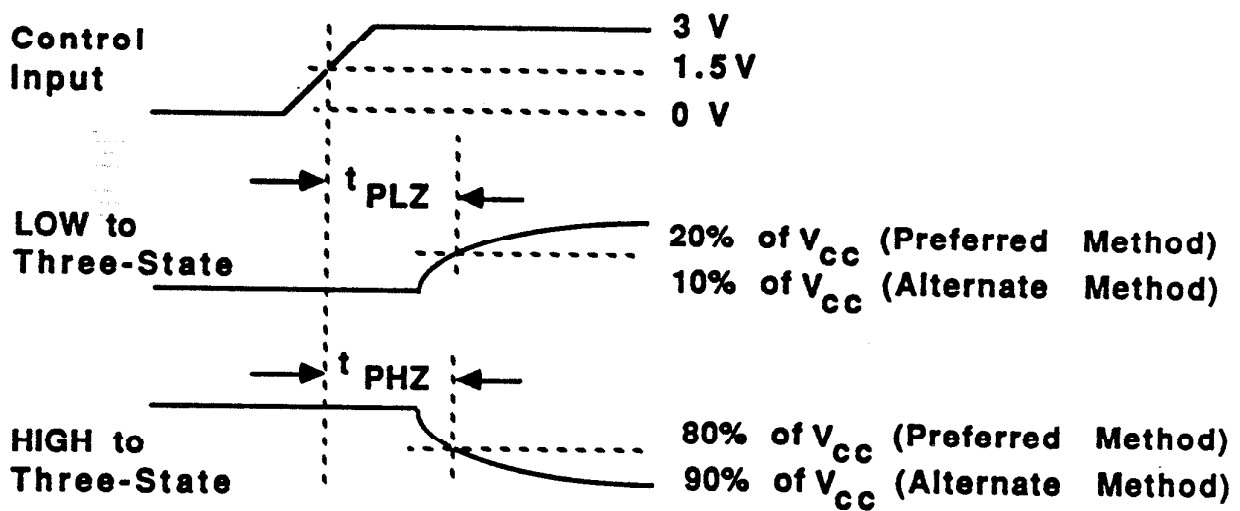


Figure 4-6
54/74ACT Three-State Waveforms

SECTION 5

1. SCOPE

The scope of this section shall be to establish quiescent I_{CC} current categories for the device types listed herein.

1.1 I_{CC}

The I_{CC} is the maximum at 25°C, with all outputs unloaded, all inputs at V_{CC} or ground. To derive the 85°C number, multiply by 10. To derive the 125°C number, multiply by 20.

ICC Type Categories for AC and ACT Devices

$I_{CC} = 4 \mu A$	$I_{CC} = 8 \mu A$					Special I_{CC}
00	125	373	823	11191	11818	520 11520
02	138	374	824	11191	11819	
04	139	377	825	11193	11821	
05	151	379	826	11194	11822	
08	153	393	827	11238	11823	
10	154	465	828	11239	11824	
11	157	466	841	11240	11825	
14@	158	467	842	11241	11826	
20	160	468	843	11244	11827	
30	161	521	844	11245	11828	
32	162	533	845	11251	11833	
74	163	534	846	11253	11834	
86	164	540	861	11257	11841	
107	165	541	862	11258	11842	
109	166	544	863	11269	11843	
112	168	564	864	11280	11844	
11000	169	564	876	11286	11845	
11002	174	569	878	11299	11846	
11004	175	573	879	11323	11853	
11008	191	574	880	11352	11854	
11010	193	576	4020	11353	11861	
11011	238	580	4060	11373	11862	
11013@	240	620	7060	11374	11863	
11014@	241	623	7623	11378	11864	
11020	244	640	11138	11379	11873	
11021	245	643	11139	11521	11874	
11027	251	645	11151	11533	11881	
11030	253	646	11153	11534	11882	
11032	257	647	11157	11568		
11034	258	648	11158	11569		
11074	273	649	11160	11579		
11109	280	651	11161	11620		
11112	283	652	11162	11623		
11132@	299	653	11163	11640		
	323	654	11168	11643		
	365	670	11169	11646		
	366	821	11174	11648		
	367	822	11175	11651		
	368		11181	11652		
			11190	11657		

@ = Non-standard characteristics apply -- refer to Section 6.

SECTION 6

NON-STANDARD DEVICE SPECIFICATIONS

1. SCOPE

The scope of this section shall be to establish measurement techniques and individual device specifications that are either not covered by the main standard or are special exceptions to this standard. The exceptions may be due to device functional, design, or application considerations.

AC/ACT SCHMITT TRIGGER INPUT SPECIFICATIONS

Table 6-1
AC 11013, 14, 11014, 11132

SYMBOL	PARAMETER	V _{CC} V	T _A = 25°C		74ACXXXXX		54ACXXXXX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{T+}	Positive	3.0		2.2		2.2		2.2	V
	Going	4.5		3.2		3.2		3.2	
	Threshold Voltage	5.5		3.9		3.9		3.9	
V _{T-}	Negative	3.0	.5		.5		.5		V
	Going	4.5	.9		.9		.9		
	Threshold Voltage	5.5	1.1		1.1		1.1		
V _H	Hysteresis	3.0	.3	1.2	.3	1.2	.3	1.2	V
	Voltage	4.5	.4	1.4	.4	1.4	.4	1.4	
		5.5	.5	1.6	.5	1.6	.5	1.6	

Table 6-2
ACT 11013, 14, 11014, 11132

SYMB	PARAMETER	V _{CC} V	T _A = 25°C		74ACTXXXXX		54ACTXXXXX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{T+}	Positive Going Threshold Voltage	4.5		2.0		2.0		2.0	V
V _{T-}	Negative Going Threshold Voltage	4.5	.8		.8		.8		V
V _H	Hysteresis Voltage	4.5	.4	1.2	.4	1.2	.4	1.2	V

SECTION 7

SWITCHING SPEED STANDARDS FOR AC/ACT XXXXX DEVICES

1. SCOPE

This section shall establish standard limits for switching parameters for the device types listed herein. For test methodology, refer to the waveforms and load circuits of Section 3.

Refer to individual manufacturers data sheets for applicable propagation delay minimums. Derating calculations are not required, as the quoted parameter is valid over the temperature range stated.

2. FORM OF DEVICE TYPE TABLES

Standardized limits for switching parameters (dynamic characteristics) are specified by part identifier in numerical order. See Paragraph 3. for index of device functions.

All limits are in nanoseconds (ns), except f_{max} , which is in megahertz (MHz).

For each " $V_{CC} = 5 \pm 0.5 \text{ V}$ " entry, two limits are shown separated by a '/' (e.g. limit a/limit b). 'Limit a' is for AC parts and 'limit b' is for ACT parts. A dash '-' is inserted whenever a number is not yet specified for a given device. The limits in the " $V_{CC} = 3.3 \pm 0.3 \text{ V}$ " row apply only to AC parts.

3. INDEX OF DEVICE TYPE TABLES

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7.1.2 Two Wide Gates:

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7.1.3 Three Wide Gates:

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7.1.4 Four or More Wide Gates:

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SECTION 7

SWITCHING SPEED STANDARDS FOR AC/ACT XXXXX DEVICES

3. INDEX OF DEVICE TYPE TABLES (CONTINUED)

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TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS**7.1.1 One Wide Buffers/Inverters****AC/ACT04**

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	15.0	17.3	19.0	ns
		5 ± 0.5	7.1/7.9	7.7/9.0	8.5/9.3	ns

AC/ACT11004

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.0	10.0	10.4	ns
		5 ± 0.5	6.3/9.0	7.1/9.7	7.5/10.3	ns

AC/ACT14

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	14.0	15.2	16.8	ns
		5 ± 0.5	10.0/-	11.0/-	12.0/-	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.1 One Wide Buffers/Inverters (continued)

AC/ACT11014

Symbol	Parameter	VCC V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.3	10.1	10.6	ns
		5 ± 0.5	6.9/-	7.4/-	7.7/-	ns

AC/ACT11034

Symbol	Parameter	VCC V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.1	10.1	10.7	ns
		5 ± 0.5	6.3/8.9	6.9/9.9	7.4/10.5	ns

7.1.2 Two Wide Gates

AC/ACT00

Symbol	Parameter	VCC V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	11.2	12.9	14.2	ns
		5 ± 0.5	8.0/11.0	8.5/12.0	8.8/13.2	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.2 Two Wide Gates (continued)

AC/ACT11000

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.8	11.1	11.9	ns
		5 ± 0.5	6.5/10.9	7.4/12.3	8.1/13.3	ns

AC/ACT02

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	13.5	14.6	16.1	ns
		5 ± 0.5	9.6/10.2	10.4/11.1	11.5/12.2	ns

AC/ACT11002

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	8.6	9.9	10.7	ns
		5 ± 0.5	6.1/9.4	6.9/10.6	7.4/11.3	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.2 Two Wide Gates (continued)

AC/ACT08

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	10.5	11.4	12.6	ns
		5 ± 0.5	7.5/10.8	9.0/11.7	9.0/12.9	ns

AC/ACT11008

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.0	10.2	11.0	ns
		5 ± 0.5	6.2/8.0	6.9/9.0	7.3/9.4	ns

AC/ACT32

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	11.1	12.1	13.3	ns
		5 ± 0.5	7.9/10.1	9.0/11.0	9.5/12.1	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.2 Two Wide Gates (continued)

AC/ACT11032

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	8.7	9.7	10.7	ns
		5 ± 0.5	6.2/8.1	6.7/9.0	7.3/9.6	ns

AC/ACT86

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	12.6	14.0	15.1	ns
		5 ± 0.5	10.0/12.2	11.0/13.3	10.8/14.6	ns

AC/ACT11086

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.0	10.1	10.8	ns
		5 ± 0.5	6.7/8.7	7.4/9.4	7.8/9.9	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.2 Two Wide Gates (continued)

AC/ACT11132

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.0	9.7	10.2	ns
		5 ± 0.5	7.0/-	7.6/-	8.0/-	ns

AC/ACT11810

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	7.9	8.6	9.1	ns
		5 ± 0.5	6.2/7.2	6.7/7.8	7.1/8.1	ns

7.1.3 Three Wide Gates

AC/ACT10

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	13.0	15.0	16.5	ns
		5 ± 0.5	8.8/9.6	9.9/10.5	10.5/11.5	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.3 Three Wide Gates (continued)

AC/ACT11010

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.0	9.9	10.4	ns
		5 ± 0.5	6.4/8.2	7.0/8.9	7.4/9.3	ns

AC/ACT11

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	14.3	16.0	17.1	ns
		5 ± 0.5	10.2/11.3	11.1/12.3	12.2/13.5	ns

AC/ACT11011

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	8.3	9.1	9.7	ns
		5 ± 0.5	6.4/8.6	6.9/9.6	7.3/10.2	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.3 Three Wide Gates (continued)

AC/ACT11027

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
tpHL, tpLH	Maximum propagation delay	3.3 ± 0.3	10.9	12.0	12.9	ns
		5 ± 0.5	7.5/9.2	8.1/10.1	8.9/10.6	ns

7.1.4 Four or More Wide Gates

AC/ACT11013

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
tpHL, tpLH	Maximum propagation delay	3.3 ± 0.3	8.7	10.2	11.2	ns
		5 ± 0.5	7.0/-	8.1/0	8.8/-	ns

AC/ACT11020

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
tpHL, tpLH	Maximum propagation delay	3.3 ± 0.3	9.2	10.1	10.7	ns
		5 ± 0.5	6.7/8.5	7.3/9.2	7.7/9.8	ns

TABLE 7.1 GATES AND SIMPLE BUFFERS/INVERTERS (CONTINUED)

7.1.4 Four or More Wide Gates (continued)

AC/ACT11021

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	11.4	13.0	13.9	ns
		5 ± 0.5	7.8/8.8	8.8/9.8	9.4/10.4	ns

AC/ACT11030

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	9.1	9.9	10.6	ns
		5 ± 0.5	6.7/8.1	7.4/8.7	8.0/9.3	ns

TABLE 7.2 BUS DRIVERS, BUFFERS, AND TRANSCEIVERS

AC/ACT240

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	10.5	12.0	12.6	ns
		5 ± 0.5	7.5/8.5	8.2/9.5	9.0/9.5	ns
t _{PZL} , t _{PZH}	Maximum output enable delay OE --> Q	3.3 ± 0.3	14.0	16.0	16.8	ns
		5 ± 0.5	10.0/11.2	10.9/12.2	12.0/13.4	ns
t _{PLZ} , t _{PHZ}	Maximum output disable delay OE --> Q	3.3 ± 0.3	14.0	16.0	16.8	ns
		5 ± 0.5	10.0/11.2	10.9/12.2	12.0/13.4	ns

AC/ACT11240

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay A --> Q	3.3 ± 0.3	10.5	11.7	12.8	ns
		5 ± 0.5	7.5/9.9	8.4/10.6	9.0/11.1	ns
t _{PZL} , t _{PZH}	Maximum output enable delay OE --> Q	3.3 ± 0.3	11.6	12.7	13.4	ns
		5 ± 0.5	8.2/11.7	9.2/12.5	9.9/13.1	ns
t _{PLZ} , t _{PHZ}	Maximum output disable delay OE --> Q	3.3 ± 0.3	9.4	9.8	10.0	ns
		5 ± 0.5	7.3/10.3	7.7/10.8	8.0/11.2	ns

TABLE 7.2 BUS DRIVERS, BUFFERS, AND TRANSCEIVERS (CONTINUED)

AC/ACT241

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	11.4	13.0	13.3	ns
	A --> Y	5 ± 0.5	7.9/9.0	8.6/10.0	9.5/10.0	ns
t _{PZL} , t _{PZH}	Maximum output enable delay	3.3 ± 0.3	14.0	16.0	16.8	ns
	$\overline{\text{OE}}$ or OE --> Y	5 ± 0.5	10.0/11.2	10.9/12.2	12.0/13.4	ns
t _{PLZ} , t _{PHZ}	Maximum output disable delay	3.3 ± 0.3	14.0	16.0	16.8	ns
	$\overline{\text{OE}}$ or OE --> Y	5 ± 0.5	10.0/11.2	10.9/12.2	12.0/13.4	ns

AC/ACT11241

Symbol	Parameter	V _{CC} V	T _A = 25° C	74AC/ACTXXXXX	54AC/ACTXXXXX	Unit
t _{PHL} , t _{PLH}	Maximum propagation delay	3.3 ± 0.3	10.0	11.4	12.2	ns
	A --> Y	5 ± 0.5	7.1/9.0	8.0/10.0	8.5/10.7	ns
t _{PZL} , t _{PZH}	Maximum output enable delay	3.3 ± 0.3	11.4	12.9	13.8	ns
	$\overline{\text{OE}}$ or OE --> Y	5 ± 0.5	8.0/11.3	9.0/12.3	9.7/13.0	ns
t _{PLZ} , t _{PHZ}	Maximum output disable delay	3.3 ± 0.3	9.3	9.9	10.3	ns
	$\overline{\text{OE}}$ or OE --> Y	5 ± 0.5	7.5/11.2	8.0/11.7	8.3/12.0	ns