

JEDEC STANDARD

Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress

JESD202

MARCH 2006

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2006
2500 Wilson Boulevard
Arlington, VA 22201-3834

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

**PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications online at
<http://www.jedec.org/Catalog/catalog.cfm>**

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies
through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT-CURRENT AND TEMPERATURE STRESS

Contents

1	Scope	1
2	Significance and Use	1
2.1	Electromigration failure mechanism	1
2.2	Model for electromigration	1
2.3	Test vehicles (Al and Cu)	2
2.4	Wafer- and package-level test	2
2.5	Applications	2
2.6	Lower limit on t_{50}	2
3	Terms and definitions	3
4	Summary of Method	3
4.1	Procedure	3
4.2	Test options	4
4.3	Parameters to be selected	4
5	Precautions and Interferences	5
5.1	Errors in mean current density and temperature stresses	5
5.2	Deviations from the stress means	5
5.3	Thermal interactions	5
5.4	Selecting a percent change in resistance for failure criterion	6
5.5	Excluding test lines	7
5.6	Limit on applied voltage	7
5.7	Recovery from failure	7
5.8	Metallization stability	7
5.9	Lower limit on t_{50}	7
5.10	Normalization temperature	7
5.11	Test line geometry	8
5.12	Low-k dielectrics	8
5.13	Standard probe-pad layout	8
5.14	Temperature range	8
5.15	Convective heat loss	8
5.16	Degradation of thermocouple calibration	8
5.17	Effect of vias on t_{50} and sigma	9
6	Preparatory measurements	9
6.1	Elevated ambient temperature measurements	9
6.2	Temperature coefficient of resistance	10
6.3	Cross-sectional area	10
6.4	Stress current	12
6.5	Microscopic inspection	12

METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT-CURRENT AND TEMPERATURE STRESS

Contents

6.6	Thermal response time of package	12
6.7	Thermal resistance	13
7	Electrical test system	14
7.1	Stress current control	14
7.2	Display resolution	14
7.3	Maximum applied voltage	14
8	Procedure	15
8.1	Install test parts	15
8.2	Measure the resistance of test lines at the lower temperature	15
8.3	Determine $TCR(T_L)$ of the test lines to be measured	15
8.4	Calculate the stress current through each test structure	16
8.5	Measure test line resistance $R(tl)_H$ at the high ambient stress temperature T_H	16
8.6	Initiate the stress test	17
8.7	Determine time to failure of each test line	17
8.8	Determine the mean stress temperature T_m of the test lines	18
8.9	Verify if failure data can be modeled by a single log-Normal distribution	18
9	Analysis of <i>Complete</i> Time to Failure, t, Data	19
9.1	Calculate sample estimates of t_{50} and sigma	19
9.2	Calculate confidence limits of t_{50} and sigma	19
9.3	Calculate a sample estimate of t_p and its confidence limits	20
10	Analysis of Singly, Right-Censored Time to Failure, t, Data	21
10.1	Calculate sample estimates of t_{50} and sigma	21
10.2	Calculate approximate confidence limits of t_{50} and sigma	22
10.3	Calculate a sample estimate of t_p and its approximate confidence limits	23
11	Required Reporting	24
11.1	Test structure description	24
11.2	Test option, conditions, and results	24
12	References	24
	ANNEX A: Sample Calculations Involved in Sections 9 and 10	26

METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT CURRENT-DENSITY AND TEMPERATURE STRESS

(From JEDEC Board Ballot JCB-05-59, formulated under the cognizance of the JC-14 Committee on Quality and Reliability of Solid State Products.)

1 Scope

This is an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a log-Normal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Failure is defined as some pre-selected fractional increase in the resistance of the line under test. Analysis procedures are provided to analyze complete and singly, right-censored failure-time data. Sample calculations for complete and right-censored data are provided in Annex A. **The analyses are not intended for the case when the failure distribution cannot be characterized by a single log-Normal distribution.**

2 Significance and use

2.1 Electromigration failure mechanism

Electromigration is a metallization failure mechanism that leads to excessive increases in resistance or even an open circuit in metallizations. It is important to those who are concerned about the reliability of electrical interconnections in microelectronic circuits and devices. The stress drivers for this failure mechanism are current density and temperature. The method is used to provide failure-time data for: assessing metallization reliability, making major decisions for the selection of metallization and processing technologies, and monitoring process control. Failure is defined as some fractional increase in the resistance of a test line.

2.2 Model for electromigration

The method assumes that Black's equation [1] (eq. 1) can satisfactorily model how the sample estimate of the median-time-to-failure, t_{50s} , (from an accelerated electromigration stress test) depends on current density and temperature. The model parameters for temperature and current density are, respectively: the activation energy, E_a , and the value of the exponent, n , to which the current density, J , is raised.

$$t_{50s} = A \frac{\exp(E_a / kT)}{J^n} \quad (1)$$

where:

- A is a constant;
- n is a constant;
- J is the mean current density of the test lines stressed;
- E_a is the activation energy;
- k is Boltzmann's constant ($8.62 \cdot 10^{-5}$ eV/K); and
- T is the mean stress temperature of the test lines stressed.

NOTE Experimental determinations of model parameters n and E_a may be obtained by use of JEDEC standard JESD63 [2].

2 Significance and use (cont'd)

2.3 Test vehicles (Al and Cu)

The test vehicle is a four-terminal, thin-film, metal test line structure where the failure criterion is either an open circuit or a prescribed percent increase in the resistance of the line. Test lines may include contacts and vias to different metallization levels. The metal lines are made of aluminum- or copper-based, thin-film metallizations that are intended for use in microelectronic circuits and devices. The test line will consist of a primary conductor of aluminum or copper, and usually an adjoining thinner and higher resistivity conductor film. Aluminum metallizations may include a higher-resistivity, adjoining conductor film that can bypass an opening in the primary conductor due to electromigration. Test lines may have additionally adjacent-running lines that can serve as extrusion monitors. Copper metallizations will generally be of a damascene construction and be enclosed by a thin, higher-resistivity, adjoining copper-diffusion-barrier film. In both cases, these higher resistivity films are designed to conduct only a small fraction of the current in the undamaged test line.

2.4 Wafer- and package-level test

The method allows the test line to be stressed on a heated stage while still part of the wafer (or portion thereof) or stressed in an oven while bonded in a package and electrically accessible via package connections.

2.5 Applications

The method is intended for use as a referee method by different testing facilities and for use at testing stations for comparing different metallizations and different processing procedures, and for monitoring product reliability. It can be used as a tool in qualifying vendors and in determining the use-life of a metallization. It can also be used as an instructional instrument to aid first users and to alert the user to potential measurement interferences that could impact the accuracy of the sample estimates.

2.6 Lower limit on t_{50}

The method is normally intended for use under stress levels where the median-time-to-failure, t_{50} , is of the order of hours. Greater stress levels can be used to reduce the test time as long as the time to achieve the stress temperature in the test lines is less than a small fraction of t_{50} and no new failure modes or significant material changes are stimulated by the higher stress.

3 Terms and definitions

3.1 metallization: A thin-film metallic conductor used to interconnect microcircuit elements.

NOTE In addition to the primary, low-resistivity metal conductor, the metallization may include a thin, higher-resistivity adjoining film.

3.2 test line: A metallization line of specified dimensions, with or without vias making connections to over- or under-lying metal levels, whose length is defined by the location of two voltage taps used to make Kelvin-like resistance measurements of the test line when two other terminals force a current through the line.

NOTE It is assumed that the major portion of the test-line length will have a uniform cross-sectional area.

3.3 test structure: A passive metallization structure, including a test line, that is fabricated on a semiconductor wafer by procedures used to manufacture microelectronic integrated devices.

3.4 test chip: A part of a wafer, containing one or more test structures, that is stressed according to the test method either at the wafer level or in a package.

4 Summary of method

4.1 Procedure

The method involves subjecting a sample of N test lines to high current-density and high ambient temperature stress, calculating the mean stress temperature of the test line (which includes any Joule heating) before any significant electromigration damage can occur, and measuring the time to failure of each test line, t .

A test is performed to determine if the experimentally determined failure times can be modeled by a single log-Normal distribution with the parameters t_{50} (median time to failure) and σ (sigma).

If the test is conducted until all parts on test have failed, so that the fail time data is complete, then the sample estimate of the median-time-to-failure, t_{50s} , for the stress conditions used in the test, is given by the exponential of the mean of the logarithms of the time-to-failure values:

$$t_{50s} = \exp[(\ln t)_{mean}] \quad (2)$$

And, the sample estimate of the sigma of the distribution, s , is given by the standard deviation of the logarithm of the time-to-fail values:

$$s = \sqrt{\sum_{i=1}^N (\ln t_i - (\ln t)_{mean})^2 / (N-1)} \quad (3)$$

4 Summary of method (cont'd)

4.1 Procedure (cont'd)

Confidence limits for the sample estimates of t_{50} and s are calculated with the use of the t -distribution and the chi-squared distribution, respectively. The p -th percentile of the fail time distribution, t_{ps} , is computed from $t_{ps} = \exp(t_{50s} + z_p s)$, where z_p is the p -th percentile of the standard normal distribution. Estimated confidence limits for t_p are calculated using the noncentral t -distribution.

If the test is halted before all parts on test have failed, so that the fail time data is censored, then a method based on the Persson and Rootzen approach is used, which gives closed-form estimators of t_{50} and sigma. Approximate confidence limits for t_{50} , sigma, and t_p are developed from the work of Meeker using the Normal-approximation method.

4.2 Test options

Three testing options are included in the test method, each involving somewhat different considerations:

Option 1 - The test structures to be stressed are part of either the entire or some portion of a wafer that is placed on a heated stage. The test structures are contacted by individual or a fixed array of probes and are stressed sequentially. This requires the dedication of a wafer-probe station.

Option 2 - Each test structure is individually packaged and stressed in a temperature-controlled oven. The thermal response time of a packaged test structure is dependent on the size and design of the package and may be of the order of several minutes. Therefore, if Joule heating is significantly large, the measurement of the stress temperature of the test line at the beginning of the test will need to be delayed until the test line is in thermal equilibrium with its package.

Option 3 – Adjacent lying test lines on a wafer or in a package are stressed at the same time. Part of the heat path to the stress ambient of each test line is shared by the others. Hence, the test lines communicate thermally with each other during the stress test. For this reason, the option may, in addition, require a calculation of a thermal resistance that is used to calculate the mean stress temperatures of the test lines as each fails and the total power dissipation decreases.

4.3 Parameters to be selected

Before the test method can be implemented, a number of parameters must be selected and agreed upon by the parties to the test.

4.3.1 Select the *ambient stress temperature*, which is the temperature of the heated stage for wafer-level testing and that of the oven for package-level testing. See 5.12 for test lines with low-k dielectrics.

4.3.2 Select the *current-density stress* in the primary conductor of the test line (see 6.4).

4.3.3 Select the *temperature*, T_n , to which the failure-time data shall be normalized (5.10).

4.3.4 Select the *failure criterion* (5.4).

4 Summary of method (cont'd)

4.3 Parameters to be selected (cont'd)

4.3.5 Select the *number, N , of the lines* to be stressed.

NOTE Both N and the sample estimate of sigma (eq. 3) are used in 9.2 to determine the confidence limits for the sample estimates of t_{50} and σ when all test lines have failed.

4.3.6 Select the *design width, thickness, and length* of the test lines to be used (see 5.11 and 5.4.3)

4.3.7 Select the value of the *activation energy, E_a* (5.10).

4.3.8 Select the *confidence percentile* to be used.

5 Precautions and interferences

5.1 Errors in mean current density and temperature stresses

Errors in estimating the mean current density and temperature stresses will lead to errors in the sample estimate of t_{50} (i.e. t_{50s}) that can be calculated from eq. 1. For example, calculations for aluminum metallizations [3] indicate that the induced percent error in t_{50s} can be between two and three times the percent error in estimating the current density and can be between 15% and 20% if there is a 5 °C error in estimating the stress temperature between 150 °C and 200 °C.

5.2 Deviations from the stress means

Deviations from the stress means of current density and temperature of the individual test lines produces changes in the time to failure, t , of these test lines. These changes lead, in turn, to increases in the sample estimate of sigma, s , and in the confidence limits for t_{50} and sigma. Deviations should be kept small enough that they do not produce changes in t by more than 20% [3]. This is especially important when sigma is less than 0.4. The effect of stress deviations on t is calculated from eq. 1 by substituting t for t_{50s} .

5.3 Thermal interactions

Thermal interactions can interfere with making accurate estimates of the mean stress temperature of individual test lines during the test. Such interactions need to be considered when the following two conditions exist: 1) when the stress current density is large enough to cause significant Joule heating in the test lines and 2) when a number of adjacent lying test lines on a chip in a package or on a wafer are stressed at the same time.

Thermal interactions among the test lines can be important when a portion of the heat path from each test line to the stress-temperature ambient is shared. In packaged test lines, an obvious shared heat path is through the interface between the bottom of the chip and the package and through the package to the high-temperature ambient of the oven in which the package is housed. The temperature drop across the interface and through the package will be equal to the product of the power dissipated by the test lines and the thermal resistance associated with the heat path in the interface and package.

5 Precautions and interferences (cont'd)

5.3 Thermal interactions (cont'd)

If, for example, each test line fails because of an open circuit, then as each line fails the remaining lines on the test will be subjected to a step-wise decrease in stress temperature (see 6.7 and 8.8.2).

In contrast to packaged test lines, thermal interactions of test lines on a wafer will generally be negligible. This is because the thermal resistance associated with the interface between the bottom side of the wafer and the top surface of the heated stage is generally negligible in comparison to the thermal resistance associated with the heat paths through the silicon chip and through any intervening dielectric layers between the test line and the silicon chip. But, if there is poor thermal contact at this interface then significant thermal interactions among the test lines may occur (see, for example, Figure 6 in ref. 4). If test lines are sufficiently closely spaced, some overlapping of the heat paths in the silicon and the intervening dielectric layers may occur that will also lead to thermal interactions.

A direct way to test for the existence of significant thermal interactions among test lines is to monitor the resistance of one test line as a current sufficient to cause measurable Joule heating is switched on in another test line. An increase in resistance of the first line is indicative of a thermal interaction.

5.4 Selecting a percent change in resistance for the failure criterion

5.4.1 Aluminum metallizations

Open-circuit line failures are seen in aluminum lines with no adjoining high-resistivity films. Such lines usually exhibit a significant increase in line resistance only near the end of life. Hence, if a relatively high percent increase in resistance is selected for the failure criterion no significant difference in the time to failure is incurred by not waiting for essentially an open circuit to occur.

5.4.2 Multilayer metallizations

The use of a relatively small percent increase in resistance as a failure criterion is necessary when testing multilayered metallizations. Such metallizations usually have an adjoining refractory metal film for aluminum-based conductors or have a higher resistivity, diffusion-barrier adjoining film for copper-based conductors. The use of higher resistivity adjoining films in these metallizations usually prevents an open-circuit failure of the test line. Using too high a percent increase may affect significantly the sample estimates of the activation energy, value for n , and t_{50s} [5]. The use of percent increases greater than 30% has been reported to lead to large variability in test results [5] and to resistance oscillations due to the formation of open circuits in all but the adjoining refractory films, when testing unpassivated aluminum-based metallizations [6].

5.4.3 Effect of line length

When selecting a value for the percent increase in resistance as a failure criterion, it should be recognized that this value represents a measure of the amount of metal movement or voiding in the metal line that must occur *relative to its length* before failure is declared. Hence, to make fair comparisons between the results of tests using different lengths, the failure criterion used in these tests must be adjusted for the difference in length. A corollary is that in any given test, all the test lines must be of the same length, otherwise an overestimate of the sigma and an uncertain error in t_{50s} will be made. (See 4.3.6.)