

JEDEC STANDARD

Serial Interface for Data Converters

JESD204C.1

(Revision of JESD204C December 2017)

DECEMBER 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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SERIAL INTERFACE FOR DATA CONVERTERS

CONTENTS_Toc62286702

1	Scope	1
2	Normative references	3
3	Terminology	4
3.1	Terms and definitions	4
3.2	Symbols and abbreviated terms	9
4	Introduction and common requirements	16
4.1	Application overview	16
4.1.1	Background	16
4.1.2	Physical layer overview	17
4.1.3	Transport and link layer overview	18
4.1.3.1	Data encoding and organization	18
4.1.3.2	Clocking	18
4.1.3.3	Sync header stream	20
4.1.3.4	Deterministic latency	20
4.1.4	Data link properties	20
4.1.4.1	Variants and modes	21
4.1.5	Configuration examples	21
4.1.5.1	General	21
4.1.5.2	Single-device ADC application	21
4.1.5.3	Single-device DAC application	23
4.2	Deterministic latency	24
4.2.1	Introduction and general requirements	24
4.2.2	No support for deterministic latency (device subclass 0 and device subclass 1 using MULTIREF)	27
4.2.3	Deterministic latency using SYSREF (device subclass 1)	27
4.2.4	Deterministic latency using SYNC~ detection (device subclass 2)	27
4.3	Physical timing	28
4.3.1	Device clock	28
4.3.2	Link layer clock	29
4.3.3	Transport layer clock	29
4.3.4	Local multiframe and extended multiblock clocks (LMFC and LEMC)	30
4.3.5	SYSREF signal (device Subclass 1)	30
4.3.6	MULTIREF signal (device subclass 1)	32
4.3.7	SYNC~ generation and detection clocks (8B/10B link layer)	34
4.3.8	Skew and latency variation budget	35
4.4	Control interfaces	46
4.5	Device classification	46
4.5.1	Classes	46
4.5.2	Device subclassification	46
4.5.3	Features to be declared	47
5	Physical layer specification	48
5.1	Category B physical layer specification	48
5.1.1	Electrical specification overview	48
5.1.2	Compliance types	49
5.1.3	Transmission medium	50
5.1.3.1	Transmission medium insertion loss	51
5.1.4	Class B-3 (LV-OIF-SxI5)	51
5.1.4.1	Compliance	51
5.1.4.2	Transmitter	52
5.1.4.3	Receiver	53
5.1.5	Class B-6 (LV-OIF-6G-SR)	55
5.1.5.1	Compliance	55
5.1.5.2	Transmitter	56

SERIAL INTERFACE FOR DATA CONVERTERS

CONTENTS (cont'd)

5.1.5.3	Receiver.....	58
5.1.6	Class B-12 (LV-OIF-11G-SR)	59
5.1.6.1	Applicability above 11.1 Gbps.....	59
5.1.6.2	Compliance	60
5.1.6.3	Transmitter	61
5.1.6.4	Receiver.....	63
5.2	Category C physical layer specification.....	65
5.2.1	Overview	65
5.2.2	Compliance	65
5.2.2.1	Compliance types	65
5.2.2.2	System compliance.....	66
5.2.3	Transmitter characteristics	66
5.2.3.1	Transmitter electrical specifications	66
5.2.3.2	Transmitter test fixture	68
5.2.3.3	Signaling rate and range	70
5.2.3.4	Signaling levels	70
5.2.3.5	Transmitter transition (rise/fall) time	71
5.2.3.6	Transmitter output return loss	72
5.2.3.7	Transmitter output waveform.....	73
5.2.3.8	Transmitter output noise and distortion.....	76
5.2.3.9	Waveform acquisition	76
5.2.3.10	Test pattern.....	77
5.2.3.11	Linear fit to the waveform measured at TP0a	77
5.2.3.12	Removal of the transfer function between the transmit function and TP0a.....	78
5.2.3.13	Transmitter output jitter.....	78
5.2.3.13.1	Overview	78
5.2.3.13.2	Even-odd jitter (DCD).....	79
5.2.3.13.3	Effective bounded uncorrelated jitter (EBUJ) and effective random jitter (ERJ).....	79
5.2.4	Receiver characteristics	80
5.2.4.1	Receiver electrical specifications	80
5.2.4.2	Receiver test fixture	82
5.2.4.3	Signaling rate and range	84
5.2.4.4	Receiver input return loss.....	84
5.2.4.5	Receiver interference tolerance	86
5.2.4.5.1	Additive broadband noise characteristics	88
5.2.4.6	Receiver jitter tolerance.....	89
5.2.5	Channel characteristics	90
5.2.5.1	Insertion loss	90
5.2.5.2	Isolation in package and footprint area.....	91
5.2.5.3	Channel Operating Margin	93
5.2.5.4	Transmitter and receiver device package models.....	98
5.2.5.5	Filters.....	98
5.2.5.5.1	Receiver noise filter	99
5.2.5.5.2	Transmitter equalizer.....	99
5.2.5.5.3	Receiver equalizer.....	99
6	Transport layer.....	100
6.1	Overview	100
6.2	User data format for an independent lane	100
6.2.1	General	100
6.2.2	User data mapping without oversampling	101
6.2.3	User data mapping with oversampling	103

SERIAL INTERFACE FOR DATA CONVERTERS

CONTENTS (cont'd)

6.3	User data format for multiple lanes	104
6.4	Tail bits	107
6.5	Idle mode	107
6.5.1	General	107
6.5.2	Dummy Samples	107
6.6	Test modes	108
6.6.1	General	108
6.6.2	Short transport layer test pattern	108
6.6.3	Long transport layer test pattern	109
7	64B/66B and 64B/80B link layer	110
7.1	Overview	110
7.1.1	64B/66B and 64B/80B encoding	110
7.1.2	Block structure	110
7.1.3	Multiblock structure	111
7.1.4	Extended multiblock structure	111
7.1.5	Data channel	111
7.1.6	Sync header stream	111
7.2	Physical coding sublayer	112
7.2.1	Overview	112
7.2.2	Transmit process	112
7.2.3	Receive process	114
7.2.4	Scrambling and descrambling	114
7.2.4.1	Overview	114
7.2.4.2	Scrambler	115
7.2.4.3	Descrambler	115
7.2.5	Fill bits for 64B/80B encoding	116
7.2.6	Gearbox	117
7.3	Sync header stream	117
7.3.1	Overview	117
7.3.2	Sync header encoding and decoding	117
7.3.3	Pilot signal	118
7.3.4	CRC-12 signal	118
7.3.5	CRC-3 signal	119
7.3.6	FEC signal	120
7.3.7	Command channel	121
7.3.7.1	Overview	121
7.3.7.2	Stand-alone command channel	121
7.3.7.3	Command word encoding	122
7.3.7.4	Header and payload sequence	123
7.3.7.5	Operating modes	124
7.3.7.6	Function codes	125
7.4	CRC encoding	125
7.4.1	General	125
7.4.2	CRC-12 encoding	126
7.4.3	CRC-3 encoding	127
7.5	FEC encoding	128
7.5.1	General	128
7.5.2	FEC encoding	128
7.5.3	FEC decoding	129
7.5.3.1	FEC code reconstruction	129
7.5.3.2	FEC code decoding	130

SERIAL INTERFACE FOR DATA CONVERTERS

CONTENTS (cont'd)

7.6	Receiver Operation	133
7.6.1	Sync header alignment	133
7.6.2	Extended multiblock alignment	134
7.6.3	Error handling	136
7.6.3.1	Error kinds.....	136
7.6.3.2	Action taken on error.....	137
7.6.3.3	Error reporting via control interface.....	137
8	8B/10B link layer	138
8.1	8B/10B encoding	138
8.2	Transmission order	138
8.3	Scrambling	139
8.3.1	Introduction	139
8.3.2	Scrambler polynomial	139
8.3.3	Scrambler bit order	140
8.3.4	Scrambler type	141
8.3.5	Early synchronization option	142
8.3.6	Initial state	143
8.3.7	Scrambling disable	143
8.4	Link operation	144
8.4.1	Code group synchronization	144
8.4.2	Combination of synchronization requests	146
8.4.3	Initial frame synchronization	147
8.4.4	Frame alignment monitoring and correction	147
8.4.4.1	Alignment characters.....	147
8.4.4.2	Character replacement without scrambling.....	148
8.4.4.3	Character replacement with scrambling	149
8.4.4.4	Frame alignment correction in the RX	150
8.4.5	Initial lane alignment	150
8.4.5.1	General principles	150
8.4.5.2	Multiframes.....	151
8.4.5.3	Initial lane alignment sequence	151
8.4.6	Lane alignment monitoring and correction	153
8.4.7	Link reinitialization	154
8.4.8	Test modes	154
8.4.8.1	General	154
8.4.8.2	Test sequences.....	155
8.5	Deterministic latency using SYNC~ detection (device subclass 2)	156
8.5.1	Introduction	156
8.5.2	Accuracy limitations	156
8.5.3	Principles of SYNC~ sampling	159
8.5.3.1	General	159
8.5.3.2	SYNC~ generation at the RX device.....	159
8.5.3.3	Adjustment resolution and adjustment clock.....	159
8.5.3.4	Detection resolution at the TX device	160
8.5.3.5	SYNC~ de-assertion detection and the detection interval	160
8.5.4	Initiator and target configurations	161
8.5.4.1	Introduction	161
8.5.4.2	ADC initiator and target configurations	162
8.5.4.3	DAC initiator and target configurations	163
8.5.5	Summary of requirements for subclass 2 deterministic latency	167
8.6	Receiver operation.....	168

SERIAL INTERFACE FOR DATA CONVERTERS

CONTENTS (cont'd)

8.6.1	Code group synchronization	168
8.6.2	Initial frame synchronization	170
8.6.3	Initial lane alignment	172
8.6.4	Monitoring and correction of frame and lane alignment	172
8.6.5	Error handling	176
8.6.5.1	Error kinds.....	176
8.6.5.2	Data output on error	176
8.6.5.3	Errors requiring reinitialization	177
8.6.5.4	Error reporting via the SYNC interface.....	177
8.6.5.5	Error reporting via a control interface	177
8.7	Transmitter operation	178
8.7.1	Synchronization	178
8.7.2	Handling of error reports and synchronization requests	180
8.7.2.1	Hard-wired SYNC interface	180
8.7.2.2	Soft SYNC interface.....	180
8.7.3	SYNC~ detection in device subclass 2	181
8.8	SYNC interface	182
8.8.1	Introduction	182
8.8.2	Hard-wired SYNC interface	182
8.8.3	Soft SYNC interface	186
8.9	Link configuration parameters and their encoding	186
Annex A (informative)	Differences between revisions	190
A.1	Differences between JESD204C and JESD204C.01	190
A.2	Differences between JESD204B and JESD204C	191
Annex B (informative)	Example of device clock and SYSREF generation	196
Annex C (informative)	Background of the values in the skew budget	198
C.1	Transmission skew	198
C.2	Timing reference skew	199
C.2.1	SYSREF and device clock skew	199
C.2.2	Device clock and MULTIREF skew	199
C.2.3	SYNC~ skew	200
C.3	Processing skew in logic device	201
C.4	Processing skew in converter device	205
C.5	Skew variation	205
Annex D (informative)	Scattering parameters computations	206
D.1	Cascade connection of two-port networks	206
D.2	Renormalization of reference port impedances	206
D.3	Two-port network for a differential shunt capacitance	207
D.4	Two-port network for a differential serial inductor	207
D.5	Two-port network for a differential series resistance-inductance combination	208
Annex E (normative for category B)	Linear insertion loss fit	209
Annex F (normative for category C)	Quadratic insertion loss fit	211
F.1	Differential insertion loss	211
F.2	Differential insertion loss deviation	214
Annex G (informative)	Physical layer implementation	215
G.1	Transmitter	215
G.2	Receiver	216
Annex H (normative)	Pseudo-random binary sequence (PRBS) generation	217
Annex I (informative)	Transport layer configuration parameters	218
Annex J (informative)	Forward error correction decoding	219
J.1	Binary cyclic codes decoding	219

SERIAL INTERFACE FOR DATA CONVERTERS

CONTENTS (cont'd)

J.2	Shortened cyclic codes decoding	221
Annex K (informative)	Clock Terminology for 64B/66B and 64B/80B link layer	224
Annex L (informative)	Clock Terminology for 8B/10B link layer	225
Annex M (informative)	Backward compatibility of 8B/10B link layer with previous versions of JESD204	226
Annex N (informative)	Device level implementation for 8B/10B link layer.....	228
N.1	TX link layer.....	228
N.2	RX Link Layer.....	229
Annex O (informative)	Parallel scrambler and descrambler implementations.....	230
Annex P (informative)	Bibliography	235

SERIAL INTERFACE FOR DATA CONVERTERS

FIGURES

Figure 1 — JESD204 layer relationship to the IEEE Ethernet model	6
Figure 2 — Scope of original JESD204 and revisions A, B, and C	2
Figure 3 — Single device ADC application	22
Figure 4 — Single device DAC application	23
Figure 5 — Timing diagram illustrating the RX elastic buffer release opportunity in a JESD204C 8B/10B system	26
Figure 6 — SYSREF sampling illustration	31
Figure 7 — SYSREF and MULTIREF signal timing	32
Figure 8 — Examples of MULTIREF distribution. Left: multidrop, and right: daisy chain topology	33
Figure 9 — Illustration of skew items in configuration with multiple ADC devices	36
Figure 10 — Illustration of skew items in configuration with multiple DAC devices	37
Figure 11 — Definition of the skew points on a multipoint ADC link	38
Figure 12 — Definition of the skew points on a multipoint DAC link	38
Figure 13 — Transmitter output voltage definitions. v_d is the differential voltage, v_{cm} is the common-mode voltage	48
Figure 14 — Transmission medium differential insertion loss mask. Data rate f_b in Hertz	51
Figure 15 — Transmit eye mask for class B-3-based operation	53
Figure 16 — Line termination at receiver	54
Figure 17 — Receive eye mask for class B-3-based operation	54
Figure 18 — Transmit eye mask for class B-6-based operation	57
Figure 19 — Receive eye mask for class B-6-based operation	59
Figure 20 — Transmit eye mask for class B-12-based operation	62
Figure 21 — Receive eye mask for class B-12-based operation	64
Figure 22 — Transmitter test fixture and test points	68
Figure 23 — Transmitter test fixture differential reference insertion loss with $f_b = 32$ Gbps	69
Figure 24 — Transmitter test fixture differential return loss limit with $f_b = 32$ Gbps	70
Figure 25 — Transmitter output voltage definitions. v_d is the differential voltage, v_{cm} is the common-mode voltage	71
Figure 26 — Transmitter differential return loss	72
Figure 27 — Transmitter common-mode return loss limit	73
Figure 28 — Transmit equalizer functional model	74
Figure 29 — Receiver test fixture and test points	82
Figure 30 — Receiver test fixture reference differential insertion loss with $f_b = 32$ Gbps	83
Figure 31 — Receiver test fixture differential return loss limit with $f_b = 32$ Gbps	84
Figure 32 — Receiver differential return loss with $f_b = 32$ Gbps	85
Figure 33 — Receiver differential-to-common-mode return loss limit	85
Figure 34 — Setup to test receiver jitter tolerance with no relative wander	89
Figure 35 — Total wander mask	90
Figure 36 — Insertion loss limit	91
Figure 37 — $PSNEXT$ and $PSFEXT$ limit lines with $f_b = 32$ Gbps	92
Figure 38 — User data format for an independent lane without oversampling	102
Figure 39 — JESD204 version 2006 and newer versions compared for a 4×12 -bit converter with control bit over a single lane, no control words	102
Figure 40 — User data format with control word (Example for 4×12 -bit converter)	103
Figure 41 — User data format for an independent lane with oversampling	103
Figure 42 — User data format with oversampling (Example for 4×12 -bit converter, $2 \times$ oversampling and control word)	104
Figure 43 — User data format for multiple lanes	104
Figure 44 — Multilane user data format for $16 \times (11+2)$ -bit converter without control word	105
Figure 45 — Multilane user data format for $16 \times (11+2)$ -bit converter with single control word	106
Figure 46 — Multilane user data format for $16 \times (11+2)$ -bit converter with two control words	106

SERIAL INTERFACE FOR DATA CONVERTERS

FIGURES (cont'd)

Figure 47 — Example of transport layer test sequence for a two-times oversampling dual 14-bits converter with one control bit	109
Figure 48 — 64B/66B block format	110
Figure 49 — 64B/80B block format	110
Figure 50 — Multiblock format	111
Figure 51 — Extended Multiblock Format	111
Figure 52 — PCS transmit bit ordering	112
Figure 53 — Mapping from transport layer to link layer	113
Figure 54 — PCS receive bit ordering	114
Figure 55 — Serial scrambler implementation	115
Figure 56 — Serial descrambler implementation	115
Figure 57 — 64B/80B fill bit mapping	116
Figure 58 — Payload size examples (CRC utilized)	123
Figure 59 — Payload Size Examples (stand-alone command channel)	123
Figure 60 — Command channel operating modes (CRC utilized)	124
Figure 61 — Command channel operating modes (stand-alone command channel)	124
Figure 62 — CRC-12 field generation	126
Figure 63 — CRC-3 field generation	127
Figure 64 — Serial FEC Encoder	129
Figure 65 — Codeword reconstruction at the receiver	129
Figure 66 — (2074, 2048) fire decoder	130
Figure 67 — Decoder sequencing state machine	131
Figure 68 — Receiver state machine for sync header alignment	133
Figure 69 — Receiver state machine for extended multiblock alignment	135
Figure 70 — Functional location of scrambler and descrambler	139
Figure 71 — Serial scrambling	140
Figure 72 — Serial scrambler and descrambler implementation and equations for parallel implementation	141
Figure 73 — Alternative serial scrambler and descrambler implementation and equations for parallel implementation	142
Figure 74 — Synchronization process for subclass 0	145
Figure 75 — Synchronization process for subclasses 1 and 2	145
Figure 76 — Examples of SYNC~ signal combination	146
Figure 77 — Examples of non-combined SYNC~ signaling	147
Figure 78 — Initial lane alignment sequence with four multiframe	152
Figure 79 — Character specification for initial lane alignment sequence	152
Figure 80 — PVT effects on SYNC~ detection and generation	158
Figure 81 — Relationship of detection interval to system signals (DAC link)	161
Figure 82 — ADC reset as a result of SYNC~ de-assertion detection	163
Figure 83 — Example state diagram of TX logic device supporting subclass 2 deterministic latency	165
Figure 84 — Example state diagram of DAC device supporting deterministic latency	166
Figure 85 — Receiver state machine for code group synchronization	169
Figure 86 — State machine for frame synchronization in receivers supporting reinitialization over the data interface	170
Figure 87 — Alternative state machine for frame synchronization in receivers <i>not</i> supporting reinitialization over the data interface	171
Figure 88 — Pseudo-code for frame alignment monitoring and correction in receiver	172
Figure 89 — Pseudo-code for lane alignment monitoring and correction in receiver	174
Figure 90 — Transmitter state machine	178
Figure 91 — SYNC~ signal timing for JESD204A compatible subclass 0 and for subclass 2 devices	184
Figure 92 — Associated edges for JESD204A compatible subclass 0 and subclass 2 devices	185
Figure B.93 — Typical implementation of device clock and SYSREF generation	197

SERIAL INTERFACE FOR DATA CONVERTERS

FIGURES (cont'd)

Figure B.94 — Timing diagram	197
Figure C.95 — JESD204 system for illustration of transmission and timing reference skews	198
Figure C.96 — Typical implementation of an 8B/10B or 64B/80B TX in a logic device.....	201
Figure C.97 — Typical implementation of an 8B/10B or 64B/80B RX in a logic device	202
Figure C.98 — Typical implementation of a 64B/66B TX in a logic device	203
Figure C.99 — Typical implementation of a 64B/66B RX in a logic device	203
Figure D.100 — Differential shunt capacitor	207
Figure D.101 — Differential series inductance	207
Figure D.102 — Differential series resistance-inductance combination	208
Figure J.103 — Generic structure of a single-link transmitter block.....	215
Figure J.104 — Transmitter physical layer.....	215
Figure G.105 — Generic structure of a receiver block.....	216
Figure G.106 — Receiver physical layer.....	216
Figure J.107 — Decoding example of a correctable error located within parity bits	219
Figure J.108 — $s(x) \neq e(x)$, when $\text{degree}(e(x)) > \text{degree}(g(x))$	220
Figure J.109 — Error correction using error trapping	220
Figure J.110 — Syndrome Computation for rotated word	221
Figure J.111 — Shortened Codeword Syndrome Computation.....	222
Figure J.112 — Rotating the syndrome by $n-k$ bits aligns the error with the received word.....	223
Figure K.113 — Relation diagram for JESD204 clocks.....	224
Figure L.114 — Relation diagram for JESD204 clocks	225
Figure O.115 — 8-bit parallel implementation of self-synchronous scrambler based on $1+x^{14}+x^{15}$	230
Figure O.116 — 8-bit parallel implementation of self-synchronous descrambler based on $1+x^{14}+x^{15}$	231
Figure O.117 — 8-bit parallel implementation of alternative early-synchronization scrambler	232
Figure O.118 — 16-bit parallel implementation of self-synchronous scrambler based on $1+x^{14}+x^{15}$	233
Figure O.119 — 16-bit parallel implementation of self-synchronous descrambler based on $1+x^{14}+x^{15}$	234

SERIAL INTERFACE FOR DATA CONVERTERS

TABLES

Table 1 — Data rate range for each data interface	17
Table 2 — JESD204C 32.45 Gbps interface device class features.....	17
Table 3 — Supported link layers versus data rate	18
Table 4 — Skew budget for subclass 0 ADC and DAC links	40
Table 5 — Skew budget for subclass 1 ADC links	41
Table 6 — Skew budget for subclass 1 DAC links	42
Table 7 — Skew budget for subclass 2 ADC links	43
Table 8 — Skew budget for subclass 2 DAC links	44
Table 9 — Maximum skew variation for subclass 0 ADC and DAC links	45
Table 10 — Maximum skew variation for subclass 1 and 2 links	46
Table 11 — Device classification.....	46
Table 12 — Device subclassification	47
Table 13 — Supported features to be declared by manufacturers	47
Table 14 — General differential output DC and AC characteristics for class B-3	52
Table 15 — General differential input DC and AC characteristics for class B-3	53
Table 16 — General differential output DC and AC characteristics for class B-6	56
Table 17 — General differential input DC and AC characteristics for class B-6	58
Table 18 — General differential output DC and AC characteristics for class B-12	61
Table 19 — General differential input DC and AC characteristics for class B-12	63
Table 20 — Category C receiver features.....	65
Table 21 — Category C transmitter electrical specification at TP0a.....	67
Table 22 — Linear fit pulse and equalizing filter parameters	75
Table 23 — Category C receiver electrical specification	81
Table 24 — Receiver interference tolerance parameters, Class-CS	87
Table 25 — Receiver interference tolerance parameters, Class-CM.....	87
Table 26 — Receiver interference tolerance parameters, Class-CR.....	88
Table 27 — COM parameters for class C-S	93
Table 28 — COM parameters for class C-M.....	95
Table 29 — COM parameters for class C-R.....	97
Table 30 — Scrambler example; initial state 0x01.....	115
Table 31 — Fill bit encoding.....	116
Table 32 — SYNC Header Encoding.....	117
Table 33 — SYNC header decoding	117
Table 34 — Sync word mapping with CRC-12 signal	118
Table 35 — Meaning of the CRC-12 sync word fields	118
Table 36 — Sync word mapping with CRC-3 signal	119
Table 37 — Meaning of the CRC-3 sync word fields	119
Table 38 — Sync word mapping with FEC signal	120
Table 39 — Meaning of the FEC sync word fields	120
Table 40 — Sync word mapping with stand-alone command channel.....	121
Table 41 — Meaning of the Cmd sync word fields.....	121
Table 42 — Command word encoding with CRC utilized.....	122
Table 43 — Command word encoding for stand-alone command channel.....	122
Table 44 — Command word function definitions	125
Table 45 — CRC12 example.....	126
Table 46 — CRC-3 example	127
Table 47 — FEC Block Boundary Example.....	129
Table 48 — FEC MultiBlock Boundary Example.....	129
Table 49 — Minimum set of errors to detect per receiver.....	136
Table 50 — Action taken on detected error.....	137
Table 51 — Variables used in receiver state machine for code group synchronization	169

SERIAL INTERFACE FOR DATA CONVERTERS**TABLES (cont'd)**

Table 52 — Variables used in initial frame synchronization.....	171
Table 53 — Variables and functions in frame alignment monitoring and correction.....	173
Table 54 — Variables and functions in lane alignment monitoring and correction	175
Table 55 — Minimum set of errors to detect per receiver.....	176
Table 56 — Variables and functions in transmitter state machine	179
Table 57 — Link configuration parameters and their encoding in the ILAS	187
Table 58 — Mapping of link configuration fields to octets.....	189
Table C.59 — Partitioning of the skew limit in the TX (link layer and PHY)	204
Table C.60 — Partitioning of the skew limit in the RX (link layer and PHY)	205
Table E.61 — Category B linearly-fitted differential insertion loss characteristics	210
Table F.62 — Class C-S channel fitted differential insertion loss characteristics	213
Table F.63 — Class C-M channel fitted differential insertion loss characteristics.....	213
Table F.64 — Class C-R channel fitted differential insertion loss characteristics.....	213
Table G.65 — PRBS polynomial taps	217
Table K.66 — Clock ratios with respect to extended multiblock clock	224
Table L.67 — Clock ratios with respect to the multiframe clock.....	225
Table M.1 — SYNC~ conditions for interoperability	227

Foreword

The JESD204 standard separates the communication mechanism between logic devices and data converters into three layers, each with a distinct function: physical (specified in clause 5), link (64B/66B and 64B/80B encoding specified clause 0, and 8B/10B encoding specified in clause 0), and transport (specified in clause 0). The JESD204 physical layer encompasses the PMA and PMD Ethernet layers; the JESD204 link layer encompasses the FEC and PCS Ethernet layers and additional CRC and alignment functionality. Finally, the JESD204 transport layer maps to the MAC Ethernet layer (Figure 1).

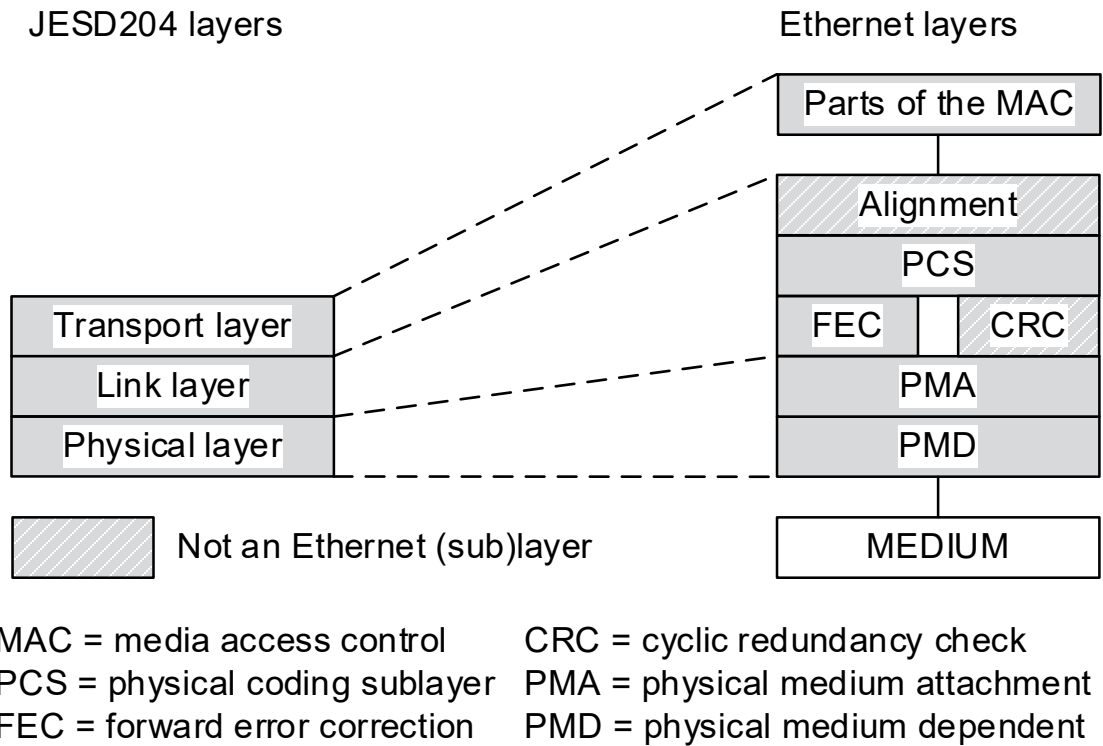


Figure 1 — JESD204 layer relationship to the IEEE Ethernet model

The JESD204C.01 standard replaces JESD204C, which replaced JESD204B standard.

SERIAL INTERFACE FOR DATA CONVERTERS

(From JEDEC Board Ballot JCB-21-56, formulated under cognizance of the JEDEC JC-16 Committee on Interface Technology.)

1 Scope

This standard describes a serialized interface between data converters and logic devices. It contains normative information to enable designers to implement devices that communicate with other devices covered by this specification. Informative annexes are included to clarify and exemplify the document.

Due to the range of applications involved, the intention of this standard is to completely specify only the serial data interface and the link protocol. Certain signals common to both the interface and the function of the device, such as device clocks and control interfaces, have application-dependent requirements. The JESD204 standard does not require a specific implementation of the control interface, however a serial interface is the recommended implementation. Devices may also have application-dependent modes, such as a low power / shutdown mode that will affect the interface. In these instances, the specification merely constrains other device properties as they relate to the interface, and leaves the specific implementation up to the designer.

Revision A of the standard was expanded to support serial data interfaces consisting of single or multiple lanes per converter device. In addition, converter functionality (ADC or DAC) can be distributed over multiple devices:

- All parallel running devices are implemented or specified to run synchronously with each other using the same data format.
- Normally this means that they are part of the same product family.

Revision B of the standard supports the following additional functions:

- Mechanism for achieving repeatable, programmable deterministic delay across the JESD204 link.
- Support for serial data rates up to 12.5 Gbps.
- Transition from using frame clock as the main clock source to using device clock as the main clock source. Device clock frequency requirements offer much more flexibility compared to requiring a frame clock input.

Revision C of the standard now supports the following additional functions:

- Data interfaces up to 32.45 Gbps.
- Three link layers – 64B/66B, 64B/80B, and 8B/10B. The 8B/10B link layer is similar to the link layer defined in JESD204B.

1 Scope (cont'd)

Figure 2 compares the scope of the original JESD204 specification and its revisions. Although not illustrated in the figure, it is possible to apply multiple, independent instances of the JESD204 standard to the same device. The logic device (e.g., ASIC or FPGA) is always assumed to be a single device.

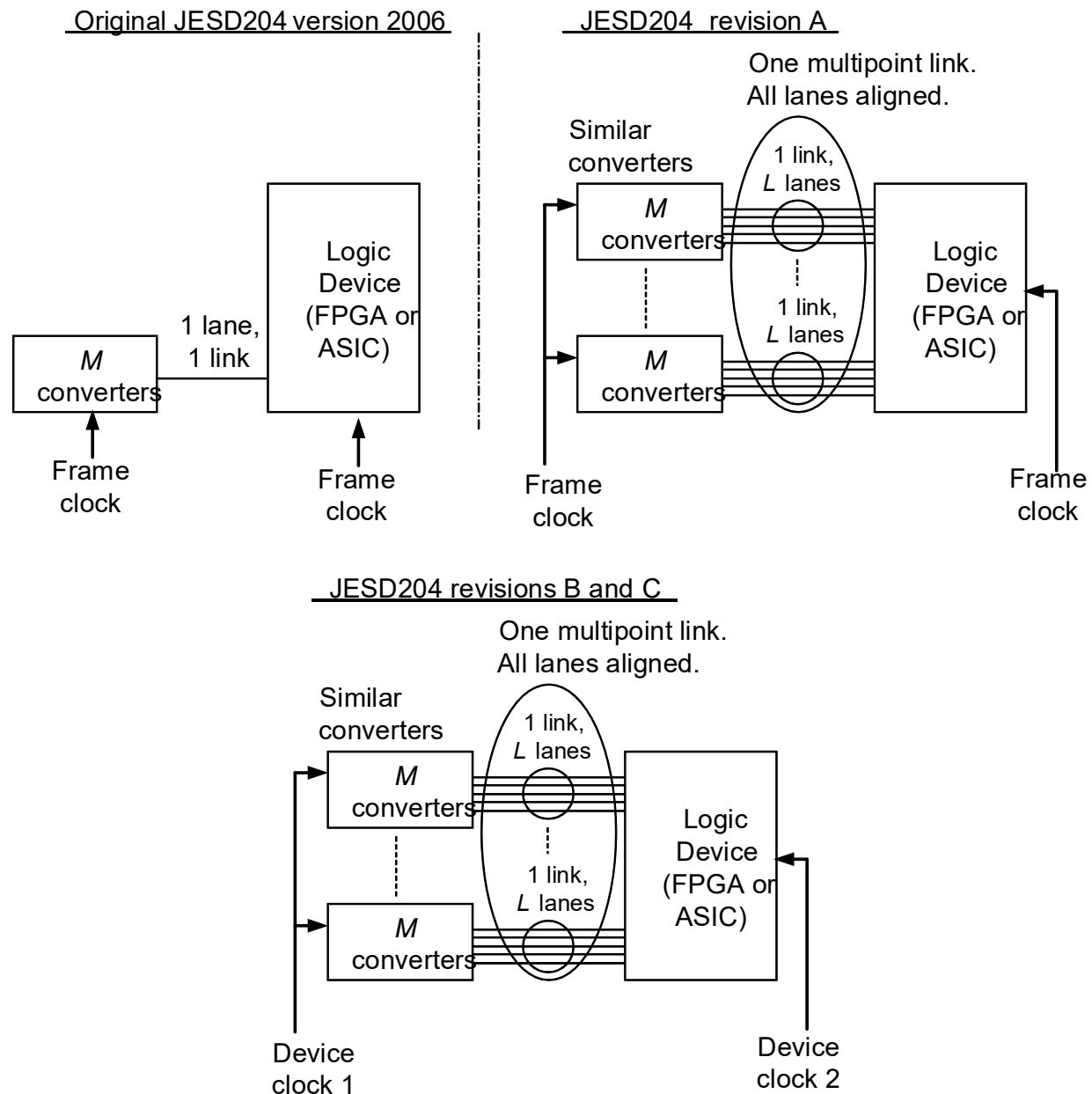


Figure 2 — Scope of original JESD204 and revisions A, B, and C

2 Normative references

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

1. JEDEC JESD99, Terms, Definitions, and Letter Symbols for Microelectronic Devices.
2. IEEE Standard for Ethernet, IEEE Std. 802.3™-2018 section 3, clause 36, *Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X*.
https://standards.ieee.org/standard/802_3-2018.html.
3. IEEE Standard for Ethernet, IEEE Std. 802.3™-2018 section 4, annex 48A, *Jitter test patterns*.
https://standards.ieee.org/standard/802_3-2018.html.
4. OIF-SxI-5-01.0, System Interface Level 5 (SxI-5): Common Electrical Characteristics for 2.488 – 3.125 Gbps Parallel Interfaces, Optical Internetworking Forum, October 2002.
<http://www.oiforum.com/wp-content/uploads/OIF-SxI5-01.0.pdf>.
5. OIF-CEI-04.0, Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps and 25G+ bps I/O, Optical Internetworking Forum, February 18, 2017
http://www.oiforum.com/wp-content/uploads/OIF_CEI_04.0.pdf.
6. INCITS TR-35-2004 (R2009), Fibre Channel - Methodologies for Jitter and Signal Quality Specification (FC-MJSQ), available from <http://webstore.ansi.org>.
7. INCITS 450-2009, *Information technology - Fibre Channel - Physical Interface - 4 (FC-PI-4)*, Annex F, *Scrambled test patterns*. Available from <http://webstore.ansi.org>.
8. INCITS TR-46-2011, *Information technology - Fibre Channel - Methodologies for Signal Quality Specification (FC-MSQS)*, clause 9, *Test patterns*. Available from <http://webstore.ansi.org>.

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3 Terminology

For the purposes of this standard, the terms and definitions given in JESD204, JESD99 (reference 1), and the following apply:

3.1 Terms and definitions

8B/10B: A DC-balanced octet-oriented data encoding sequence (see IEEE Std. 802.3 [5].)

64B/66B: An encoding type consisting of 64 unaltered user data bits concatenated with a 2-bit sync header (see 0).

64B/80B: An encoding type consisting of 64 unaltered user data bits concatenated with a 2-bit sync header and 14 fill bits (see 0.)

active edge of a clock: The clock edge on which the logic changes state.

NOTE 1 The active edge can be the rising edge, the falling edge, or both.

NOTE 2 The drawings in this standard show the rising edge as active edge.

ADC device: A device containing one or more analog-to-digital converters connected to the JESD204 link.

ADC link: A link from an ADC device to a logic device.

analog-to-digital converter: A functional block converting an analog signal to a digital sampled data stream. If the analog signal is converted to a complex data stream, the ADC is defined as the subblock generating either the real or the imaginary component of the data stream.

BERT: Bit Error Ratio Test or Tester (ref. OIF-CEI-04.0.)

block (64B/80B): A structure starting with a 2-bit sync header containing 80 bits total.

block (64B/66B or 64B/80B): A structure starting with a 2-bit sync header containing either 66 or 80 bits total.

CDR: Clock Data Recovery (ref. OIF-CEI-04.0.)

ceil(x): The smallest integer greater than or equal to x.

character: A symbol produced by 8B/10B encoding of an octet.

NOTE 1 While all octets can be encoded as data characters, certain octets can also be encoded as control characters.

NOTE 2 The same character may exist as two different code groups, depending on running disparity.

3.1 Terms and definitions (cont'd)

clock generator: A circuit used to generate synchronous, phase aligned device clocks to various devices in the JESD204 system.

NOTE A clock generator circuit can include one or more clock generator devices, but they must use a common source clock.

code group: A set of ten bits that, when representing data, conveys an octet (applies to 8B/10B encoding, see IEEE Std. 802.3 [5].)

command channel: Data stream using extra bandwidth afforded from sync headers (see 7.3.7.)

control interface: An application-specific interface used to pass information (usually status and control information) between a converter device and a logic device and/or between a device and a higher layer application level.

NOTE The JESD204 specification does not require a specific implementation of the control interface, however a serial interface is the recommended implementation.

converter: An analog-to-digital converter (ADC) or digital-to-analog converter (DAC).

NOTE In this standard, a converter is assumed to interface via a single stream of digital samples.

converter device: A component package containing one or more converters.

NOTE This standard specifies the interactions between one logic device and one or more converter devices.

DAC device: A device containing one or more digital-to-analog converters connected to the JESD204 link.

DAC link: A link from a DAC device to a logic device.

data link: An assembly that is controlled by a link protocol enabling data to be transferred from a data source to a data sink and consists of parts of two devices and the interconnecting data circuit, that is (“terminal” replaced by “device” in Ref. ATIS Telecom Glossary [1].)

data rate: speed at which data is transferred measured in bits per second, denoted by the symbol f_b .

descrambler: The inverse of a scrambler. (Ref. ATIS Telecom Glossary [1].)

NOTE The descrambler output is a signal restored to the state that it had when it entered the associated scrambler, provided that no errors have occurred.

device clock: A main clock signal from which a device must generate its local clocks.

digital-to-analog converter: A circuit converting a digital sampled data stream to an analog signal. If the analog signal is converted from a complex data stream, the DAC is defined as the subblock accepting either the real or the imaginary component of the data stream.

EMB_LOCK: A state asserting that extended multiblock alignment has been achieved.

extended multiblock: A set of data containing one or more multiblocks.

fill bit: A bit used to artificially extend the block size in 64B/80B encoding mode.

3.1 Terms and definitions (cont'd)

floor(x): The greatest integer less than or equal to x.

frame: A set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal (adapted from Ref. ATIS Telecom Glossary.)

frame clock: A signal used for sequencing frames or monitoring their alignment.

NOTE A physical frame clock is not required in this version of this standard, but may be required in the implementation of previous versions.

idle mode: An operating mode used for a converter that is not currently sampling data.

invalid code group: A code group that is not found in the proper column of the 8B/10B decoding tables, according to the current running disparity (see IEEE Std. 802.3 [5].)

lane: A differential signal pair for data transmission in one direction.

link: Synonym for “data link”.

local clock: A clock derived inside a device from the device clock and used in the implementation of the JESD204 link within the device.

NOTE 1 It is possible to align a local clock to an external signal, e.g., SYSREF.

NOTE 2 An internal copy of the device clock is not a local clock.

logic device: A component package containing exclusively or primarily digital logic; e.g., an ASIC or FPGA.

NOTE This standard specifies the interactions between one logic device and one or more converter devices.

max(x, y): The largest of x and y.

MB: Multiblock.

medium: The transmission path along which a signal propagates.

min(x, y): The smallest of x and y.

mod(x, y): The remainder after dividing x by y (x modulo y).

multiblock: A set of data containing 32 64B/66B or 64B/80B blocks.

3.1 Terms and definitions (cont'd)

multiframe: A set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal (ref. ATIS Telecom Glossary [1].) Applicable to the 8B/10B encoding option (see 0.)

NOTE 1 The multiframe alignment signal does not necessarily occur in each multiframe.

NOTE 2 In JESD204, a multiframe consists of K frames and is transmitted over a single lane.

multiframe clock: A signal used for sequencing multiframe or monitoring their alignment. Applicable to the 8B/10B encoding option (see 0.)

multipoint link: A data communications link that interconnects three or more devices (“terminal” replaced by “device” in Ref. ATIS Telecom Glossary [1].)

nibble: A group of four data bits (ref. IEEE 802.3 [3].)

normal operation: Operation of a link for the purpose of transmitting converter samples. That is, not a test mode or a power down mode.

octet: A group of eight adjacent binary digits (similar to a byte.)

receiver: A circuit attached to a lane for reconstructing a serial bit stream into time-aligned frames.

NOTE A receiver consists of one physical layer block and one link layer block.

receiver block: The combination of the receiver transport layer and all receiver link layer and physical layer blocks connected to a link.

receiver device: A component package containing one or more receiver blocks.

relative wander: Components of wander that are uncorrelated between any two in band signals (ref. OIF-CEI-04.0.)

rising edge of a differential signal(P,N): The simultaneous transitions that occur when signal(P) changes from the low logic level to the high logic level and signal(N) changes from the high logic level to the low logic level.

running disparity: A binary parameter having a value of + or –, representing the imbalance between the number of ones and zeros in a sequence of 8B/10B code-groups (see IEEE Std. 802.3 [5].)

sample: The instantaneous value of a signal measured or determined at a discrete time (adapted from ASIS Telecom Glossary, “sampled data” [1].)

NOTE In the context of JESD204, a sample is always the digital representation of a signal.

scrambler: A randomizing mechanism that is used to eliminate long strings of consecutive identical transmitted symbols and avoid the presence of spectral lines in the signal spectrum without changing the signaling rate (ref. IEEE 802.3 [3].)

3.1 Terms and definitions (cont'd)

SH_LOCK: A state that asserts the sync header alignment has been achieved.

skew: The magnitude of the time difference between two events that ideally would occur simultaneously (ref. JESD65B.)

steady-state voltage: The voltage at the transmitter output or receiver input resulting from the transmission of a series of consecutive logic-ones or logic-zeros, after the initial transient part of the waveform and any transmit filter compensation, have ended.

source clock: An oscillator from which the various other clock signals are derived. This oscillator is typically a VCO inside a clock generator device, or an external VCO within a clock generator circuit.

symbol: The smallest unit of coded data on the medium (simplified from IEEE 802.3 [3].)

NOTE In this standard used as synonym to “character”.

sync header: Two bits, which guarantee a transition, preceding every block in the 64B/66B and 64/80B link layer (see 0.)

sync word: A group of 32 encoded sync transitions in the 64B/66B and 64/80B link layer (see 0.)

SYSREF: A periodic, one-shot (strobe-type), or “gapped” periodic signal used to align the boundaries of local clocks in Subclass 1 devices. SYSREF must be source synchronous with the device clock.

transition time: Collective name given to the rise and fall time of a signal.

transmitter: A circuit that serializes the input frames and transports the resulting bit stream across a lane.

NOTE A transmitter consists of one link layer block and one physical layer block.

transmitter block: The combination of the transmitter transport layer and all transmitter link layer and physical layer blocks connected to a link.

transmitter device: A component package containing one or more transmitter blocks.

valid code group: A code group that is found in the proper column of the 8B/10B decoding tables, according to the current running disparity (see IEEE Std. 802.3 [5].)

word: A character string or a binary element string that it is convenient to consider as an entity.

3.2 Symbols and abbreviated terms

AC: Alternating Current.

ADC: Analog-to-Digital Converter.

A_{DD} : Dual-Dirac jitter added to received signal after the decision feedback equalizer (see Table 27, Table 28 and Table 29).

A_{fe} : Far-end aggressor transmitter peak differential output voltage (see Table 27, Table 28 and Table 29).

A_{ne} : Near-end aggressor transmitter peak differential output voltage voltage (see Table 27, Table 28 and Table 29).

ASIC: Application-Specific Integrated Circuit.

A_v : Transmitter differential output voltage voltage (see Table 27, Table 28 and Table 29).

BER: Bit Error Rate – The rate at which errors occur, in errors per number of bits transmitted.

BERT: Bit Error Rate Tester.

BGA: Ball Grid Array.

BkW : Block Width – The number of bits in a 64B/66B or 64B/80B block.

B-3: A class of devices that support data rates up to 3.125 Gbps.

B-6: A class of devices that support data rates up to 6.375 Gbps.

B-12: A class of devices that support data rates up to 12.5 Gbps.

$b_{max}[j]$: Normalized maximum decision feedback equalizer coefficient magnitude voltage (see Table 27, Table 28 and Table 29).

$b(n)$: Normalized magnitude of n^{th} decision feedback equalizer coefficient magnitude voltage (see Table 27, Table 28 and Table 29)

C: Control bit (used in figures, applies to the transport layer specification.)

CBHPJ: Correlated Bounded High-Probability Jitter.

CF: Number of control words per frame clock period per link.

CGS: Code Group Synchronization.

Cmd: Command – as related to the command channel.

COM: Channel Operating Margin (see IEEE Std. 802.3-2018.)

Cr: Converter (used in figures, applies to the transport layer specification.)

3.2 Symbols and abbreviated terms (cont'd)

CRC: Cyclic Redundancy Check.

CS: Number of control bits per conversion sample.

CTLE: Continuous Time Linear Equalizer.

C-S: A class of devices that support data rates up to 32.45 Gbps, with a short-reach channel.

C-M: A class of devices that support data rates up to 32.45 Gbps, with a medium-reach channel.

C-R: A class of devices that support data rates up to 32.45 Gbps, with a reflective channel.

$c(-1)$: Normalized value of the pre-cursor (bit before current bit) coefficient in the functional model for the feed-forward transmitter equalizer voltage (see Table 27, Table 28 and Table 29).

$c(0)$: Normalized value of the cursor (current bit) coefficient in the functional model for the feed-forward transmitter voltage (see Table 27, Table 28 and Table 29).

$c(+1)$: Normalized value of the post-cursor (bit after current bit) coefficient in the functional model for the feed-forward transmitter equalizer voltage (see Table 27, Table 28 and Table 29)

D: Dx.y, any 8B10B data symbol (used in figures, applies to the 8B/10B link layer specification.)

DAC: Digital-to-Analog Converter.

DC: Direct Current.

DCD: Duty Cycle Distortion.

DER_0 : Target detector (bit) error rate; used in COM.

DFE: Decision Feedback Equalizer.

D_p : Differential steady-state transmitter output voltage linear fit pulse delay.

D_w : Differential steady-state transmitter output voltage linear fit equalizer delay.

E: The number of multiblocks in an extended multiblock.

EBUJ: Effective Bounded Uncorrelated Jitter.

DA: Electronic Design Automation.

EMB: Extended Multiblock.

EoMB: End-of-multiblock sequence (00001).

EoEMB: End of extended multiblock identifier bit.

ERJ: Effective Random Jitter.

3.2 Symbols and abbreviated terms (cont'd)

F (as symbol): Number of octets per frame on a single lane.

FEC: Forward error correction.

FEXT: Far-End cross Talk.

FFE: Feed Forward Equalizer.

FIR: Finite Impulse Response.

FOM: Figure of Merit.

f_b : (1) Used data rate.

(2) Data rate at which a device, channel or system is compliance tested.

f_{min} : Start frequency of COM voltage (see Table 27, Table 28 and Table 29).

f_r : Receiver 3 dB bandwidth voltage (see Table 27, Table 28 and Table 29).

GJ: Gaussian Jitter.

g_{DC} : Continuous time filter, CTLE, DC gain voltage (see Table 27, Table 28 and Table 29).

HD: High Density user data format.

$H(z)$: Transmitter feed-forward equalizer discrete-time transfer function.

IBIS-AMI: Input/output Buffer Information Specification Algorithmic Modeling Interface (see Annex P reference 10.)

IFT: Inverse Fourier transform.

IL: Insertion Loss.

ILAS: Initial Lane Alignment Sequence. Applies to 8B/10B encoding.

$ILD(f)$: Insertion Loss Deviation as a function of frequency (see Annex F.2.)

ISI: Inter-Symbol Interference.

K (as symbol): (1) Number of frames per multiframe. Applies to the 8B/10B link layer, see 8.4.5.2.

(2) Number of frames per extended multiblock. Applies to the 64B/66B and 64B/80B link layers, see 7.1.4.

NOTE In the 8B/10B link layer, K is an independent design parameter. In the 64B/66B and 64B/80B link layers, K is dependent on E and F : $K = 256 \cdot E/F$.

3.2 Symbols and abbreviated terms (cont'd)

L: (1) Number of lanes per converter device.

(2) Number of signal levels (see Table 27, Table 28 and Table 29).

LCM: Lowest Common Multiple.

LEMC: Local Extended Multiblock Clock.

LFSR: Linear Feedback Shift Register.

LMFC: Local Multi Frame Clock.

M: (1) Number of converters per device (as used in the transport layer.)

(2) Number of samples per unit interval; used in COM.

mod: Modulo. $x \bmod y$ is used as alternative notation for $\text{mod}(x, y)$.

N: Converter resolution (as used in the transport layer.)

N_b: Number of taps of the receiver decision feedback equalizer (see Table 27, Table 28 and Table 29).

N_{max}: Number of samples of the sampled pulse response.

NEXT: Near-End crosstalk.

NG: Nibble Group.

N_p: Differential steady-state transmitter output voltage linear fit pulse length.

NRZ: Non-Return-to-Zero.

N_w: Differential steady-state transmitter output voltage linear fit equalizer length.

N': Total number of bits per sample in the user data format.

n: (1) Coefficient index in a decision feedback equalizer (see Table 27, Table 28 and Table 29). $0 \leq n \leq N_b$.

PCB: Printer Circuit Board.

PCS: Physical Coding Sublayer.

PMA: Physical Medium Attachment Sublayer.

PRBS: Pseudo-Random Bit Sequence.

PSFEXT(f): Far-end crosstalk power sum.

PSNEXT(f): Near-end crosstalk power sum.

3.2 Symbols and abbreviated terms (cont'd)

PVT: A term denoting the variations of a device across process corner, supply voltage, and temperature.

p_{max} : Peak value of the linear fit to the differential steady-state transmitter output.

NOTE Depending on the context, $p(k)$ applies specifically to the case that the ‘cursor’ TX equalizer coefficient is set to its maximum value and the other equalizer coefficients are zero, or to any configuration of the transmit equalizer.

p.u.l.: per unit length

RBD: Receive Buffer Delay.

RD: Running Disparity. Applies to 8B/10B encoding (see IEEE Std. 802.3 [5].)

RL: Return loss.

$RL_{CD}(f)$: Differential-to-common-mode return loss, i.e. the ratio between differential-mode incident power and common-mode reflected power.

$RL_{CM}(f)$: Common-mode return loss, i.e. the ratio between common-mode incident power and common-mode reflected power.

$RL_{DD}(f)$: Differential-mode return loss, i.e. the ratio between differential-mode incident power and differential-mode reflected power.

$RL_{RXF_{ref}}(f, f_b)$: Reference differential return loss of the receiver test fixture as a function of frequency for a specified data rate (see 5.2.4.2.)

$RL_{TXF_{ref}}(f, f_b)$: Reference differential return loss of the transmitter test fixture as a function of frequency for a specified data rate (see 5.2.3.2.)

RMS: Root Mean Square.

R_o : Reference single-ended resistance of COM (see Table 27, Table 28 and Table 29).

RX: Receiver.

S: Number of samples transmitted per single converter per frame cycle.

SERDES: Serializer/Deserializer.

SH: Sync Header.

SJ_{LF} : Low-frequency sinusoidal jitter to be tolerated by a compliant receiver.

SJ_{LH} : High-frequency sinusoidal jitter to be tolerated by a compliant receiver.

$SL_{<p>}$: Transmitter or receiver differential pair positive terminal voltage.

$SL_{<n>}$: Transmitter or receiver differential pair negative terminal voltage.

3.2 Symbols and abbreviated terms (cont'd)

SNDR: Signal-to-Noise-and-Distortion Ratio.

SNR: Signal-to-Noise Ratio.

SNR_{TX}: Transmitter signal-to-noise ratio (see Table 27, Table 28 and Table 29).

SSPS-64: Short Stress Pattern SDH64 (see OIF-CEI-04.0.)

T: Tail bit (applies to the transport layer specification.)

TJ: Total jitter.

T_{LLC}: The duration of one cycle of the link layer clock.

T_{SYNCLK}: The duration of one cycle of the SYNC~ generation or detection clock.

T_{TLC}: The duration of one cycle of the transport layer clock.

TUJ: Effective Total Uncorrelated Jitter.

TX: Transmitter.

UBHPJ: Uncorrelated Bounded High-Probability Jitter.

UI: Unit Interval = the duration of a serial bit.

U_k: Number of laminate package lengths of the reference model.

U_{LLC}: The maximum expected number of unit intervals (serial bit durations) in one cycle of the link layer clock.

U_{TLC}: The maximum expected number of unit intervals (serial bit durations) in one cycle of the transport layer clock.

v_{cm}: Common-mode voltage, i.e. the average of the voltages at the “true” (or positive) and “complement” (or negative) input or output terminals of a circuit.

v_d: Differential voltage, i.e. the voltage between the “true” (or positive) and “complement” (or negative) input or output terminals of a circuit.

v_f: Differential zero-to-peak voltage at the transmitter test/measurement point resulting from the transmission of a series of consecutive logic-ones, after the initial transient part of the waveform has ended, when the transmit equalizer “cursor” (current bit) coefficient has been set to its maximum value and all other pre- and post-cursor equalizer coefficients have been nulled.

Δf: Maximum frequency step in (see Table 27, Table 28 and Table 29).

η_o: One-sided noise spectral density of reference receiver model (see Table 27, Table 28 and Table 29).

3.2 Symbols and abbreviated terms (cont'd)

σ_{RJ} : Random jitter added to received signal after the decision feedback equalizer (see Table 27, Table 28 and Table 29).

/A/: K28.3 character, lane align. Applies to 8B/10B encoding.

/D_{x,y}/: Data code group D_{x,y} encoded according to the current running disparity (see IEEE Std. 802.3 [5].)

/F/ (as abbreviation): K28.7 character, frame sync. Applies to 8B/10B encoding.

/K/ (as abbreviation): K28.5 character, code group synchronization. Applies to 8B/10B encoding.

/K_{x,y}/: Control code group K_{x,y} encoded according to the current running disparity (see IEEE Std. 802.3 [5].)

/R/: K28.0 character. Applies to 8B/10B encoding.

4 Introduction and common requirements

4.1 Application overview

4.1.1 Background

In many data converter applications, a side effect of advances in converter technology is that device packages, power consumption and circuit board area are now driven by interconnect and data transfer requirements, instead of the intrinsic needs of the application. High resolution data converters typically need more board space for the interconnection (board traces and vias) than for the chip package itself. Single-ended digital interfaces cause switching noise, which affects the performance of the analog part, and parallel differential-signaling interfaces (such as LVDS) exacerbate the board area cost of the interconnect.

While technological advances have led to significantly lower power consumption in the intrinsic part of converters, similar reductions in the I/O power consumption and the size of the chip package have not taken place because of the large number of I/O lines needed. These problems become even more evident when multiple converters are integrated in the same package, e.g., for direct conversion radio transceivers. This I/O pin count limit also affects multi-channel data acquisition applications, such as beam forming, in which signal processors synthesize the output of an array of A/D converters into a single data stream.

Various approaches, such as integrating converters with signal processing logic or multi-chip modules, have addressed this problem but have drawbacks where converter performance is critical. The optimal processes for the converter function and digital VLSI are different. Integrating the two can impose performance limits on mixed-signal design, increases the risk of coupling digital switching noise into sensitive analog circuitry and can add cost to the digital design. Over multiple generations of a system design, requirements for the two areas evolve independently. From a practical standpoint, the two functions are typically supplied by different manufacturers. For many applications, then, the preferred configuration remains separate ADCs, DACs, and logic devices for driving the DAC devices and receiving data from the ADC devices.

Serialized differential links offer a solution in this case. Although such links have been widely adopted in data transfer applications, existing industry standards such as PCI Express provide services better suited to processors or dedicated interface devices. Such PC-centric interfaces impose unacceptable additional complexity and overhead on the simple, continuous, constant-bandwidth data stream considered here. What is needed is a definition of signals and data formats that enables front-end data acquisition systems to take advantage of high-speed serial links with minimal overhead.

The purpose of this specification is to allow manufacturers of converter devices (ADC devices and DAC devices) and logic devices (ASICs and FPGAs) to guarantee interoperability between devices, which will promote reuse of components across applications and enable system integrators to independently select the best device for each function. Implementation of this standard only requires logic blocks that are already commonly available to both FPGA and ASIC designers. Standard logic libraries, PLLs and SERDES macros are sufficient to implement this standard.

The intended application is one with short, point-to-point links between devices, either on the same printed circuit board, across one or more impedance-controlled connectors, or across short-reach cables. The electrical layer signal generally represents what is commercially referred to as Current Mode Logic or "CML", terminated at 1.2 V.

4.1.1 Background (cont'd)

The sampled converter data is sent over a serial data interface as a continuous, encoded data stream. The data interface consists of one or more lanes, i.e., pairs of differential signals. The collection of lanes and circuitry connecting two devices to each other is called a link. Several links connecting to the same logic device can be combined into a multipoint link on which all lanes are time-aligned.

4.1.2 Physical layer overview

JESD204C supports data rates for a single lane ranging from 0.3125 to 32.45 Gbps (raw bit rate), which supports a range of applications with varying requirements of converter resolution, sample rate, and number of channels. In multi-channel applications, several lower bandwidth channels are aggregated on a single link. In addition, the specification optionally supports links consisting of multiple lanes. Multiple lanes may be utilized when the converter data rate is higher than any single lane can accommodate or when lower rates are desired for reasons of simplicity or economy. Further, the specification optionally supports multiple data converters connected to the same logic device. Embedded alignment data enable the receiver(s) to realign associated information across multiple lanes and multiple links.

JESD204C defines two categories of classes, category B and category C. Three classes are defined within category B (B-3, B-6, and B-12), each with a different maximum data rate. Category C also contains three classes, however all of the category C classes have the same maximum data rate of 32.45 Gbps. Table 2 specifies the minimum and maximum data rate for each class.

Table 1 — Data rate range for each data interface

Data interface class	Minimum data rate (Gbps)	Maximum data rate (Gbps)
B-3	0.3125	3.125
B-6	0.3125	6.375
B-12	6.375	12.5
Category C	6.375	32.45

Three category C classes are defined to minimize link power dissipation for a variety of channel types: C-S(hort), C-M(edium) and C-R(eflective), each class being a superset of the previous one. Table 3 describes the most important architecture differences between the classes. A device may implement one or more classes or operating modes and still be considered JESD204C compliant.

Table 2 — JESD204C 32.45 Gbps interface device class features

Class	Relative power	Transmit filter boost	Receive filter boost	Receiver DFE taps
C-S	Low	9.5dB	6dB	0
C-M	Medium	9.5dB	9dB	3
C-R	High	9.5dB	12dB	14

JESD204C category C class interface compliance is assessed by calculating a figure of merit called channel operating margin or COM. A link's COM may be calculated using the JESD204C channel operating margin (JCOM) reference implementation tool, which is derived from the IEEE802.3 channel operating margin tool. A JESD204 compliant link is one that has a COM higher than 2dB. Subsuming channel compliance to an overall link compliance using JCOM affords greater flexibility in managing the trade-offs of channel impairments and SERDES architectural complexity.

4.1.3 Transport and link layer overview

4.1.3.1 Data encoding and organization

JESD204C provides three encoding options, which are listed in Table 4. For the four ranges of data rates shown in the table, each link layer is either required, recommended, optional, or not recommended. For example, 64B/66B encoding is recommended (but not required) between 6.375 and 12.5 Gbps, and required above 12.5 Gbps. 8B/10B encoding may not be optimal when paired with decision feedback equalizers (DFEs) as it may not provide adequate spectral richness required for successful DFE adaptation. For this reason, as well as the relative power efficiency of 64B/66B encoding, 8B/10B encoding is not recommended above 16 Gbps.

Table 3 — Supported link layers versus data rate

Data rate (DR) (Gbps)	8B/10B	64B/66B	64B/80B
DR ≤ 6.375	Required	Not Recommended	Not Recommended
6.375 < DR ≤ 12.5	Required	Recommended	Optional
12.5 < DR ≤ 16	Optional	Required	Optional
16 < DR ≤ 32	Not Recommended	Required	Optional

The 8B/10B link layer organizes the data into multiframes, which contain $K \cdot F$ octets. The 64B/66B and 64B/80B link layer organizes the data into multiblocks, which contain 32 blocks, with each block containing eight octets.

Data scrambling is optional when using 8B/10B encoding, however it is mandatory when using 64B/66B or 64B/80B encoding.

4.1.3.2 Clocking

The JESD204 standard specifies the use of a device clock. The device clock addresses a key problem of the system designer – the problem of having to transmit clocks of different frequencies to different devices in the system. Such transmission causes not only complications in the clock generation scheme but is also prone to spurious effects from sub-harmonic energies existing on the board. The ideal scenario for a system designer therefore would be to transmit clocks of identical frequencies to all the devices in the system. If the different devices in turn have provisions to generate their desired internal clocks from this main clock, it would vastly simplify the problem of system clocking. The device clocks transmitted to all the converter devices are expected to be identical, and may or may not be identical to the device clock transmitted to the logic device.

The sample clock may be internally generated from the device clock, of which a copy is provided to each device. Since most converter applications demand a low jitter sample clock to minimize noise, the device clock provided to the converter should have this desired low jitter. Also in low jitter applications, it would be desirable to generate the sample clock from the device clock through a simple process of clock division.

4.1.3.2 Clocking (cont'd)

The process of generating the internal clocks from the device clock may involve operations like clock division, which require a mechanism for phase synchronization across chips. As an example, multiple ADC devices interfacing to the same logic device might generate their internal sampling clocks based on a process of division – if the phase synchronization between these divided clocks is not established, it would result in a relative skew between the sampling instants of the different ADCs. In applications like beamforming for instance, such a relative skew would not be tolerable. The 8B/10B link layer offers a solution to this problem of phase synchronization by exploiting the existence of a Local Multiframe clock (LMFC). Similarly, the 64B/66B and 64B/80B link layer instead uses the LEMC (Local Extended Multiblock Clock). While the LMFC marks multiframe boundaries in the 8B/10B link layer, the LEMC is used to mark extended multiblock boundaries in the 64B/66B and 64B/80B link layer. The LEMC period spans multiple multiblocks, and should be chosen to be long enough to fit a whole number of frames and to allow for a certain amount of delay uncertainty on the lanes, the physical layers, and the link layers.

The 8B/10B link layer attempts to phase align the LMFCs between all the devices through two different means in two different subclasses, subclass 1 and subclass 2. However, the 64B/66B and 64B/80B link layer only supports subclass 1. In subclass 1, the LEMC/LMFCs are synchronized by a source synchronous signal called SYSREF, which is transmitted to all the devices with controlled timing. In subclass 2 (again, this is only supported when using the 8B/10B link layer), the logic device generates its LMFC through a process of division of its device clock. The logic device then communicates the phase of its LMFC to the converter devices, each of which adjust their LMFC phases with respect to the common logic main device so that clocks are in phase.

It is recommended that the pin configuration of a subclass 1 device would have the SYSREF pin in close proximity to the device clock pins. It is also recommended that the electrical characteristics of the SYSREF signal be identical to that of the device clock. While SYSREF is expected to be a much slower clock than the device clock, its rise/fall times are expected to be similar to that of the device clock. As a result, the signal integrity of the SYSREF signal might be as much of a concern as that of the device clock.

A related concern to be kept in mind while controlling the timing of the SYSREF signal relative to the device clock is the fact that SYSREF, by virtue of being a slow signal would have logic high and low voltage levels that would be close to the saturation levels. In comparison, a high speed device clock is more likely to have logic high and low voltage levels that are further away from the saturation levels. This can lead to a mismatch in the rise/ fall times of the SYSREF signal relative to the device clock, and therefore needs to be considered while analyzing the setup and hold times available for the device clock edge to latch the SYSREF. In a case where SYSREF is provided as a low frequency periodic signal, the data converter vendor as well as the system implementer would do well to analyze the spurious effects from having such a sub-harmonic clock, and minimize its effects on the converter and system performance.

4.1.3.3 Sync header stream

The 64B/66B and 64B/80B link layer define a sync header stream, which allows the transmission of information parallel to the user data. This information is encoded using the sync header portion of the 66B or 80B word block. Specifically, one sync header per block is decoded to a single bit, and 32 of these bits across a multiblock make up the 32-bit sync word. Four formats of the sync word are supported – one that supplies Forward Error Correction (FEC) parity information, two that supply Cyclic Redundancy Check (CRC) parity information along with a command channel, and one that only supplies the command channel. The command channel provides a mechanism for the transmitter to send various commands and data to the receiver.

4.1.3.4 Deterministic latency

Yet another key system issue that is addressed in the JESD204 standard is the problem of deterministic latency. In the context of multiple ADC devices interfacing to a common logic device, deterministic latency is simply the following – at a particular instant, the frames appearing at the final output of the receiver must be relatable to a specific sampling instant of each ADC. These sampling instants for each ADC must, within margins of aperture error, correspond to the same absolute time instant. This relation between the ADC sampling instants and the frame-based output at the receiver output must be maintained the same over temperature and supply voltage, across devices, and must be repeatable over power-up cycles. For the case of a logic device transmitter interfacing to multiple DAC devices, deterministic latency implies a known deterministic relation between the frames going into the logic device transmitter and the analog output transitions at the output of the multiple DAC devices. While the 8B/10B link layer utilizes the LMFC to achieve deterministic latency, the 64B/66B and 64B/80B link layer uses the LEMC to achieve deterministic latency. Please refer to clause 4.2 for further details on the implementation of deterministic latency.

4.1.4 Data link properties

With the 8B/10B link layer, JESD204 uses the SYNC interface for synchronization and error reporting. When using the 64B/66B or 64B/80B encoding options, sync headers within the encoded data are used for the synchronization process and the reporting of errors is left to the application-layer software.

With the 8B/10B link layer, the alignment between multiple converter devices happens through the alignment of their LMFCs as determined by SYSREF in subclass 1, and SYNC~ in subclass 2. With the 64B/66B and 64B/80B link layer, the alignment between multiple converter devices happens through the alignment of their LEMC as determined by SYSREF in subclass 1. Each converter device can then adjust its LEMC phase to match with the common LEMC of the logic device. Subclass 2 may still be used with the 8B/10B link layer.

When one or more converters inside a device are in power-down mode, the link can still be kept active and synchronized. This state is called idle mode. In idle mode, samples of inactive converters are replaced by dummy samples. On the link level, no difference can be seen between an active and an inactive converter. The presence of dummy samples is indicated to the receiver via the control interface or via dedicated control bits in the sample stream.

When all converters in a device are inactive for a long period of time, it may be advantageous for the link to enter a shut-down mode. Operation in shut-down mode is similar to the continuous mode, but with power-down and power-up procedures applied between the periods of activity. These power-down and power-up procedures are not part of the current specification and their implementation is left to the application.

4.1.4.1 Variants and modes

The interface supports a wide range of data converter devices over single and multiple serial links. In addition, each link may consist of a single lane or multiple lanes as needed to support the required data throughput. Each lane contains synchronization and alignment data that allows the data to be reassembled in the receiver, effectively rebuilding the structure of the original converter data. Although one or more converter devices are supported by this standard, only one logic device is supported.

The configuration variants can be classified according to the following scheme:

1. Single vs. multiple converters per converter device.
2. Single lane vs. multiple lanes per converter device.
3. Single converter device vs. multiple converter devices connected to one logic device.

The interface can work in one of the following modes:

4. Data mode vs. test mode.
5. Active mode vs. idle mode.

Test modes can be implemented on the physical layer level, e.g., by transmitting a PRBS pattern, on the link layer level, e.g., by transmitting a stream of synchronization characters, or on the transport layer level, by transmitting a stream of test samples. In the idle mode one or more converters in a device may be shut down and their samples are replaced by dummy samples.

4.1.5 Configuration examples

4.1.5.1 General

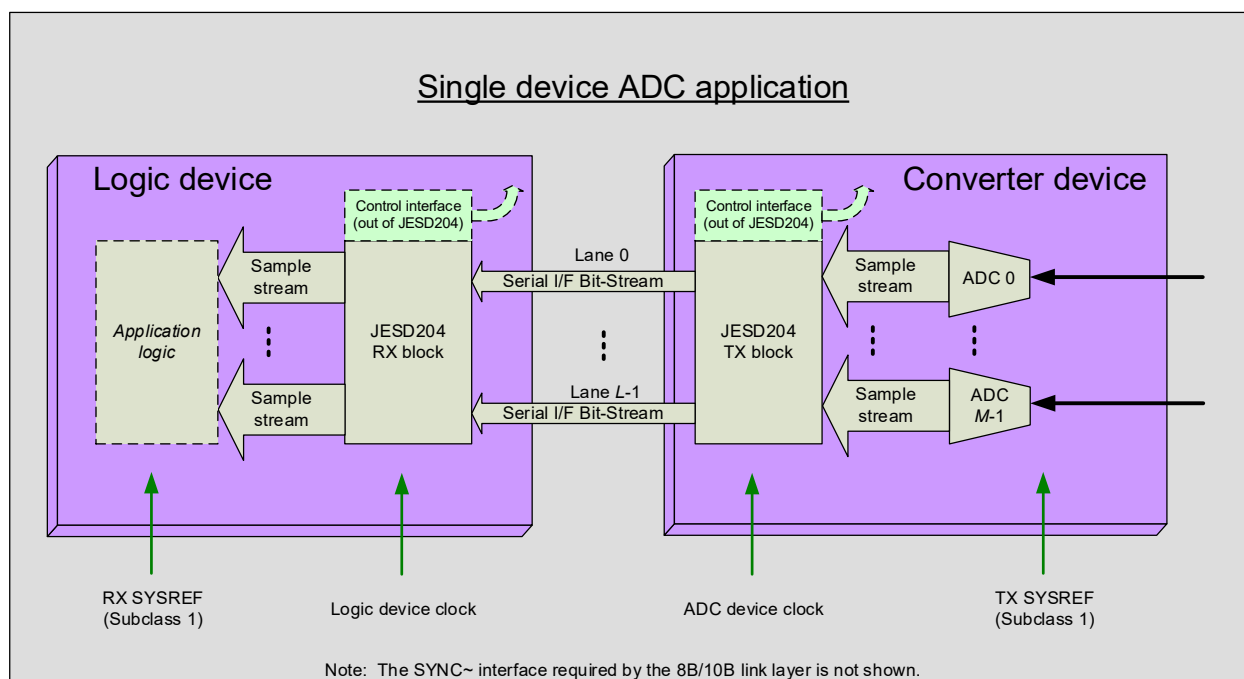
The following examples illustrate configurations for a single link, connecting a logic device to a single converter device. Configurations with multiple converter devices consist of multiple single links in parallel, which share the same logic device. Multiple links can be independent of each other, or they can use certain functionality to align their data streams, as described in clauses 4.2 and 4.3. While specified for data converters, the standard is also suitable for all systems that transmit real-time streaming data between devices. Therefore, the configurations outlined below provide a few examples of the many possibilities.

4.1.5.2 Single-device ADC application

Figure 3 illustrates a typical implementation of the interface as it applies to a single ADC device communicating with a single logic device. With this configuration, a single package contains one or more ADCs. As described earlier, the converters' output data is aggregated by the JESD204 TX block and is sent across one or more lanes to the receiving logic device.

The logic device de-serializes the data in the JESD204 RX block. If multiple lanes are involved, the logic device RX block is also responsible for ensuring alignment of the data streams being sent to the application logic.

In subclass 1, the zero-to-one transitions on the signals marked as TX SYSREF and RX SYSREF are sampled by the ADC Device clock and the Logic Device clock respectively, thereby synchronizing the LMFC/LEMC phase inside each of the devices.

4.1.5.2 Single-device ADC application (cont'd)**Figure 3 — Single device ADC application**

4.1.5.3 Single-device DAC application

Figure 4 shows an application using multiple DACs in a single package. In this application, the logic device provides DAC samples using one or more lanes. In the DAC device's JESD204 RX block, the data is de-serialized and provided to the DACs.

In subclass 1, the zero-to-one transitions on the signals marked as TX SYSREF and RX SYSREF are sampled by the logic device clock and the DAC device clock respectively, thereby synchronizing the LMFC phase inside each of the devices.

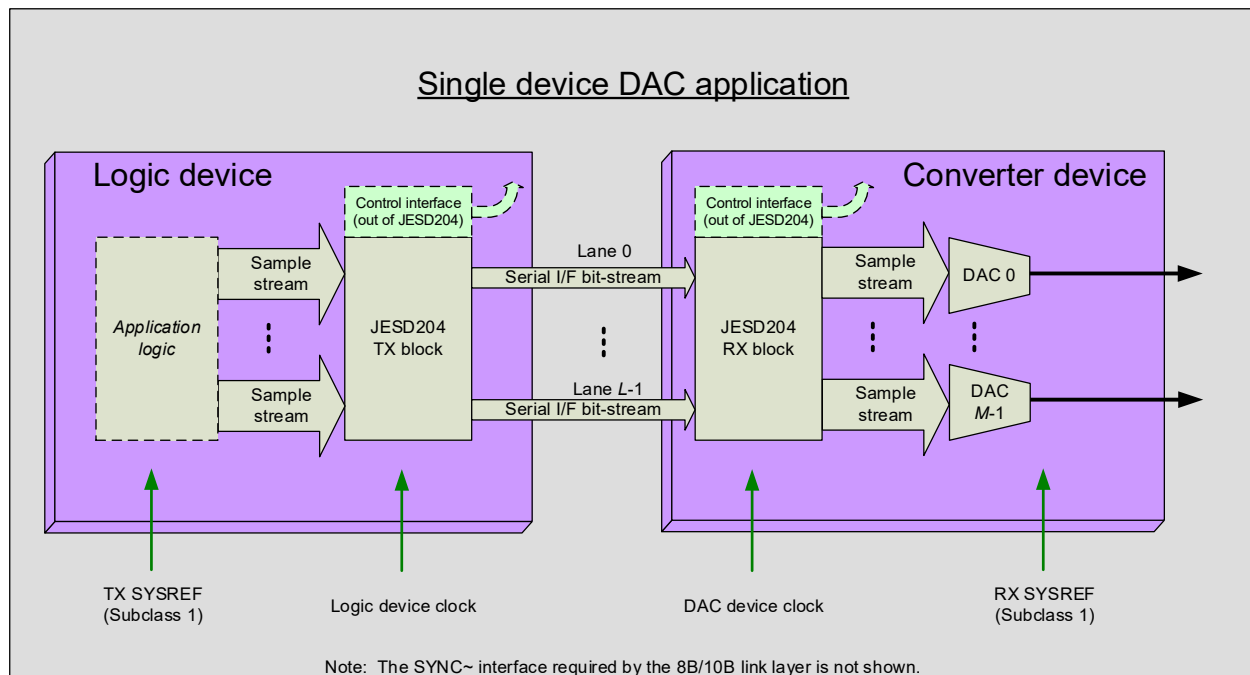


Figure 4 — Single device DAC application

4.2 Deterministic latency

4.2.1 Introduction and general requirements

Many JESD204 systems contain various data processing elements that are distributed across different clock domains and lead to ambiguous delays through the interface. These ambiguities lead to non-repeatable latencies across the link from power-up to power-up or over link-reestablishments. The JESD204 standard provides the option for what's called "deterministic latency" to avoid such ambiguity.

Deterministic latency across the link is defined from the parallel frame-based data input on the TX device to the parallel frame-based data output on the RX device. This latency across the link shall be repeatable from power-up cycle to power-up cycle and across link re-synchronization events, provided that the auxiliary timing signals meet the required specifications at the device inputs.

NOTE The frame-based input and output points for defining latency are at the interface between the transport layer and the application layer. Therefore, the implementation of the deterministic latency may partly or wholly take place in the transport layer or application layer.

The use of a local multiframe clock (LMFC) or local extended multiblock clock (LEMC) is required to achieve deterministic latency. The data in the TX and RX devices shall be aligned to the LMFC/LEMC in the following way:

In the TX device, the start of any multiframe or extended multiblock shall be initiated simultaneously across all lanes at a well-defined moment in time.

- The 'well-defined moment in time' for TX transmission is a deterministic period of time from all active LMFC/LEMC edges.

In the RX device, a buffer shall exist to hold all lane data for release (i.e., data allowed to propagate) simultaneously at a well-defined moment in time.

- The 'well-defined moment in time' for RX buffer release is a programmable number of steps after an active LMFC/LEMC edge. This programmable number of steps is referred to as the RX Buffer Delay (*RBD*).
- The full adjustment range of *RBD* shall cover the full size of the RX elastic buffer or at least one LMFC/LEMC cycle, whichever is smaller.
- The minimum size required for the RX elastic buffer corresponds to the maximum possible skew at skew point SP5 for the relevant subclass (see 4.3.8).
- The oldest data in the buffer available for release shall correspond to the start of a multiframe or extended multiblock.
- The *RBD* adjustment resolution shall not be greater than 255 steps.
- The *RBD* adjustment resolution shall be at least 16 steps. If more than one multiframe or multiblock per lane fits in the buffer, the *RBD* adjustment resolution shall be at least 16 steps per multiframe or multiblock.

4.2.1 Introduction and general requirements (cont'd)

The *RBD* adjustment is required to move the release of the elastic buffer away from any point in time that may lie within the range of lane data arrival skew (see example below). It must be possible, through the use of *RBD*, to select a release opportunity that does not lie in this range. Smaller and more numerous *RBD* adjustment steps are preferred to meet this requirement and to assist in selecting a release opportunity just after the latest possible lane arrival, which is useful to minimize total latency through the link. In order that the system implementer can select the optimum *RBD* value, the RX device shall be able to report over the control interface the arrival time of the multiframe or extended multiblock boundary relative to the active LMFC/LEMC edge for at least the slowest received lane.

The moments of generation of the multiframe or extended multiblock boundaries and release of the RX buffer mentioned above are related to the LMFC/LEMCs in the TX and RX devices. Thus, the achievement of deterministic latency with minimum uncertainty relies on achievement of a fixed offset between the LMFC/LEMCs within TX and RX devices. To achieve proper performance of the deterministic latency protocol while utilizing the 8B/10B link layer, the period of the LMFC must be larger than the maximum possible delay variation across any link or multipoint link. To achieve proper performance of the deterministic latency protocol while utilizing either the 64B/66B link layer or the 64B/80B link layer, the period of the LEMC must be larger than double the maximum possible delay variation across any link or multipoint link.

To achieve deterministic latency for JESD204 links, the RX device must be able to buffer the incoming data of all lanes until the RX elastic buffer can be released. To release the elastic buffer, data must be present that corresponds to the start of a multiframe or extended multiblock for all active lanes. The buffer must be released after an active LMFC/LEMC edge according to the *RBD* value.

The selection of the moment to release the buffers in a JESD204C system is illustrated in the timing diagram of Figure 5. As part of the initial lane alignment, the TX device transmits a stream of /K/ characters, followed by an initial lane alignment sequence (ILAS). In this example, ILAS starts exactly on an active LMFC edge. The RX device will then detect the start of ILAS on each lane, and will feed this data into per-lane elastic buffers. The 'release opportunity' of these buffers is set to *RBD* character durations after each active LMFC edge. On the first release opportunity after the RX device receives valid ILAS data on all lanes, it will release all the elastic store buffers. The resulting data output from the RX device is aligned with a fixed latency across the link.

4.2.1 Introduction and general requirements (cont'd)

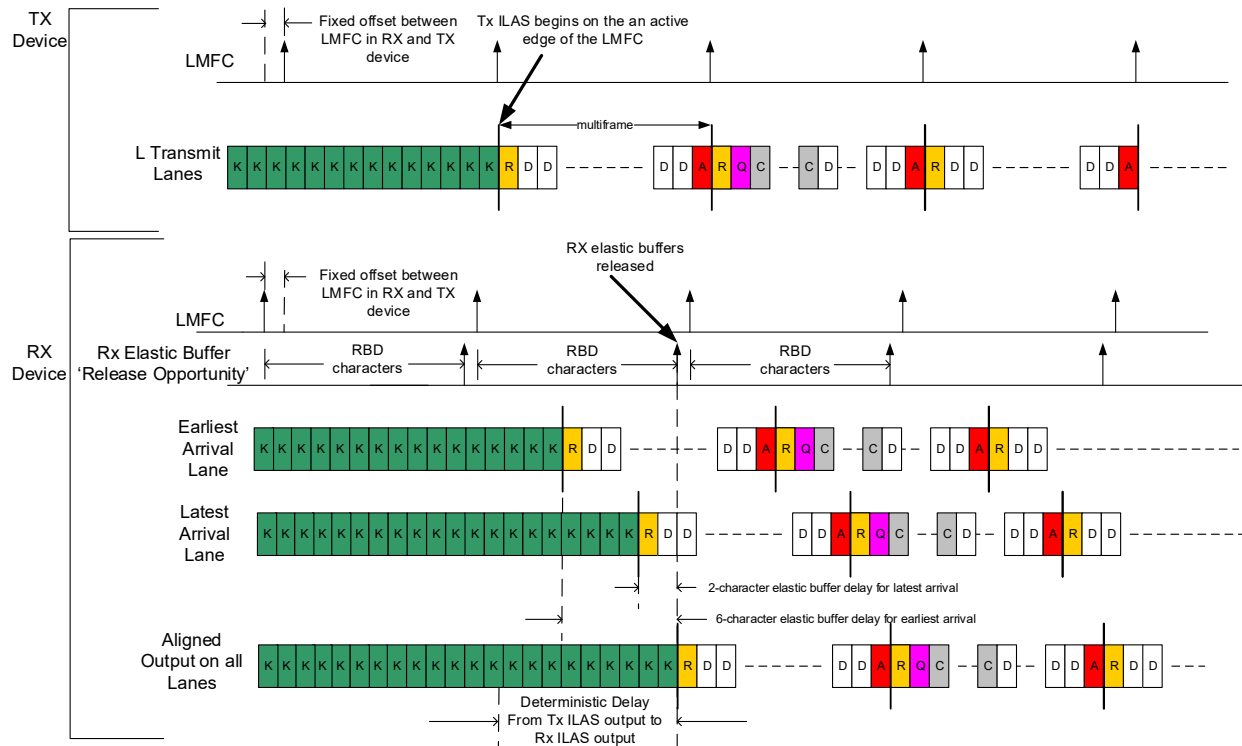


Figure 5 — Timing diagram illustrating the RX elastic buffer release opportunity in a JESD204C 8B/10B system

The selection of the *RBD* value should take into account margin for latency variations due to e.g., power reset or resynchronization of the link. The following might occur between two subsequent power-ups in the same system if this were not the case:

- 1) The start of a multiframe or extended multiblock on the slowest lane arrives at the Rx just soon enough for a particular release opportunity. In this case the data is released from the buffer with little delay.
- 2) The start of a multiframe or extended multiblock on the slowest lane arrives at the Rx just too late for a particular release opportunity. In this case the data is held for the next release opportunity and the buffer inserts close to a whole LMFC/LEMC period worth of delay.

Deterministic latency would not be preserved in the above example because the second instance would add exactly an LMFC/LEMC period worth of total link delay compared with the first instance.

4.2.2 No support for deterministic latency (device subclass 0 and device subclass 1 using MULTIREF)

In subclass 0 operation, the RX buffers are released at the earliest opportunity after the detection of a multiframe or extended multiblock boundary in each lane. Subclass 0 operation requires no alignment of LMFC/LEMCs across transmitter and receiver devices. Subclass 0 is intended for interfacing to JESD204A devices and for applications in which minimum link delay is desired, without need for deterministic latency.

In subclass 1 operation, the MULTIREF signal may be used to align the LMFC/LEMCs across converter devices (see 4.3.6). In this use case, the MULTIREF signal does not align the LMFC/LEMCs between the logic device and the converter devices. Therefore, this use case of the MULTIREF signal will not create deterministic latency. The MULTIREF signal replaces the lane-to-lane inter-device synchronization interface for subclass 0 DAC devices of the JESD204B standard as well as lane alignment across subclass 0 ADC devices using sync signal combination.

4.2.3 Deterministic latency using SYSREF (device subclass 1)

For subclass-1 devices, the creation of properly aligned LMFC/LEMC signals within TX and RX devices is achieved using a signal designated as ‘SYSREF’, which must be distributed to all converter and logic devices.

Delay uncertainty in the system is minimized by using highly accurate SYSREF / device clock signal pairs. While it is not mandatory, it is recommended that SYSREF be generated from the same device producing the TX and RX device clocks.

Due to the variety of allowable SYSREF signal types (periodic, one-shot (strobe-type), or “gapped” periodic), the variety of clock generator devices that may not support all the options for SYSREF generation, and to accommodate systems where SYSREF will be ‘turned off’ during normal operation, the following requirements for subclass-1 devices apply:

- RX and TX logic Devices shall have the ability to issue a ‘generate SYSREF’ request, which enables the clock generator (or other SYSREF generating device) to generate one or more SYSREF pulses to all devices in the system or at least those connected to the link.
- All TX and RX devices shall have the ability to determine whether or not to adjust the phase alignment of their LMFC/LEMCs based on the next detected SYSREF pulse. Implementation details for this function are left to the device implementer but three possible options are listed below:
 - Every SYSREF pulse may be examined by the device to determine if the existing phase alignment of the LMFC/LEMC requires adjustment.
 - A device may be instructed via device input pin or control interface command to use the next detected SYSREF pulse to force a phase alignment of the LMFC/LEMC.
 - A device may be instructed via device input pin or control interface command to ignore all future SYSREF pulses.

NOTE For subclass 1 devices, LMFC/LEMC phase realignment based on SYSREF will only be necessary in cases where a device is being initialized or where a link has exhibited a failure and wants to rule out LMFC/LEMC misalignment as a cause.

4.2.4 Deterministic latency using SYNC~ detection (device subclass 2)

Please refer to 8.5.

4.3 Physical timing

4.3.1 Device clock

The device clock is the external timing reference of each transmitter and receiver converter device in the JESD204 system. It is not mandatory that all devices share a common device clock. However, all device clocks in the system shall be phase locked to a common source, which is known as the source clock. The devices shall be able to generate and receive data at a constant rate derived from their device clock. Inside the devices, all internal clocks that influence the delay on the link shall be derived from the device clock.

The permitted relationships between the periods of the TX and RX device clock and the durations of data structures on the link depend on the JESD204 subclass as follows:

- Subclass 0: The permitted relationships between the device clock period and the duration of the frame, 8B/10B character, 64B/66B block or 64B/80B block shall be specified by the device implementer. The device implementer shall specify possible extra restrictions on the device clock period for backwards compatibility with JESD204A or JESD204B, if applicable.
- Subclass 1: The duration of the multiframe or extended multiblock shall be a whole number of device clock periods.
- Subclass 2 (8B/10B link layer only): The multiframe duration shall be a whole number of device clock periods. Additionally, the TX device clock period shall be a whole number of RX device clock periods, or the RX device clock period shall be a whole number of TX device clocks periods.

NOTE The above requirements for subclasses 1 and 2 are necessary, in order that the devices can align the LMFC or LEMC edges (see 4.3.4) to the device clock edges.

The electrical characteristics of the device clock signal are not specified in this document, because other considerations may determine these characteristics. It is expected that Low Voltage CMOS type electrical characteristics, as specified by such JEDEC standards as JESD8-5 (2.5 V) or JESD8-7 (1.8 V) would be used for this signal. Higher clock rates might demand the use of a differential signal format, such as LVPECL, LVDS or CML.

The device clock input's frequency and phase stability (jitter), however, have a direct bearing on the operation of this interface. For this reason, manufacturers shall specify the required jitter for the device clock.

Other circuitry in the transmitter or receiver device may require more restrictive jitter characteristics and may also have additional requirements such as duty cycle.

4.3.2 Link layer clock

In this standard, the link layer clock is defined as the clock that sequences the signal processing in the link layer and the parallel interface between the link layer and the physical layer. The skew budget is based on the following requirement for the duration T_{LLC} of one link layer clock cycle:

$$T_{LLC} \leq \begin{cases} 20 \text{ UI}, & f_b \leq 4 \text{ Gbps} \\ 40 \text{ UI}, & 4 \text{ GHz} < f_b \leq 8 \text{ Gbps} \\ 80 \text{ UI}, & f_b > 8 \text{ Gbps} \end{cases}$$

where f_b is the serial bit rate and UI is the duration of a serial bit.

JESD204 does not specify the device implementation. The device implementer may deviate from the above assumptions, but such a deviation shall not lead to a violation of the skew budget (see 4.3.8).

4.3.3 Transport layer clock

In this standard, the transport layer clock is defined as the clock that sequences the signal processing in the transport layer and the parallel interface between the transport layer and the link layer. The skew budget is based on the following requirement for the duration T_{TLC} of one transport layer clock cycle:

$$\text{For 8B/10B and 64B/80B encoding: } T_{TLC} \leq \begin{cases} 20 \text{ UI}, & f_b \leq 4 \text{ Gbps} \\ 40 \text{ UI}, & 4 \text{ GHz} < f_b \leq 8 \text{ Gbps} \\ 80 \text{ UI}, & f_b > 8 \text{ Gbps} \end{cases}$$

$$\text{For 64B/66B encoding: } T_{TLC} \leq 66 \text{ UI}$$

where f_b is the serial bit rate and UI is the duration of a serial bit.

JESD204 does not specify the device implementation. The device implementer may deviate from the above assumptions, but such a deviation may not lead to a violation of the skew budget (see 4.3.8).

4.3.4 Local multiframe and extended multiblock clocks (LMFC and LEMC)

The local multiframe clock (LMFC, used with 8B/10B encoded data) and the local extended multiblock clock (LEMC, used with 64B/66B and 64B/80B encoded data) are internal clocks used to align the boundaries of the multiframe or extended multiblocks between lanes and – in deterministic latency devices – to an external reference (SYSREF or MULTIREF in subclass 1 and SYNC~ in subclass 2). The use of an LMFC / LEMC is mandatory in subclasses 1 and 2 and optional in subclass 0.

NOTE Subclass 2 is only applicable to 8B/10B encoding.

The local multiframe / extended multiblock clocks in device subclasses 1 and 2 shall comply with the following requirements:

- The LMFC / LEMC period in all transmitter and receiver devices shall be identical.
- The LMFC / LEMC shall be derived from the device clock.
- At each side of the link, the LMFC / LEMC shall be common to all lanes of the link.
- In subclass 1 devices, there shall be a fixed or programmable offset between the rising or falling edge of the LMFC / LEMC and the device clock edge upon which the SYSREF / MULTIREF signal is detected as being active.
- Subclass 1 devices shall be able to measure the amount of device clock cycles by which the detected active edge of the SYSREF / MULTIREF signal deviates from its expected position and not to realign the LMFC / LEMC if the deviation from the expected position is less than a programmable number of device clock cycles.

If a device supports multiple JESD204 links, the above requirements are applied separately to each link.

4.3.5 SYSREF signal (device Subclass 1)

In Subclass 1 deterministic latency systems, a signal named SYSREF is distributed to all transmitter and receiver devices in the system. The purpose of SYSREF is to identify the device clock edge that shall be used to align the phase of the LMFC or LEMC.

SYSREF can be either a periodic, one-shot (strobe-type), or “gapped” periodic signal. It is an active high signal, which is sampled by the device clock. Devices shall be able to support sampling SYSREF on the device clock rising edge, but may optionally allow SYSREF to be sampled on the device clock falling edge.

For periodic or “gapped” periodic SYSREF signals, the period shall be an integer multiple of the LMFC or LEMC period. The phase of the LMFC or LEMC within a device shall be determined by the device clock sampling edge upon which the sampled SYSREF value has transitioned from “0” to “1”.

It is not mandatory that a common SYSREF signal is generated to all devices in the system. However, it is required that SYSREF signals be generated to all devices in a manner that ensures a deterministic relationship between the moments when SYSREF is sampled active by all devices in the system. A timing diagram illustrating this concept (using device clock rising edge to sample SYSREF) and showing simultaneous sampling of the active SYSREF signal at both devices is shown in Figure 6.

4.3.5 SYSREF signal (device Subclass 1) (cont'd)

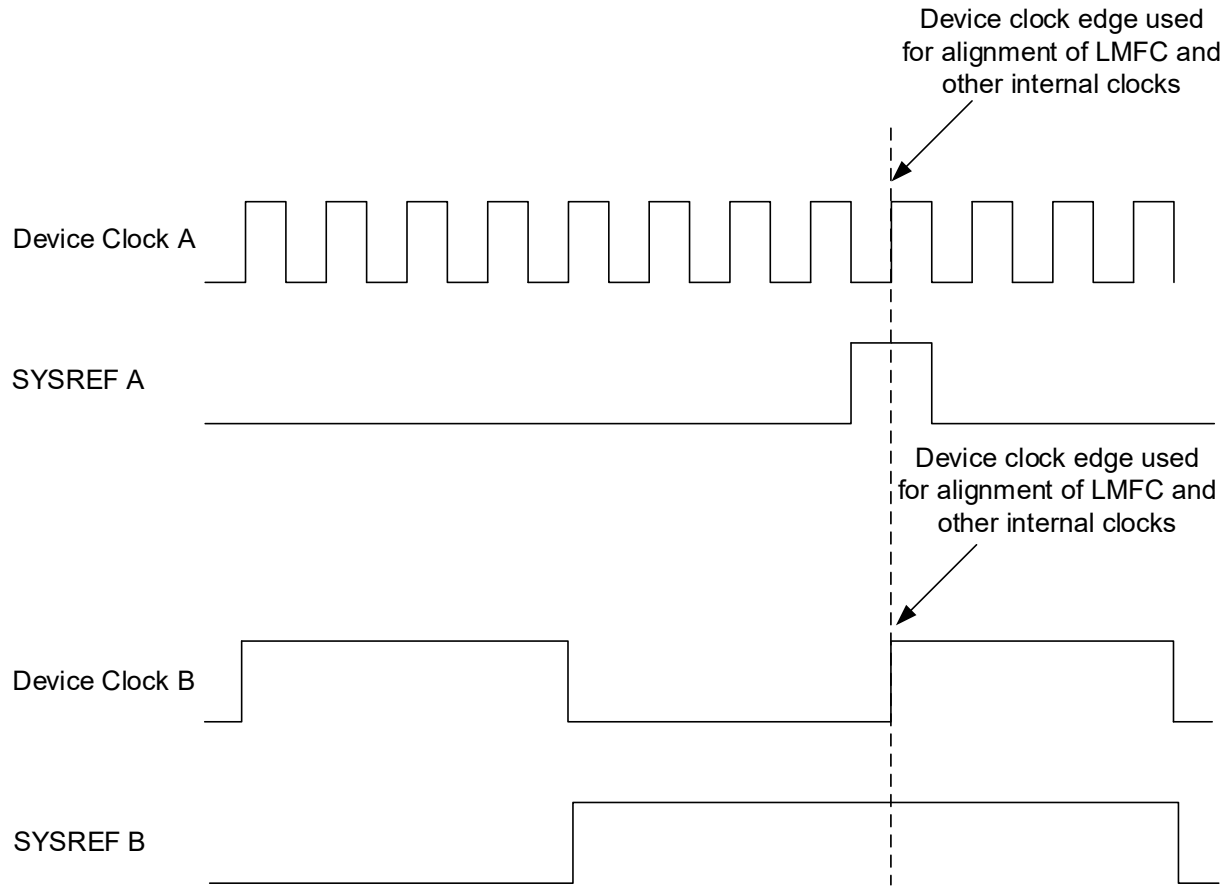


Figure 6 — SYSREF sampling illustration

Delay uncertainty across the link is caused by the uncertainty in phase alignment between the LMFCs / LEMCs in the TX and RX devices within the system. Minimizing delay uncertainty relies on the generation of the LMFC / LEMC in both the TX and RX to be governed by events that happen at the same time instant. For Subclass-1 devices, this time instant corresponds to the device clock cycle upon which a “0” to “1” transition on SYSREF is detected. Therefore, it is recommended that the system implementer follows these guidelines for minimizing phase alignment offset between TX and RX LMFCs / LEMCs.

1. The device clock and SYSREF signal to each device should be routed close to each other.
2. SYSREF (source synchronous to device clock) should be distributed within the system for maximum setup/hold compliance at the device receiver.
3. SYSREF should ideally have the timing relationship relative to the device clock as shown in Figure 7. However, with very high speed device clocks, it may not be possible to meet SYSREF setup/hold time requirements. The resulting amount of delay uncertainty across the link can be minimized by controlling the phase of the SYSREF signal relative to the setup/hold time requirements of the device that is sampling it.

It is strongly recommended to use the same type of signal type for SYSREF and the device clock, to maintain an accurate timing relationship.

4.3.5 SYSREF signal (device Subclass 1) (cont'd)

Figure 7 shows the critical timing specifications relating to the SYSREF signal. The values for these parameters are not specified here but the transmitter and receiver device specifications shall specify these values.

t_{SU_S} (min) and t_{H_S} (min): Setup and hold times of SYSREF with respect to device clock at the device SYSREF pin. Subclass-1 transmitter and receiver devices shall specify these parameters.

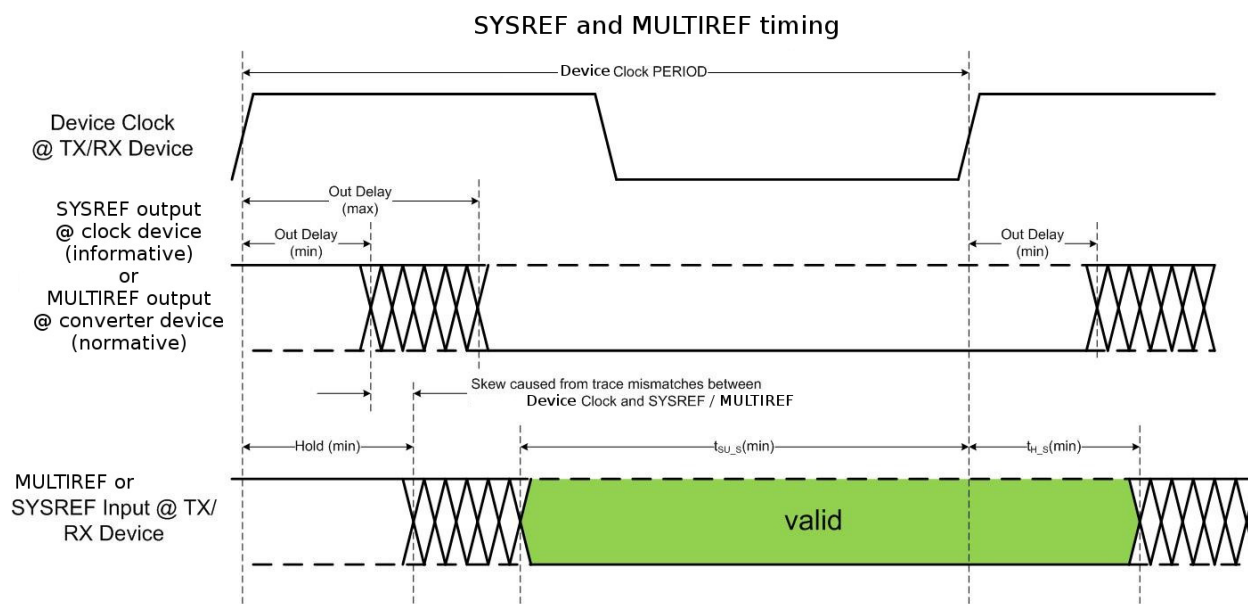


Figure 7 — SYSREF and MULTIREF signal timing

4.3.6 MULTIREF signal (device subclass 1)

In applications where lane alignment between multiple converter devices is required, but no deterministic latency is needed, the SYSREF signal may be replaced by the optional MULTIREF signal. The MULTIREF signal is fed to the SYSREF input of the converter devices. The converter devices shall use the MULTIREF signal to align their LMFCs or LEMCs, exactly in the same way as SYSREF. However, unlike SYSREF, the MULTIREF signal is generated in a converter device, not in the clock generator. For this reason, it may be more difficult to meet the setup and hold requirements relative to the device clock at the device inputs. Hence, the alignment obtained by means of the MULTIREF signal is possibly less accurate than what can be obtained by the SYSREF signal. Despite its disadvantages of no deterministic latency and possibly reduced alignment accuracy, the MULTIREF signal may be a useful option, because it simplifies the clocking architecture.

Figure 7 shows the critical timing specifications relating to the MULTIREF signal. The specification of the setup and hold times is common with the SYSREF signal. In addition, the specification of the devices that are capable of transmitting the MULTIREF signal shall specify the delay of the MULTIREF output relative to the active device clock edge. It is recommended that this delay is programmable, to facilitate compliance with the setup and hold times of the MULTIREF receiving device(s).

4.3.6 MULTIREF signal (device Subclass 1) (cont'd)

The timing of the MULTIREF signal is controlled by a main device. A main ADC device shall align the rising edge of the transmitted MULTIREF signal to the active edge of its LMFC or LEMC. A main DAC device shall align its LMFC or LEMC and the rising edge of the transmitted MULTIREF signal to the start of the received multiframe or extended multiblock on the latest lane. Optionally, a main device may advance the transmitted MULTIREF signal by a programmable number of device clock cycles relative to the LMFC or LEMC, to compensate the transmission delay to the secondary device(s). After alignment of its LMFC to the latest lane signal, a main DAC device shall delay the received lane signals relative to the LMFC or LEMC as specified by the parameter *RBD* (see 4.2.1).

Secondary devices accept the MULTIREF signal at their SYSREF input. A secondary device shall align its LMFC or LEMC to the rising edge of the received MULTIREF signal. After alignment of its LMFC or LEMC to the received MULTIREF signal, a secondary DAC device shall delay the start of the multiframe or extended multiblock of the received lane signals relative to its LMFC or LEMC as specified by the parameter *RBD*, see 4.2.1.

A logic device receiver connected to a multipoint ADC link that is aligned using MULTIREF, shall behave as if it were a subclass 0 receiver: the RX buffers are released at the earliest opportunity after the detection of a multiframe or extended multiblock boundary in each lane.

There are two kinds of MULTIREF devices possible: one-directional and repeater type. One-directional devices can either receive the MULTIREF signal or transmit it, but not simultaneously. Repeater devices receive the MULTIREF signal at their SYSREF input and forward it to a MULTIREF output. One-directional devices can be used in a multidrop topology, and repeater devices in a daisy chain topology, as illustrated in Figure 8. When using a daisy chain topology, it is recommended to use a periodic or “gapped” periodic MULTIREF signal, in order that the repeater device can regenerate the MULTIREF signal and align it to the received MULTIREF signal with essentially zero delay. A secondary repeater device may optionally advance the transmitted MULTIREF signal by a programmable number of device clock cycles relative to its LMFC or LEMC, to compensate the transmission delay to the next secondary device.

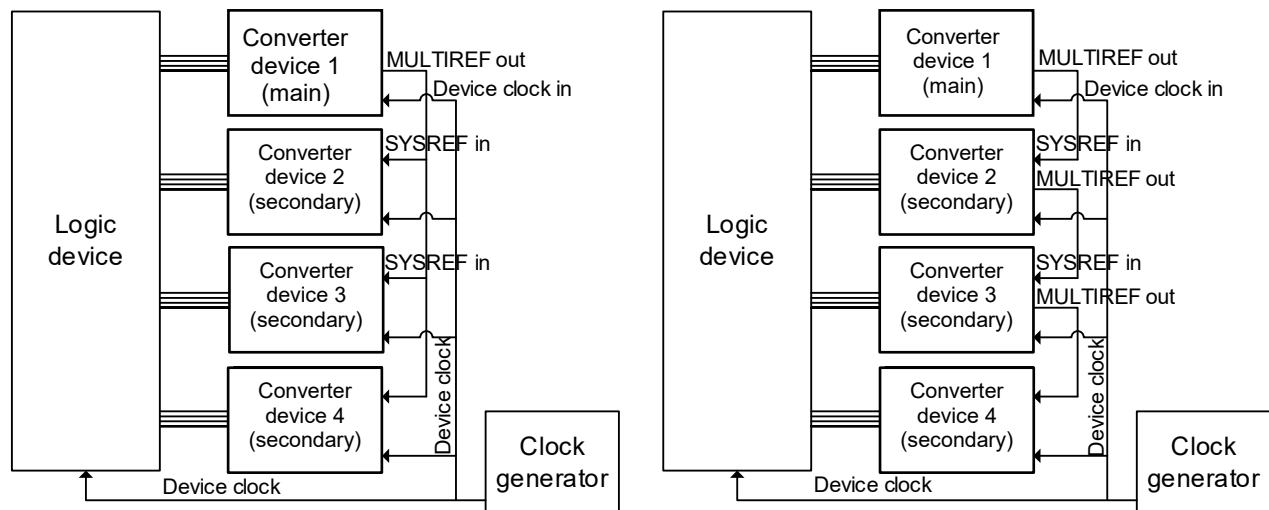


Figure 8 — Examples of MULTIREF distribution. Left: multidrop, and right: daisy chain topology

4.3.7 SYNC~ generation and detection clocks (8B/10B link layer)

The SYNC~ generation clock is the clock used in the RX device for generating the SYNC~ signal to the hard-wired SYNC interface (see 8.8.2). The SYNC~ detection clock is the clock used in the TX device for sampling the SYNC~ signal from the hard-wired SYNC interface (see 8.8.2).

In most of the expected applications, it will be possible to use the link layer clock as SYNC~ generation or detection clock. However, it may be necessary to use another clock in the following cases:

- for backward compatibility with a previous version of this standard (see Annex M);
- if the multiframe duration is not a whole number of link layer clock periods;
- to provide a sufficiently fine detection resolution in a subclass-2 TX (see 8.5.3.4).

In device subclasses 1 and 2, the SYNC~ generation and detection clocks shall operate at a harmonic of the LMFC and be phase aligned to the LMFC.

The duration T_{SYNCCLK} of one cycle of the SYNC~ generation or detection clock shall comply to the following requirements:

For subclass 1 devices: $T_{\text{SYNCCLK}} \leq 80 \text{ UI}$

For subclass 2 devices: $T_{\text{SYNCCLK}} \leq \begin{cases} 20 \text{ UI}, & f_b \leq 4 \text{ Gbps} \\ 40 \text{ UI}, & 4 \text{ GHz} < f_b \leq 8 \text{ Gbps} \\ 80 \text{ UI}, & f_b > 8 \text{ Gbps} \end{cases}$

where

f_b is the serial bit rate and UI is the duration of a serial bit.

NOTE The above requirements ensure that the TX device can distinguish a synchronization request from an error report (see 8.8.2). The requirement for subclass 2 devices ensures in addition that the SYNC~ generation and detection clocks will not be slower than the slowest expected link layer clock, so that the skew budget can be based on the assumptions for the link layer clock.

4.3.8 Skew and latency variation budget

Skew is introduced at various places in the link(s) and within the clock distribution circuit. The implementation of the system shall be such that certain amounts of skew can be tolerated without affecting system performance. In JESD204 this means that all data generated simultaneously at the TX side will be aligned to the same clock edge at the RX side. Deterministic latency requires in addition alignment to a predictable device clock edge.

NOTE Skew compares signals at either the receiving or the transmitting side of the link, not signals at opposite sides of the link.

The total skew budget can be broken down into the following parts:

- a) **Transmission skew:** the skew contribution due to the different propagation delays in the transmission medium for different lanes.
- b) **Processing skew:** the skew contribution due to the different signal processing delays inside the devices for different lanes. Processing skew includes the effects of both physical delays and clock domain crossings.
- c) **Timing reference skew:** the skew contribution due to the different arrival times of timing reference signals at the converter devices connected to a multipoint link. In JESD204, these timing reference signals are the device clock and, depending on the type of the link layer and the device subclass, SYSREF (optionally MULTIREF) and SYNC~.

NOTE Wander is not counted in the skew value, see OIF-CEI-04.0 subclause 1.6 [12].

Transmission skew and processing skew are generally larger for multipoint links than for single links. Inside a link, the lane lengths in the transmission medium are usually matched. Between links, there may be a significant difference in lane lengths. Inside the devices, the input or output pins belonging to a single link are usually situated next to each other. The pins of different links of a multipoint link may be situated at different edges of the device package, which could lead to a significant difference in propagation delays inside large (logic) devices. Although this difference in propagation delay can be compensated by extra buffering in the shorter paths, the physical distance between the links will cause increased sensitivity to PVT and clock skew in the device. Between converter devices, the delays caused by e.g., clock boundary transitions can be different. The skew budgets have therefore an allowance for extra skew on multipoint links. This allowance is modelled by the items inter-link transmission skew and inter-link processing skew.

All deterministic latency devices are required to support multipoint links. The system implementer will generally adjust the same deterministic latency on all links of a multipoint link. Therefore, the receive buffer on the fastest lane in the system shall be able to compensate for the extra delay on the slowest lane. Hence, the receive buffer of a deterministic latency device shall be dimensioned for the maximum skew on the multipoint link. Also, the system implementer will generally adjust the same deterministic latency on each board. Even if there is only a single link, this link could be “fast” on one board and “slow” on another board. Hence, also in case of a single link, the receive buffer shall be dimensioned for the maximum skew on the multipoint link.