

# JEDEC STANDARD

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## FBDIMM Specification:

## DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

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**JESD205**

**March 2007**

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## Product Description

This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/ PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs). These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DRAM clock speed and offering 4266/5333/6400 MB/s bandwidth.

| DIMM     | DRAM     | DRAM Clock | Single DIMM Bandwidth | Channel Clock | Channel Transfer Rate |
|----------|----------|------------|-----------------------|---------------|-----------------------|
| PC2-4200 | DDR2-533 | 266 MHz    | 4266 MB/s             | 133 MHz       | 3.2 GT/s              |
| PC2-5300 | DDR2-667 | 333 MHz    | 5333 MB/s             | 166 MHz       | 4.0 GT/s              |
| PC2-6400 | DDR2-800 | 400 MHz    | 6400 MB/s             | 200 MHz       | 4.8 GT/s              |

Reference design examples are included which provide an initial basis for Fully Buffered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-5300/PC2-6400 support. All Fully Buffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design..

## Product Family Attributes

|                           |                                                                                                                                                                            |               |                    |                                                                                 |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|--------------------|---------------------------------------------------------------------------------|
| DIMM organization         | x72 ECC                                                                                                                                                                    |               |                    |                                                                                 |
| DIMM dimensions (nominal) | 30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness)<br>MO-256 variation AB<br>30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness)<br>MO-256 variation BB |               |                    |                                                                                 |
| Pin count                 | 240                                                                                                                                                                        |               |                    |                                                                                 |
| SDRAMs supported          | 256Mb, 512Mb, 1Gb, 2Gb, 4Gb                                                                                                                                                |               |                    |                                                                                 |
| Capacity                  | 256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB                                                                                                                                     |               |                    |                                                                                 |
| Serial PD                 | Consistent with JC 45                                                                                                                                                      |               |                    |                                                                                 |
| Supply voltages (nominal) | min                                                                                                                                                                        | typ           | max                |                                                                                 |
|                           | 1.7                                                                                                                                                                        | 1.8           | 1.9                | (DRAM $V_{DD}/V_{DDQ}$ , AMB $V_{DDQ}$ )                                        |
|                           | 1.455 <sup>1</sup>                                                                                                                                                         | 1.5           | 1.575 <sup>1</sup> | (AMB $V_{CC}/V_{CCFBD}$ )                                                       |
|                           | 0.453* $V_{DD}$                                                                                                                                                            | 0.5* $V_{DD}$ | 0.547* $V_{DD}$    | (DRAM Interface $V_{TT}$ )<br>This supply should track as 0.5 * 1.8 volt supply |
|                           | 3.0                                                                                                                                                                        | 3.3           | 3.6                | ( $V_{DDSPD}$ )                                                                 |
| Buffer Interface          | High-speed Differential Point-to-point Link at 1.5 volt                                                                                                                    |               |                    |                                                                                 |
| DRAM Interface            | SSTL_18                                                                                                                                                                    |               |                    |                                                                                 |

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.

Note 2: V<sub>tt</sub> range accommodates measurable offset due to complementary CA bus current paths. (See V<sub>tt</sub> section)

An Unloaded system should supply V<sub>tt</sub> of 0.48\*V<sub>dd</sub>/0.52\*V<sub>dd</sub> to Dimm socket

The reference designs for the DIMM PCBs are called the “raw cards”, abbreviated R/C. After the designs have been verified in working systems, the JEDEC JC-45 committee will post registrations of these R/C designs to the JEDEC web site for use by the industry at large.

### Product Family Raw Card Types

| Raw Card | DRAM Data Width | # of Ranks | # of DRAM | Z-axis             | Width x Height (mm) |
|----------|-----------------|------------|-----------|--------------------|---------------------|
| A        | x8              | 1          | 9         | planar             | 133.35 x 30.35      |
| B        | x8              | 2          | 18        | planar             | 133.35 x 30.35      |
| C        | x4              | 1          | 18        | planar             | 133.35 x 30.35      |
| D        | x4              | 2          | 36        | stacked / dual die | 133.35 x 30.35      |
| E        | x4              | 2          | 36        | planar             | 133.35 x 30.35      |
| H        | x4              | 2          | 36        | planar             | 133.35 x 30.35      |
| J        | x4              | 2          | 36        | stacked / dual die | 133.35 x 30.35      |

## Environmental Requirements

DDR2 SDRAM Fully Buffered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

### Environmental Parameters

| Symbol           | Parameter                                 | Rating      | Units    | Notes |
|------------------|-------------------------------------------|-------------|----------|-------|
| T <sub>OPR</sub> | Operating temperature                     | See Note    |          | 1     |
| H <sub>OPR</sub> | Operating humidity (relative)             | 10 to 90    | %        | 2     |
| T <sub>STG</sub> | Storage temperature                       | -50 to +100 | °C       | 2     |
| H <sub>STG</sub> | Storage humidity (without condensation)   | 5 to 95     | %        | 2     |
| P <sub>BAR</sub> | Barometric pressure (operating & storage) | 105 to 69   | K Pascal | 2     |

1. The designer must meet the case temperature specifications for individual module components.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Architecture

## Architecture

## DIMM Connector Pin Description

| Pin Name                     | Pin Description                                                                                                                                                                                                                                                                                                                                                                                       | Count |
|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| SCK                          | System Clock Input, positive line <sup>1</sup>                                                                                                                                                                                                                                                                                                                                                        | 1     |
| $\overline{\text{SCK}}$      | System Clock Input, negative line <sup>1</sup>                                                                                                                                                                                                                                                                                                                                                        | 1     |
| PN[13:0]                     | Primary Northbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                               | 14    |
| $\overline{\text{PN}}[13:0]$ | Primary Northbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                               | 14    |
| PS[9:0]                      | Primary Southbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                               | 10    |
| $\overline{\text{PS}}[9:0]$  | Primary Southbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                               | 10    |
| SN[13:0]                     | Secondary Northbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                             | 14    |
| $\overline{\text{SN}}[13:0]$ | Secondary Northbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                             | 14    |
| SS[9:0]                      | Secondary Southbound Data, positive lines                                                                                                                                                                                                                                                                                                                                                             | 10    |
| $\overline{\text{SS}}[9:0]$  | Secondary Southbound Data, negative lines                                                                                                                                                                                                                                                                                                                                                             | 10    |
| SCL                          | Serial Presence Detect (SPD) Clock Input                                                                                                                                                                                                                                                                                                                                                              | 1     |
| SDA                          | SPD Data Input / Output                                                                                                                                                                                                                                                                                                                                                                               | 1     |
| SA[2:0]                      | SPD Address Inputs, also used to select the DIMM number in the AMB                                                                                                                                                                                                                                                                                                                                    | 3     |
| VID[1:0]                     | Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs<br>VID[0] is $V_{DD}$ value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is $V_{CC}$ value: OPEN = 1.5 V, GND = 1.2 V                                                                                                                                                                                                            | 2     |
| $\overline{\text{RESET}}$    | AMB reset signal                                                                                                                                                                                                                                                                                                                                                                                      | 1     |
| RFU                          | Reserved for Future Use <sup>2</sup>                                                                                                                                                                                                                                                                                                                                                                  | 16    |
| $V_{CC}$                     | AMB Core Power and AMB Channel Interface Power (1.5 Volt)                                                                                                                                                                                                                                                                                                                                             | 8     |
| $V_{DD}$                     | DRAM Power and AMB DRAM I/O Power (1.8 Volt)                                                                                                                                                                                                                                                                                                                                                          | 24    |
| $V_{TT}$                     | DRAM Address/Command/Clock Termination Power ( $V_{DD}/2$ )                                                                                                                                                                                                                                                                                                                                           | 4     |
| $V_{DDSPD}$                  | SPD Power                                                                                                                                                                                                                                                                                                                                                                                             | 1     |
| $V_{SS}$                     | Ground                                                                                                                                                                                                                                                                                                                                                                                                | 80    |
| DNU/M_Test                   | The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of $V_{ref}$ which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.<br>1 | 1     |
|                              | Total                                                                                                                                                                                                                                                                                                                                                                                                 | 240   |

1. System Clock Signals SCK and  $\overline{\text{SCK}}$  switch at one half the DRAM CK/ $\overline{\text{CK}}$  frequency  
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

## DDR2 240-pin FBDIMM Pinout

| Pin # | Front Side                | Pin # | Back Side               | Pin # | Front Side               | Pin # | Back Side                | Pin # | Front Side               | Pin # | Back Side                | Pin # | Front Side              | Pin # | Back Side               |
|-------|---------------------------|-------|-------------------------|-------|--------------------------|-------|--------------------------|-------|--------------------------|-------|--------------------------|-------|-------------------------|-------|-------------------------|
| 1     | V <sub>DD</sub>           | 121   | V <sub>DD</sub>         | 31    | PN3                      | 151   | SN3                      | 61    | $\overline{\text{PN9}}$  | 181   | $\overline{\text{SN9}}$  | 91    | $\overline{\text{PS9}}$ | 211   | $\overline{\text{SS9}}$ |
| 2     | V <sub>DD</sub>           | 122   | V <sub>DD</sub>         | 32    | $\overline{\text{PN3}}$  | 152   | $\overline{\text{SN3}}$  | 62    | V <sub>SS</sub>          | 182   | V <sub>SS</sub>          | 92    | V <sub>SS</sub>         | 212   | V <sub>SS</sub>         |
| 3     | V <sub>DD</sub>           | 123   | V <sub>DD</sub>         | 33    | V <sub>SS</sub>          | 153   | V <sub>SS</sub>          | 63    | PN10                     | 183   | SN10                     | 93    | PS5                     | 213   | SS5                     |
| 4     | V <sub>SS</sub>           | 124   | V <sub>SS</sub>         | 34    | PN4                      | 154   | SN4                      | 64    | $\overline{\text{PN10}}$ | 184   | $\overline{\text{SN10}}$ | 94    | $\overline{\text{PS5}}$ | 214   | $\overline{\text{SS5}}$ |
| 5     | V <sub>DD</sub>           | 125   | V <sub>DD</sub>         | 35    | $\overline{\text{PN4}}$  | 155   | $\overline{\text{SN4}}$  | 65    | V <sub>SS</sub>          | 185   | V <sub>SS</sub>          | 95    | V <sub>SS</sub>         | 215   | V <sub>SS</sub>         |
| 6     | V <sub>DD</sub>           | 126   | V <sub>DD</sub>         | 36    | V <sub>SS</sub>          | 156   | V <sub>SS</sub>          | 66    | PN11                     | 186   | SN11                     | 96    | PS6                     | 216   | SS6                     |
| 7     | V <sub>DD</sub>           | 127   | V <sub>DD</sub>         | 37    | PN5                      | 157   | SN5                      | 67    | $\overline{\text{PN11}}$ | 187   | $\overline{\text{SN11}}$ | 97    | $\overline{\text{PS6}}$ | 217   | $\overline{\text{SS6}}$ |
| 8     | V <sub>SS</sub>           | 128   | V <sub>SS</sub>         | 38    | $\overline{\text{PN5}}$  | 158   | $\overline{\text{SN5}}$  | 68    | V <sub>SS</sub>          | 188   | V <sub>SS</sub>          | 98    | V <sub>SS</sub>         | 218   | V <sub>SS</sub>         |
| 9     | V <sub>CC</sub>           | 129   | V <sub>CC</sub>         | 39    | V <sub>SS</sub>          | 159   | V <sub>SS</sub>          | KEY   |                          |       |                          | 99    | PS7                     | 219   | SS7                     |
| 10    | V <sub>CC</sub>           | 130   | V <sub>CC</sub>         | 40    | PN13                     | 160   | SN13                     | 69    | V <sub>SS</sub>          | 189   | V <sub>SS</sub>          | 100   | $\overline{\text{PS7}}$ | 220   | $\overline{\text{SS7}}$ |
| 11    | V <sub>SS</sub>           | 131   | V <sub>SS</sub>         | 41    | $\overline{\text{PN13}}$ | 161   | $\overline{\text{SN13}}$ | 70    | PS0                      | 190   | SS0                      | 101   | V <sub>SS</sub>         | 221   | V <sub>SS</sub>         |
| 12    | V <sub>CC</sub>           | 132   | V <sub>CC</sub>         | 42    | V <sub>SS</sub>          | 162   | V <sub>SS</sub>          | 71    | $\overline{\text{PS0}}$  | 191   | $\overline{\text{SS0}}$  | 102   | PS8                     | 222   | SS8                     |
| 13    | V <sub>CC</sub>           | 133   | V <sub>CC</sub>         | 43    | V <sub>SS</sub>          | 163   | V <sub>SS</sub>          | 72    | V <sub>SS</sub>          | 192   | V <sub>SS</sub>          | 103   | $\overline{\text{PS8}}$ | 223   | $\overline{\text{SS8}}$ |
| 14    | V <sub>SS</sub>           | 134   | V <sub>SS</sub>         | 44    | RFU*                     | 164   | RFU*                     | 73    | PS1                      | 193   | SS1                      | 104   | V <sub>SS</sub>         | 224   | V <sub>SS</sub>         |
| 15    | V <sub>TT</sub>           | 135   | V <sub>TT</sub>         | 45    | RFU*                     | 165   | RFU*                     | 74    | $\overline{\text{PS1}}$  | 194   | $\overline{\text{SS1}}$  | 105   | RFU**                   | 225   | RFU**                   |
| 16    | VID1                      | 136   | VID0                    | 46    | V <sub>SS</sub>          | 166   | V <sub>SS</sub>          | 75    | V <sub>SS</sub>          | 195   | V <sub>SS</sub>          | 106   | RFU**                   | 226   | RFU**                   |
| 17    | $\overline{\text{RESET}}$ | 137   | DNU/M_Test              | 47    | V <sub>SS</sub>          | 167   | V <sub>SS</sub>          | 76    | PS2                      | 196   | SS2                      | 107   | V <sub>SS</sub>         | 227   | V <sub>SS</sub>         |
| 18    | V <sub>SS</sub>           | 138   | V <sub>SS</sub>         | 48    | PN12                     | 168   | SN12                     | 77    | $\overline{\text{PS2}}$  | 197   | $\overline{\text{SS2}}$  | 108   | V <sub>DD</sub>         | 228   | SCK                     |
| 19    | RFU**                     | 139   | RFU**                   | 49    | $\overline{\text{PN12}}$ | 169   | $\overline{\text{SN12}}$ | 78    | V <sub>SS</sub>          | 198   | V <sub>SS</sub>          | 109   | V <sub>DD</sub>         | 229   | $\overline{\text{SCK}}$ |
| 20    | RFU**                     | 140   | RFU**                   | 50    | V <sub>SS</sub>          | 170   | V <sub>SS</sub>          | 79    | PS3                      | 199   | SS3                      | 110   | V <sub>SS</sub>         | 230   | V <sub>SS</sub>         |
| 21    | V <sub>SS</sub>           | 141   | V <sub>SS</sub>         | 51    | PN6                      | 171   | SN6                      | 80    | $\overline{\text{PS3}}$  | 200   | $\overline{\text{SS3}}$  | 111   | V <sub>DD</sub>         | 231   | V <sub>DD</sub>         |
| 22    | PN0                       | 142   | SN0                     | 52    | $\overline{\text{PN6}}$  | 172   | $\overline{\text{SN6}}$  | 81    | V <sub>SS</sub>          | 201   | V <sub>SS</sub>          | 112   | V <sub>DD</sub>         | 232   | V <sub>DD</sub>         |
| 23    | $\overline{\text{PN0}}$   | 143   | $\overline{\text{SN0}}$ | 53    | V <sub>SS</sub>          | 173   | V <sub>SS</sub>          | 82    | PS4                      | 202   | SS4                      | 113   | V <sub>DD</sub>         | 233   | V <sub>DD</sub>         |
| 24    | V <sub>SS</sub>           | 144   | V <sub>SS</sub>         | 54    | PN7                      | 174   | SN7                      | 83    | $\overline{\text{PS4}}$  | 203   | $\overline{\text{SS4}}$  | 114   | V <sub>SS</sub>         | 234   | V <sub>SS</sub>         |
| 25    | PN1                       | 145   | SN1                     | 55    | $\overline{\text{PN7}}$  | 175   | $\overline{\text{SN7}}$  | 84    | V <sub>SS</sub>          | 204   | V <sub>SS</sub>          | 115   | V <sub>DD</sub>         | 235   | V <sub>DD</sub>         |
| 26    | $\overline{\text{PN1}}$   | 146   | $\overline{\text{SN1}}$ | 56    | V <sub>SS</sub>          | 176   | V <sub>SS</sub>          | 85    | V <sub>SS</sub>          | 205   | V <sub>SS</sub>          | 116   | V <sub>DD</sub>         | 236   | V <sub>DD</sub>         |
| 27    | V <sub>SS</sub>           | 147   | V <sub>SS</sub>         | 57    | PN8                      | 177   | SN8                      | 86    | RFU*                     | 206   | RFU*                     | 117   | V <sub>TT</sub>         | 237   | V <sub>TT</sub>         |
| 28    | PN2                       | 148   | SN2                     | 58    | $\overline{\text{PN8}}$  | 178   | $\overline{\text{SN8}}$  | 87    | RFU*                     | 207   | RFU*                     | 118   | SA2                     | 238   | VDDSPD                  |
| 29    | $\overline{\text{PN2}}$   | 149   | $\overline{\text{SN2}}$ | 59    | V <sub>SS</sub>          | 179   | V <sub>SS</sub>          | 88    | V <sub>SS</sub>          | 208   | V <sub>SS</sub>          | 119   | SDA                     | 239   | SA0                     |
| 30    | V <sub>SS</sub>           | 150   | V <sub>SS</sub>         | 60    | PN9                      | 180   | SN9                      | 89    | V <sub>SS</sub>          | 209   | V <sub>SS</sub>          | 120   | SCL                     | 240   | SA1                     |
|       |                           |       |                         |       |                          |       |                          | 90    | PS9                      | 210   | SS9                      |       |                         |       |                         |

RFU = Reserved Future Use.

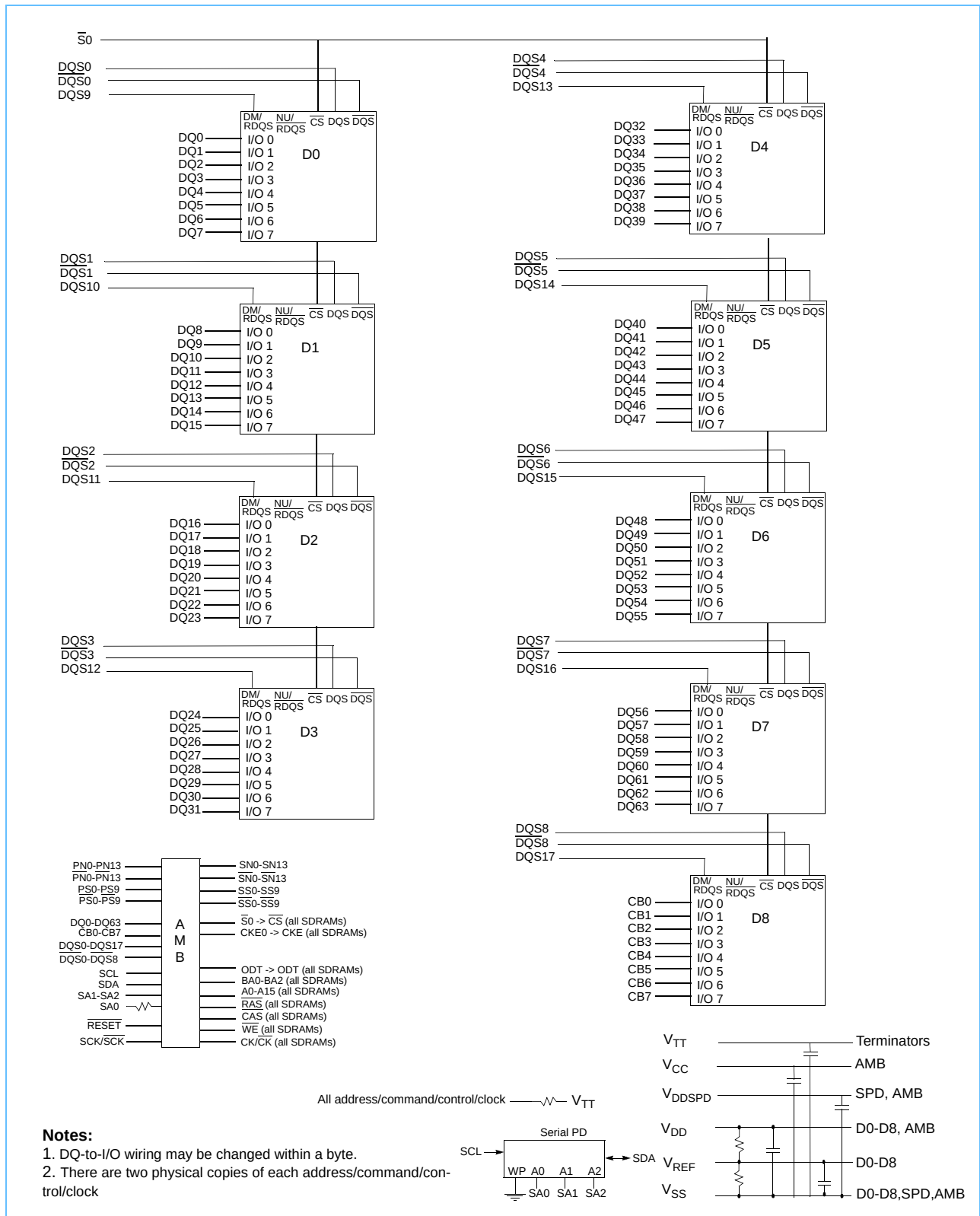
\* These pin positions are reserved for forwarded clocks to be used in future module implementations

\*\* These pin positions are reserved for future architecture flexibility

1) The following signals are CRC bits and thus appear out of the normal sequence: PN12/ $\overline{\text{PN12}}$ , SN12/ $\overline{\text{SN12}}$ , PN13/ $\overline{\text{PN13}}$ , SN13/ $\overline{\text{SN13}}$ , PS9/PS9, SS9/SS9

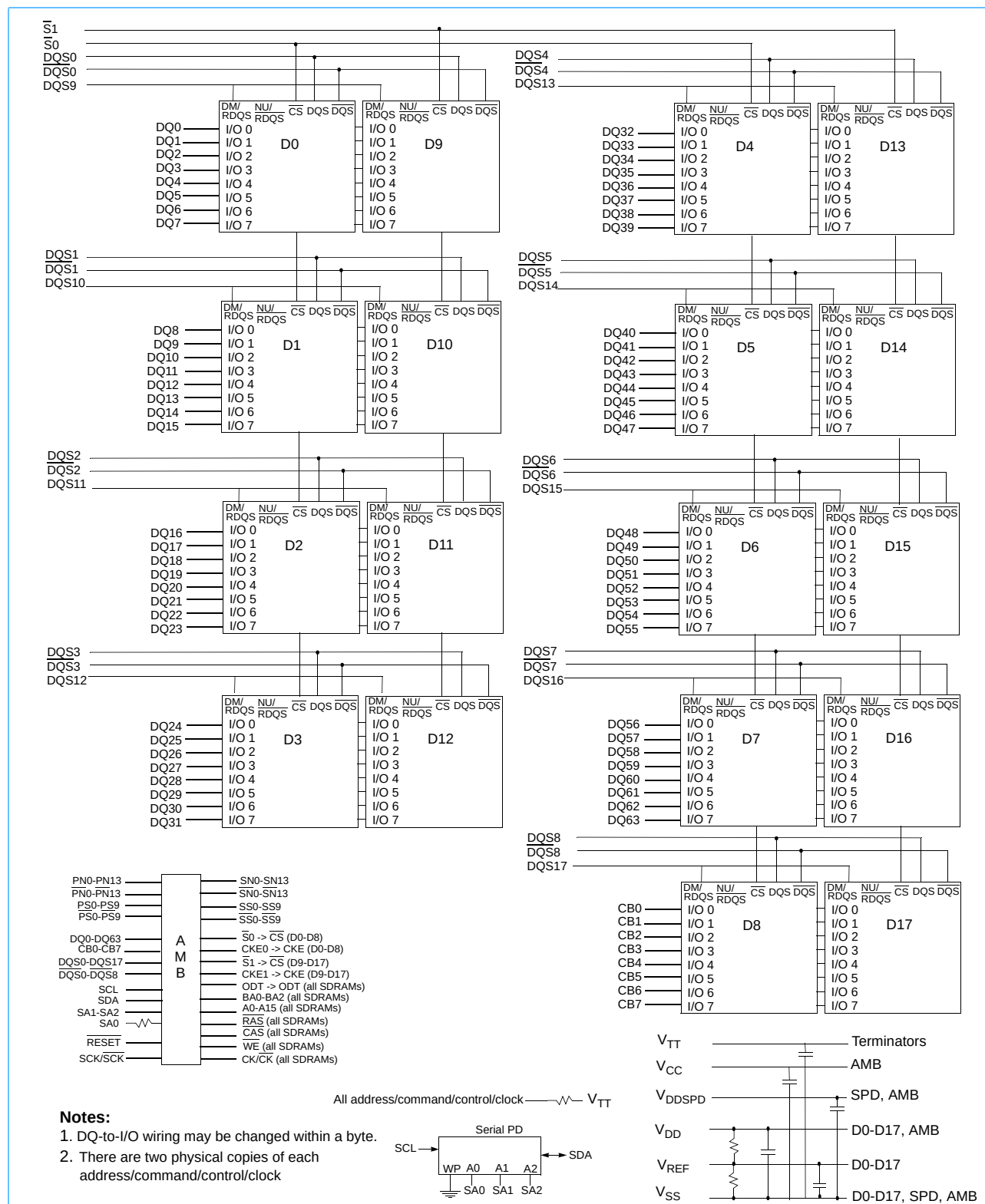
## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Block Diagram: Raw Card Version A (x72 ECC DIMM, one physical rank of x8 DDR2 SDRAMs)



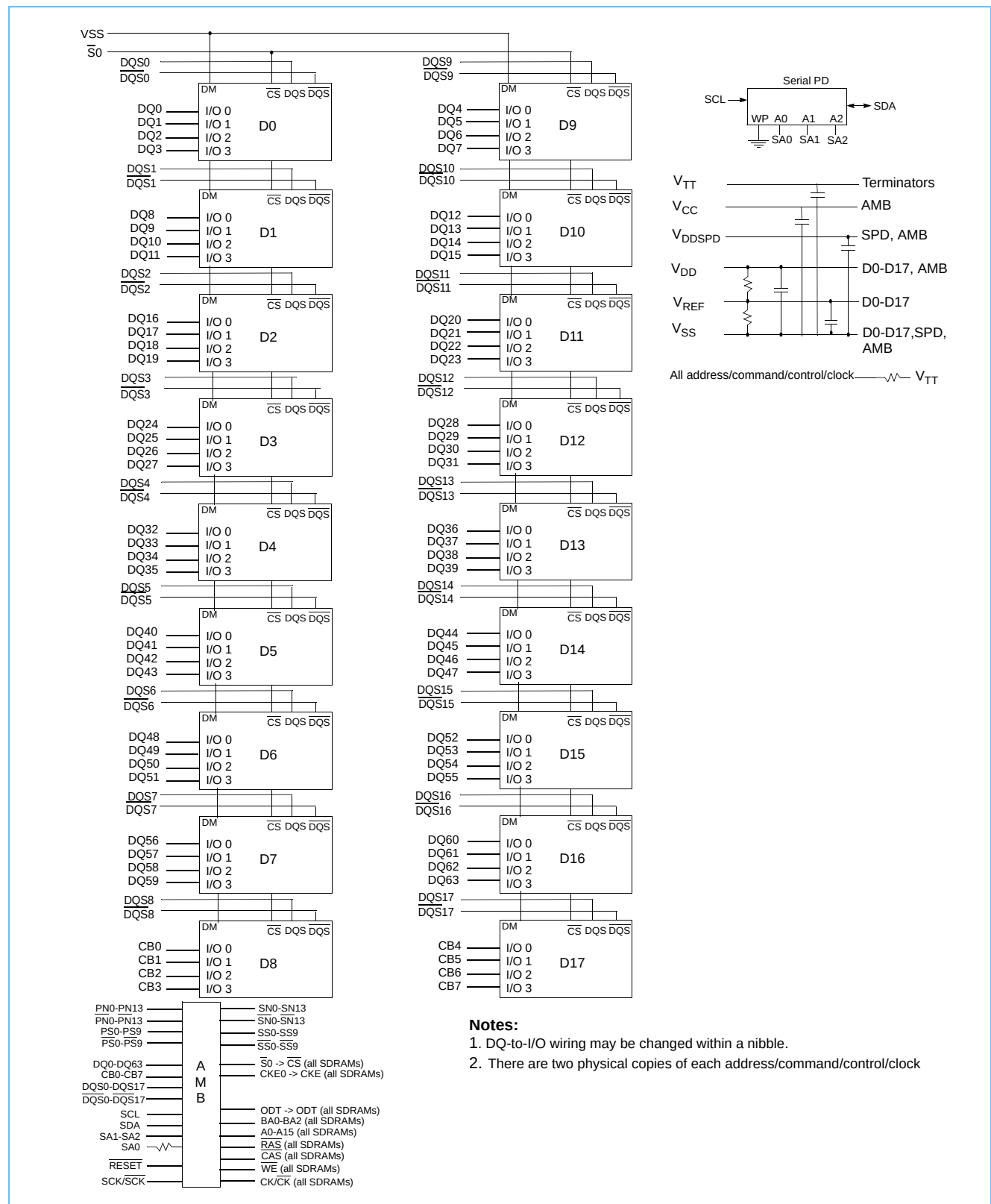
## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Block Diagram: Raw Card Version B (x72 ECC DIMMs, two physical ranks of x8 DDR2 SDRAMs)



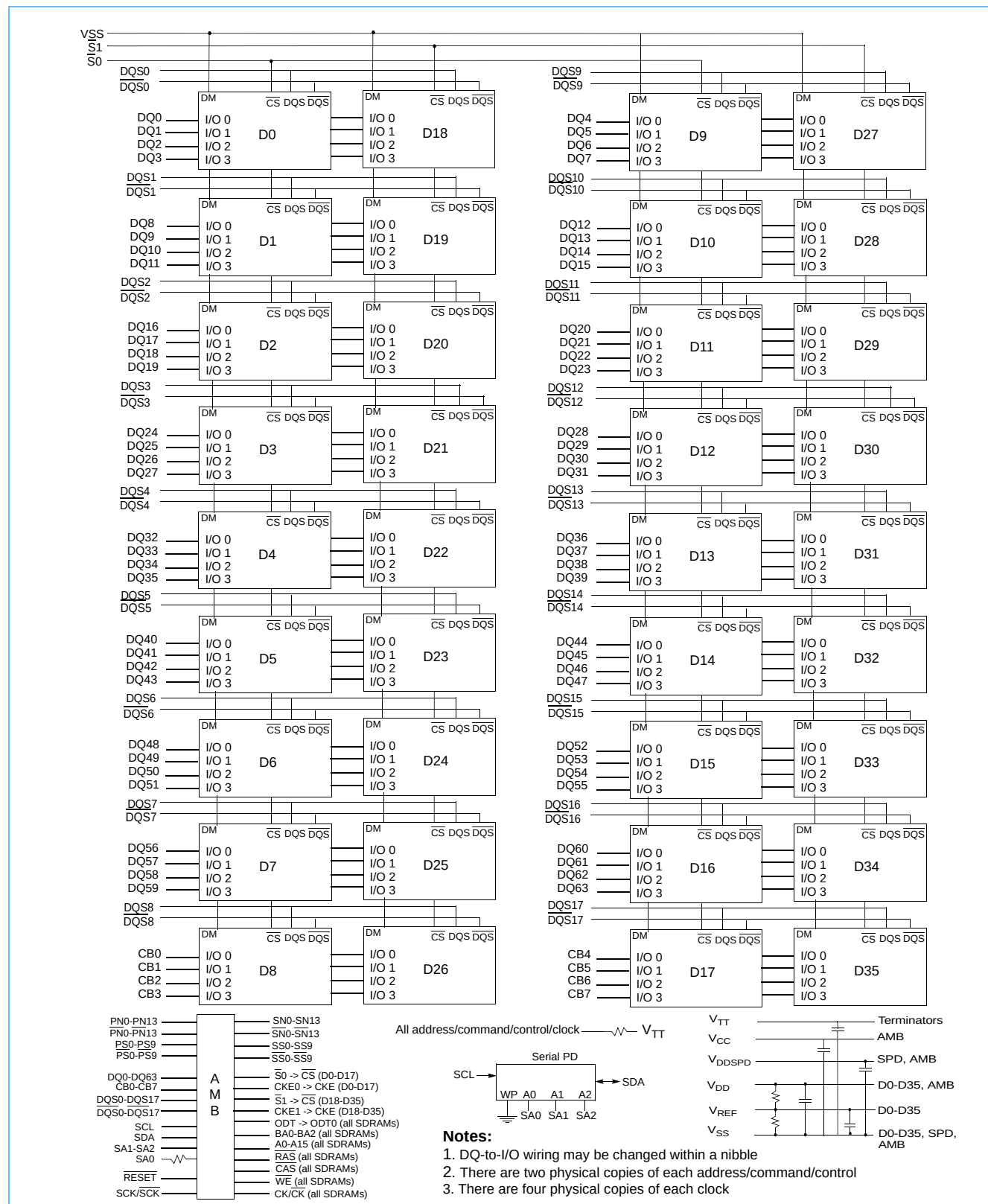
## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Block Diagram: Raw Card Version C (x72 ECC DIMM, one physical rank of x4 DDR2 SDRAMs)



## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Block Diagram: RC Versions D,E,H,J (x72 ECC DIMMs, 2 physical ranks of x4 DDR2 SDRAMs)



## Component Details:

## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Component Details:

## DDR2 SDRAM, 256 Mb to 4 Gb

Raw cards A and B accommodate the x8 ballout with or without support balls, using the x8 common footprint. Raw card C accommodates the x4 ballout with or without support balls, using the x4 common footprint. Raw card D accommodates the stacked x4 ballout with or without support balls, using the stacked x4 common footprint. The tables on the next few pages may include blank rows above the first row with balls, so that all of the tables line up with the common footprints for x4, x8 and stacked x4.

## Pin Assignments for x4 and x8 Ballouts without Support Balls (Top View)

(MO-207 variation DJ-z, 60 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

|   | 1    | 2    | 3                      | 7                       | 8                       | 9    |
|---|------|------|------------------------|-------------------------|-------------------------|------|
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
| A | VDD  | NC   | VSS                    | VSSQ                    | $\overline{\text{DQS}}$ | VDDQ |
| B | NC   | VSSQ | DM                     | DQS                     | VSSQ                    | NC   |
| C | VDDQ | DQ1  | VDDQ                   | VDDQ                    | DQ0                     | VDDQ |
| D | NC   | VSSQ | DQ3                    | DQ2                     | VSSQ                    | NC   |
| E | VDDL | VREF | VSS                    | VSSDL                   | CK                      | VDD  |
| F |      | CKE  | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |
| G | BA2  | BA0  | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |
| H |      | A10  | A1                     | A2                      | A0                      | VDD  |
| J | VSS  | A3   | A5                     | A6                      | A4                      |      |
| K |      | A7   | A9                     | A11                     | A8                      | VSS  |
| L | VDD  | A12  | A14,NC                 | A15,NC                  | A13,NC                  |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |
|   |      |      |                        |                         |                         |      |

x8 Ballout of DDR2 SDRAMs (Top view)

|  | 1    | 2           | 3                      | 7                       | 8                       | 9    |
|--|------|-------------|------------------------|-------------------------|-------------------------|------|
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  | VDD  | NU/<br>RDQS | VSS                    | VSSQ                    | $\overline{\text{DQS}}$ | VDDQ |
|  | DQ6  | VSSQ        | DM/<br>RDQS            | DQS                     | VSSQ                    | DQ7  |
|  | VDDQ | DQ1         | VDDQ                   | VDDQ                    | DQ0                     | VDDQ |
|  | DQ4  | VSSQ        | DQ3                    | DQ2                     | VSSQ                    | DQ5  |
|  | VDDL | VREF        | VSS                    | VSSDL                   | CK                      | VDD  |
|  |      | CKE         | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |
|  | BA2  | BA0         | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |
|  |      | A10         | A1                     | A2                      | A0                      | VDD  |
|  | VSS  | A3          | A5                     | A6                      | A4                      |      |
|  |      | A7          | A9                     | A11                     | A8                      | VSS  |
|  | VDD  | A12         | A14,NC                 | A15,NC                  | A13,NC                  |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |
|  |      |             |                        |                         |                         |      |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball A2 (NU/RDQS) will be open on the x8 based DIMMs.

Pin Assignments for Stacked x4 Ballout without Support Balls (Top View)

(MO-242 variation AA, 63 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

|   |      |      |                        |  |                         |                         |                         |
|---|------|------|------------------------|--|-------------------------|-------------------------|-------------------------|
|   | 1    | 2    | 3                      |  | 7                       | 8                       | 9                       |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
| A | VDD  | NC   | VSS                    |  | VSSQ                    | $\overline{\text{DQS}}$ | VDDQ                    |
| B | NC   | VSSQ | DM                     |  | DQS                     | VSSQ                    | NC                      |
| C | VDDQ | DQ1  | VDDQ                   |  | VDDQ                    | DQ0                     | VDDQ                    |
| D | NC   | VSSQ | DQ3                    |  | DQ2                     | VSSQ                    | NC                      |
| E | VDDL | VREF | VSS                    |  | VSSDL                   | CK                      | VDD                     |
| F |      | CKE0 | $\overline{\text{WE}}$ |  | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT0                    |
| G | BA2  | BA0  | BA1                    |  | $\overline{\text{CAS}}$ | $\overline{\text{CS0}}$ | $\overline{\text{CS1}}$ |
| H | CKE1 | A10  | A1                     |  | A2                      | A0                      | VDD                     |
| J | VSS  | A3   | A5                     |  | A6                      | A4                      | ODT1                    |
| K |      | A7   | A9                     |  | A11                     | A8                      | VSS                     |
| L | VDD  | A12  | A14,NC                 |  | A15,NC                  | A13,NC                  |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |
|   |      |      |                        |  |                         |                         |                         |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to stacked x4 PCB symbol.
3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

**Component Details:****DDR2 SDRAM Fully Buffered DIMM Design Specification**

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DM-z, 68 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

x8 Ballout of DDR2 SDRAMs (Top view)

|   | 1    | 2    | 3                      | 7                       | 8                       | 9    |  | 1    | 2                               | 3                      | 7                       | 8                       | 9    |
|---|------|------|------------------------|-------------------------|-------------------------|------|--|------|---------------------------------|------------------------|-------------------------|-------------------------|------|
| A | NC   | NC   |                        |                         | NC                      | NC   |  | NC   | NC                              |                        |                         | NC                      | NC   |
| B |      |      |                        |                         |                         |      |  |      |                                 |                        |                         |                         |      |
| C |      |      |                        |                         |                         |      |  |      |                                 |                        |                         |                         |      |
| D |      |      |                        |                         |                         |      |  |      |                                 |                        |                         |                         |      |
| E | VDD  | NC   | VSS                    | VSSQ                    | $\overline{\text{DQS}}$ | VDDQ |  | VDD  | $\frac{\text{NU}}{\text{RDQS}}$ | VSS                    | VSSQ                    | $\overline{\text{DQS}}$ | VDDQ |
| F | NC   | VSSQ | DM                     | DQS                     | VSSQ                    | NC   |  | DQ6  | VSSQ                            | DM/<br>RDQS            | DQS                     | VSSQ                    | DQ7  |
| G | VDDQ | DQ1  | VDDQ                   | VDDQ                    | DQ0                     | VDDQ |  | VDDQ | DQ1                             | VDDQ                   | VDDQ                    | DQ0                     | VDDQ |
| H | NC   | VSSQ | DQ3                    | DQ2                     | VSSQ                    | NC   |  | DQ4  | VSSQ                            | DQ3                    | DQ2                     | VSSQ                    | DQ5  |
| J | VDDL | VREF | VSS                    | VSSDL                   | CK                      | VDD  |  | VDDL | VREF                            | VSS                    | VSSDL                   | CK                      | VDD  |
| K |      | CKE  | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |  |      | CKE                             | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |
| L | BA2  | BA0  | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |  | BA2  | BA0                             | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |
| M |      | A10  | A1                     | A2                      | A0                      | VDD  |  |      | A10                             | A1                     | A2                      | A0                      | VDD  |
| N | VSS  | A3   | A5                     | A6                      | A4                      |      |  | VSS  | A3                              | A5                     | A6                      | A4                      |      |
| P |      | A7   | A9                     | A11                     | A8                      | VSS  |  |      | A7                              | A9                     | A11                     | A8                      | VSS  |
| L | VDD  | A12  | A14,NC                 | A15,NC                  | A13,NC                  |      |  | VDD  | A12                             | A14,NC                 | A15,NC                  | A13,NC                  |      |
| T |      |      |                        |                         |                         |      |  |      |                                 |                        |                         |                         |      |
| U |      |      |                        |                         |                         |      |  |      |                                 |                        |                         |                         |      |
| V |      |      |                        |                         |                         |      |  |      |                                 |                        |                         |                         |      |
| W | NC   | NC   |                        |                         | NC                      | NC   |  | NC   | NC                              |                        |                         | NC                      | NC   |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball E2 (NU/RDQS) will be open on the x8 based DIMMs.

## DDR2 SDRAM Fully Buffered DIMM Design Specification

Component Details:

Pin Assignments for Stacked x4 Ballout with Support Balls (Top View)

(MO-242 variation AD, 71 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

|   | 1    | 2    | 3                      | 7                       | 8                       | 9                       |
|---|------|------|------------------------|-------------------------|-------------------------|-------------------------|
|   |      |      |                        |                         |                         |                         |
|   |      |      |                        |                         |                         |                         |
|   |      |      |                        |                         |                         |                         |
| A | NC   | NC   |                        |                         | NC                      | NC                      |
| B |      |      |                        |                         |                         |                         |
| C |      |      |                        |                         |                         |                         |
| D |      |      |                        |                         |                         |                         |
| E | VDD  | NC   | VSS                    | VSSQ                    | $\overline{\text{DQS}}$ | VDDQ                    |
| F | NC   | VSSQ | DM                     | DQS                     | VSSQ                    | NC                      |
| G | VDDQ | DQ1  | VDDQ                   | VDDQ                    | DQ0                     | VDDQ                    |
| H | NC   | VSSQ | DQ3                    | DQ2                     | VSSQ                    | NC                      |
| J | VDDL | VREF | VSS                    | VSSDL                   | CK                      | VDD                     |
| K |      | CKE0 | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT0                    |
| L | BA2  | BA0  | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS0}}$ | $\overline{\text{CS1}}$ |
| M | CKE1 | A10  | A1                     | A2                      | A0                      | VDD                     |
| N | VSS  | A3   | A5                     | A6                      | A4                      | ODT1                    |
| P |      | A7   | A9                     | A11                     | A8                      | VSS                     |
| L | VDD  | A12  | A14,NC                 | A15,NC                  | A13,NC                  |                         |
| T |      |      |                        |                         |                         |                         |
| U |      |      |                        |                         |                         |                         |
| V |      |      |                        |                         |                         |                         |
| W | NC   | NC   |                        |                         | NC                      | NC                      |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to stacked x4 PCB symbol.
3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

## Component Details:

## DDR2 SDRAM Fully Buffered DIMM Design Specification

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DL-z, 92 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

x8 Ballout of DDR2 SDRAMs (Top view)

|    | 1   | 2      | 3                      | 7                       | 8                       | 9   |  | 1   | 2                               | 3                               | 7                       | 8                       | 9    |
|----|-----|--------|------------------------|-------------------------|-------------------------|-----|--|-----|---------------------------------|---------------------------------|-------------------------|-------------------------|------|
| A  | NC  | NC     |                        |                         | NC                      | NC  |  | NC  | NC                              |                                 |                         | NC                      | NC   |
| B  |     |        |                        |                         |                         |     |  |     |                                 |                                 |                         |                         |      |
| C  |     |        |                        |                         |                         |     |  |     |                                 |                                 |                         |                         |      |
| D  | VDD | NC     | VSS                    | VSS                     | NC                      | VDD |  | VDD | NC                              | VSS                             | VSS                     | NC                      | VDD  |
| E  | NC  | NC     | NC                     | NC                      | NC                      | NC  |  | NC  | NC                              | NC                              | NC                      | NC                      | NC   |
| F  | NC  | NC     | NC                     | NC                      | NC                      | NC  |  | NC  | NC                              | NC                              | NC                      | NC                      | NC   |
| G  | NC  | NC     | NC                     | NC                      | NC                      | NC  |  | NC  | NC                              | NC                              | NC                      | NC                      | NC   |
| H  | VDD | NC     | VSS                    | VSS                     | $\overline{\text{DQS}}$ | VDD |  | VDD | $\frac{\text{NU}}{\text{RDQS}}$ | VSS                             | VSS                     | $\overline{\text{DQS}}$ | VDDQ |
| J  | NC  | VSS    | DM                     | DQS                     | VSS                     | NC  |  | DQ6 | VSS                             | $\frac{\text{DM}}{\text{RDQS}}$ | DQS                     | VSS                     | DQ7  |
| K  | VDD | DQ1    | VDD                    | VDD                     | DQ0                     | VDD |  | VDD | DQ1                             | VDD                             | VDD                     | DQ0                     | VDD  |
| L  | NC  | VSS    | DQ3                    | DQ2                     | VSS                     | NC  |  | DQ4 | VSSQ                            | DQ3                             | DQ2                     | VSS                     | DQ5  |
| M  | VDD | VREF   | VSS                    | VSS                     | CK                      | VDD |  | VDD | VREF                            | VSS                             | VSS                     | CK                      | VDD  |
| N  |     | CKE    | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT |  |     | CKE                             | $\overline{\text{WE}}$          | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |
| P  | BA2 | BA0    | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |     |  | BA2 | BA0                             | BA1                             | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |
| R  |     | A10/AP | A1                     | A2                      | A0                      | VDD |  |     | A10/AP                          | A1                              | A2                      | A0                      | VDD  |
| T  | VSS | A3     | A5                     | A6                      | A4                      |     |  | VSS | A3                              | A5                              | A6                      | A4                      |      |
| U  |     | A7     | A9                     | A11                     | A8                      | VSS |  |     | A7                              | A9                              | A11                     | A8                      | VSS  |
| V  | VDD | A12    | A14,NC                 | A15,NC                  | A13,NC                  |     |  | VDD | A12                             | A14,NC                          | A15,NC                  | A13,NC                  |      |
| W  |     |        |                        |                         |                         |     |  |     |                                 |                                 |                         |                         |      |
| Y  |     |        |                        |                         |                         |     |  |     |                                 |                                 |                         |                         |      |
| AA | NC  | NC     |                        |                         | NC                      | NC  |  | NC  | NC                              |                                 |                         | NC                      | NC   |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball H2 (NU/RDQS) will be open on the x8 based DIMMs.

## DDR2 SDRAM Fully Buffered DIMM Design Specification

Component Details:

Pin Assignments for Stacked x4 with Support Balls (Top View)

(MO-242 variation AC, 95 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked  
DIMM (Top view)

|    | 1   | 2      | 3                      | 7                       | 8                       | 9                       |
|----|-----|--------|------------------------|-------------------------|-------------------------|-------------------------|
| A  | NC  | NC     |                        |                         | NC                      | NC                      |
| B  |     |        |                        |                         |                         |                         |
| C  |     |        |                        |                         |                         |                         |
| D  | VDD | NC     | VSS                    | VSS                     | NC                      | VDD                     |
| E  | NC  | NC     | NC                     | NC                      | NC                      | NC                      |
| F  | NC  | NC     | NC                     | NC                      | NC                      | NC                      |
| G  | NC  | NC     | NC                     | NC                      | NC                      | NC                      |
| H  | VDD | NC     | VSS                    | VSS                     | $\overline{\text{DQS}}$ | VDD                     |
| J  | NC  | VSS    | DM                     | DQS                     | VSS                     | NC                      |
| K  | VDD | DQ1    | VDD                    | VDD                     | DQ0                     | VDD                     |
| L  | NC  | VSS    | DQ3                    | DQ2                     | VSS                     | NC                      |
| M  | VDD | VREF   | VSS                    | VSS                     | CK                      | VDD                     |
| N  |     | CKE    | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT0                    |
| P  | BA2 | BA0    | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS0}}$ | $\overline{\text{CS1}}$ |
| R  |     | A10/AP | A1                     | A2                      | A0                      | VDD                     |
| T  | VSS | A3     | A5                     | A6                      | A4                      | ODT1                    |
| U  |     | A7     | A9                     | A11                     | A8                      | VSS                     |
| V  | VDD | A12    | A14,NC                 | A15,NC                  | A13,NC                  |                         |
| W  |     |        |                        |                         |                         |                         |
| Y  |     |        |                        |                         |                         |                         |
| AA | NC  | NC     |                        |                         | NC                      | NC                      |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to stacked x4 PCB Symbol.
3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

**Component Details:****DDR2 SDRAM Fully Buffered DIMM Design Specification**

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DK-z, 84 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

x8 Ballout of DDR2 SDRAMs (Top view)

|   | 1   | 2      | 3                      |  | 7                       | 8                       | 9   |
|---|-----|--------|------------------------|--|-------------------------|-------------------------|-----|
|   |     |        |                        |  |                         |                         |     |
|   |     |        |                        |  |                         |                         |     |
|   |     |        |                        |  |                         |                         |     |
| A | VDD | NC     | VSS                    |  | VSS                     | NC                      | VDD |
| B | NC  | NC     | NC                     |  | NC                      | NC                      | NC  |
| C | NC  | NC     | NC                     |  | NC                      | NC                      | NC  |
| D | NC  | NC     | NC                     |  | NC                      | NC                      | NC  |
| E | VDD | NC     | VSS                    |  | VSS                     | $\overline{\text{DQS}}$ | VDD |
| F | NC  | VSS    | DM                     |  | DQS                     | VSS                     | NC  |
| G | VDD | DQ1    | VDD                    |  | VDD                     | DQ0                     | VDD |
| H | NC  | VSS    | DQ3                    |  | DQ2                     | VSS                     | NC  |
| J | VDD | VREF   | VSS                    |  | VSS                     | CK                      | VDD |
| K |     | CKE    | $\overline{\text{WE}}$ |  | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT |
| L | BA2 | BA0    | BA1                    |  | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |     |
| M |     | A10/AP | A1                     |  | A2                      | A0                      | VDD |
| N | VSS | A3     | A5                     |  | A6                      | A4                      |     |
| P |     | A7     | A9                     |  | A11                     | A8                      | VSS |
| R | VDD | A12    | A14,NC                 |  | A15,NC                  | A13,NC                  |     |
|   |     |        |                        |  |                         |                         |     |
|   |     |        |                        |  |                         |                         |     |
|   |     |        |                        |  |                         |                         |     |
|   |     |        |                        |  |                         |                         |     |

|  | 1   | 2                                | 3                                |  | 7                       | 8                       | 9    |
|--|-----|----------------------------------|----------------------------------|--|-------------------------|-------------------------|------|
|  |     |                                  |                                  |  |                         |                         |      |
|  |     |                                  |                                  |  |                         |                         |      |
|  |     |                                  |                                  |  |                         |                         |      |
|  | VDD | NC                               | VSS                              |  | VSS                     | NC                      | VDD  |
|  | NC  | NC                               | NC                               |  | NC                      | NC                      | NC   |
|  | NC  | NC                               | NC                               |  | NC                      | NC                      | NC   |
|  | NC  | NC                               | NC                               |  | NC                      | NC                      | NC   |
|  | VDD | $\frac{\text{NU/}}{\text{RDQS}}$ | VSS                              |  | VSS                     | $\overline{\text{DQS}}$ | VDDQ |
|  | DQ6 | VSS                              | $\frac{\text{DM/}}{\text{RDQS}}$ |  | DQS                     | VSS                     | DQ7  |
|  | VDD | DQ1                              | VDD                              |  | VDD                     | DQ0                     | VDD  |
|  | DQ4 | VSSQ                             | DQ3                              |  | DQ2                     | VSS                     | DQ5  |
|  | VDD | VREF                             | VSS                              |  | VSS                     | CK                      | VDD  |
|  |     | CKE                              | $\overline{\text{WE}}$           |  | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |
|  | BA2 | BA0                              | BA1                              |  | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |
|  |     | A10/AP                           | A1                               |  | A2                      | A0                      | VDD  |
|  | VSS | A3                               | A5                               |  | A6                      | A4                      |      |
|  |     | A7                               | A9                               |  | A11                     | A8                      | VSS  |
|  | VDD | A12                              | A14,NC                           |  | A15,NC                  | A13,NC                  |      |
|  |     |                                  |                                  |  |                         |                         |      |
|  |     |                                  |                                  |  |                         |                         |      |
|  |     |                                  |                                  |  |                         |                         |      |
|  |     |                                  |                                  |  |                         |                         |      |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to x4 and x8 PCB Symbol.
3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball E2 (NU/RDQS) will be open on the x8 based DIMMs.

## DDR2 SDRAM Fully Buffered DIMM Design Specification

Component Details:

## Pin Assignments for Stacked x4 Ballouts with Support Balls (Top View)

(MO-242 variation AD, 87 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked  
DIMM (Top view)

|   | 1   | 2      | 3                      |  | 7                       | 8                       | 9                       |
|---|-----|--------|------------------------|--|-------------------------|-------------------------|-------------------------|
|   |     |        |                        |  |                         |                         |                         |
|   |     |        |                        |  |                         |                         |                         |
|   |     |        |                        |  |                         |                         |                         |
| A | VDD | NC     | VSS                    |  | VSS                     | NC                      | VDD                     |
| B | NC  | NC     | NC                     |  | NC                      | NC                      | NC                      |
| C | NC  | NC     | NC                     |  | NC                      | NC                      | NC                      |
| D | NC  | NC     | NC                     |  | NC                      | NC                      | NC                      |
| E | VDD | NC     | VSS                    |  | VSS                     | $\overline{\text{DQS}}$ | VDD                     |
| F | NC  | VSS    | DM                     |  | DQS                     | VSS                     | NC                      |
| G | VDD | DQ1    | VDD                    |  | VDD                     | DQ0                     | VDD                     |
| H | NC  | VSS    | DQ3                    |  | DQ2                     | VSS                     | NC                      |
| J | VDD | VREF   | VSS                    |  | VSS                     | CK                      | VDD                     |
| K |     | CKE    | $\overline{\text{WE}}$ |  | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT0                    |
| L | BA2 | BA0    | BA1                    |  | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  | $\overline{\text{CS1}}$ |
| M |     | A10/AP | A1                     |  | A2                      | A0                      | VDD                     |
| N | VSS | A3     | A5                     |  | A6                      | A4                      | ODT1                    |
| P |     | A7     | A9                     |  | A11                     | A8                      | VSS                     |
| R | VDD | A12    | A14,NC                 |  | A15,NC                  | A13,NC                  |                         |
|   |     |        |                        |  |                         |                         |                         |
|   |     |        |                        |  |                         |                         |                         |
|   |     |        |                        |  |                         |                         |                         |
|   |     |        |                        |  |                         |                         |                         |

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.
2. Above coordinates of ball out corresponds to stacked x4 PCB Symbol on PCB
3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

## Component Details:

## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Pin Assignments for x4 and x8 PCB Symbol (Top View)

x4 Common Symbol on PCB (Top view)

|    | 1   | 2      | 3                      | 7                       | 8                       | 9   |
|----|-----|--------|------------------------|-------------------------|-------------------------|-----|
| A  | NU  | NU     |                        |                         | NU                      | NU  |
| B  |     |        |                        |                         |                         |     |
| C  |     |        |                        |                         |                         |     |
| D  | VDD | NU     | VSS                    | VSS                     | NU                      | VDD |
| E  | NU  | NU     | NU                     | NU                      | NU                      | NU  |
| F  | NU  | NU     | NU                     | NU                      | NU                      | NU  |
| G  | NU  | NU     | NU                     | NU                      | NU                      | NU  |
| H  | VDD | NU     | VSS                    | VSS                     | $\overline{\text{DQS}}$ | VDD |
| J  | NU  | VSS    | DM                     | DQS                     | VSS                     | NU  |
| K  | VDD | DQ1    | VDD                    | VDD                     | DQ0                     | VDD |
| L  | NU  | VSS    | DQ3                    | DQ2                     | VSS                     | NU  |
| M  | VDD | VREF   | VSS                    | VSS                     | CK                      | VDD |
| N  |     | CKE    | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT |
| P  | BA2 | BA0    | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |     |
| R  |     | A10/AP | A1                     | A2                      | A0                      | VDD |
| T  | VSS | A3     | A5                     | A6                      | A4                      |     |
| U  |     | A7     | A9                     | A11                     | A8                      | VSS |
| V  | VDD | A12    | A14                    | A15                     | A13                     |     |
| W  |     |        |                        |                         |                         |     |
| Y  |     |        |                        |                         |                         |     |
| AA | NU  | NU     |                        |                         | NU                      | NU  |
| AB | NU  | NU     |                        |                         | NU                      | NU  |

x8 Common Symbol on PCB (Top view)

|    | 1   | 2      | 3                      | 7                       | 8                       | 9    |
|----|-----|--------|------------------------|-------------------------|-------------------------|------|
| A  | NU  | NU     |                        |                         | NU                      | NU   |
| B  |     |        |                        |                         |                         |      |
| C  |     |        |                        |                         |                         |      |
| D  | VDD | NU     | VSS                    | VSS                     | NU                      | VDD  |
| E  | NU  | NU     | NU                     | NU                      | NU                      | NU   |
| F  | NU  | NU     | NU                     | NU                      | NU                      | NU   |
| G  | NU  | NU     | NU                     | NU                      | NU                      | NU   |
| H  | VDD | NC     | VSS                    | VSS                     | $\overline{\text{DQS}}$ | VDDQ |
| J  | DQ6 | VSS    | DM/<br>RDQS            | DQS                     | VSS                     | DQ7  |
| K  | VDD | DQ1    | VDD                    | VDD                     | DQ0                     | VDD  |
| L  | DQ4 | VSSQ   | DQ3                    | DQ2                     | VSS                     | DQ5  |
| M  | VDD | VREF   | VSS                    | VSS                     | CK                      | VDD  |
| N  |     | CKE    | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT  |
| P  | BA2 | BA0    | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$  |      |
| R  |     | A10/AP | A1                     | A2                      | A0                      | VDD  |
| T  | VSS | A3     | A5                     | A6                      | A4                      |      |
| U  |     | A7     | A9                     | A11                     | A8                      | VSS  |
| V  | VDD | A12    | A14                    | A15                     | A13                     |      |
| W  |     |        |                        |                         |                         |      |
| Y  |     |        |                        |                         |                         |      |
| AA | NU  | NU     |                        |                         | NU                      | NU   |
| AB | NU  | NU     |                        |                         | NU                      | NU   |

1. Above coordinates of symbol corresponds to x4 and x8 ballouts of the DDR2 SDRAMs.

2. "NC" means that a solder pad is present and is not connected to any signal on the PCB. NC solder pads may be mated with any of the balls of an SDRAM. On the FB-DIMM x8 symbol, only ball H2 is NC.

3. "NU" means that the solder pad is present and may or may not be electrically connected to an active signal on the PCB. NU solder pads may only be mated with the NC ball of an SDRAM. On FB-DIMM, the NU solder pads will be either open, or connected to Vdd/VddQ. The NU pad may be a continuation of a surface plane utilized for power delivery purposes, thus it must only mate to a NC ball on the SDRAM.

## Pin Assignments for Stacked x4 PCB Symbol ( Top View)

## x4 Common Symbol on PCB for Stacked DIMM (Top view)

|    | 1    | 2      | 3                      | 7                       | 8                       | 9                       |
|----|------|--------|------------------------|-------------------------|-------------------------|-------------------------|
| A  | NU   | NU     |                        |                         | NU                      | NU                      |
| B  |      |        |                        |                         |                         |                         |
| C  |      |        |                        |                         |                         |                         |
| D  | VDD  | NU     | VSS                    | VSS                     | NU                      | VDD                     |
| E  | NU   | NU     | NU                     | NU                      | NU                      | NU                      |
| F  | NU   | NU     | NU                     | NU                      | NU                      | NU                      |
| G  | NU   | NU     | NU                     | NU                      | NU                      | NU                      |
| H  | VDD  | NU     | VSS                    | VSS                     | $\overline{\text{DQS}}$ | VDD                     |
| J  | NU   | VSS    | DM                     | DQS                     | VSS                     | NU                      |
| K  | VDD  | DQ1    | VDD                    | VDD                     | DQ0                     | VDD                     |
| L  | NU   | VSS    | DQ3                    | DQ2                     | VSS                     | NU                      |
| M  | VDD  | VREF   | VSS                    | VSS                     | CK                      | VDD                     |
| N  |      | CKE0   | $\overline{\text{WE}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$  | ODT0                    |
| P  | BA2  | BA0    | BA1                    | $\overline{\text{CAS}}$ | $\overline{\text{CS0}}$ | $\overline{\text{CS1}}$ |
| R  | CKE1 | A10/AP | A1                     | A2                      | A0                      | VDD                     |
| T  | VSS  | A3     | A5                     | A6                      | A4                      | ODT1                    |
| U  |      | A7     | A9                     | A11                     | A8                      | VSS                     |
| V  | VDD  | A12    | A14                    | A15                     | A13                     |                         |
| W  |      |        |                        |                         |                         |                         |
| Y  |      |        |                        |                         |                         |                         |
| AA | NU   | NU     |                        |                         | NU                      | NU                      |
| AB | NU   | NU     |                        |                         | NU                      | NU                      |

1. Above coordinates of symbol corresponds to stacked x4 ballout of the DDR2 SDRAMs.

2. "NU" means that the solder pad is present and may or may not be electrically connected to an active signal on the PCB. NU solder pads may only be mated with the NC ball of an SDRAM. On FB-DIMM, the NU solder pads will be either open, or connected to Vdd/VddQ. The NU pad may be a continuation of a surface plane utilized for power delivery purposes, thus it must only mate to a NC ball on the SDRAM.

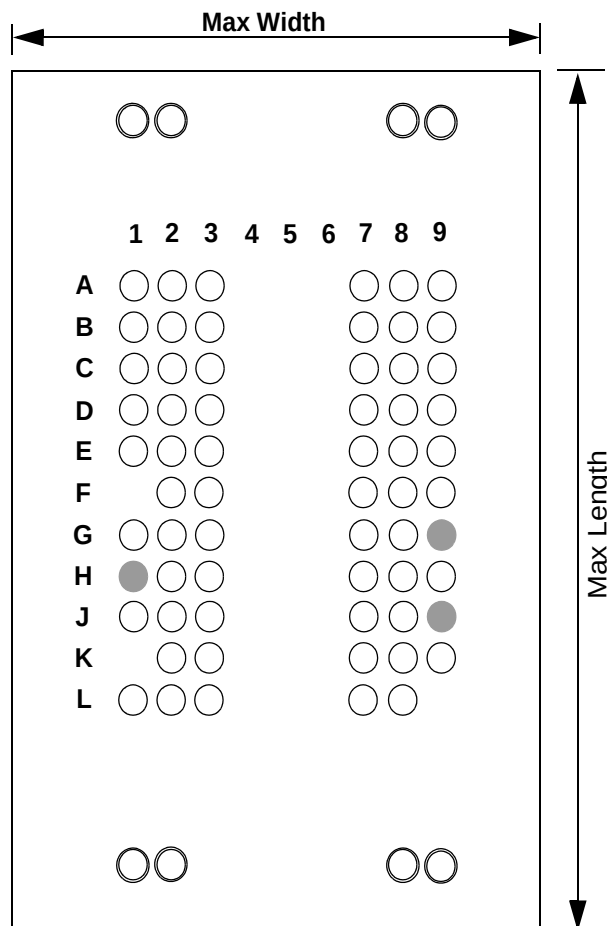
## Component Details

## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Component Details

## Supported SDRAM Component Maximum size for 256Mb to 4Gb, DDR2 SDRAM

| Raw Card                                                                                                                                                                                                                                                                         | Package Type | Supported DRAM Outline (Width x Length) max. (mm) |                                               |                                                            |                                               |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------------------------------------------|-----------------------------------------------|------------------------------------------------------------|-----------------------------------------------|
|                                                                                                                                                                                                                                                                                  |              | MO-207 Variation                                  |                                               |                                                            |                                               |
|                                                                                                                                                                                                                                                                                  |              | DJ-z (60 pins)                                    | DM-z (68 pins)                                | DL-z (92 pins)                                             | DK-z (84 pins)                                |
| A                                                                                                                                                                                                                                                                                | Planar       | 12.4 x 15                                         | 12.4 x 18                                     | 12.4 x 21                                                  | 12.4 x 21                                     |
| B,C                                                                                                                                                                                                                                                                              | Planar       | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 15     | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 18 | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 21 <sup>3</sup> | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 21 |
| E                                                                                                                                                                                                                                                                                | Planar       | 11 x 11.5                                         | --                                            | --                                                         | --                                            |
| H                                                                                                                                                                                                                                                                                | Planar       | 12 <sup>4</sup> x 11                              | --                                            | --                                                         | --                                            |
|                                                                                                                                                                                                                                                                                  |              | MO-242 Variation                                  |                                               |                                                            |                                               |
|                                                                                                                                                                                                                                                                                  |              | AA (63 pins)                                      | AD (71 pins)                                  | AC (95 pins)                                               | AB (87 pins)                                  |
|                                                                                                                                                                                                                                                                                  |              |                                                   |                                               |                                                            |                                               |
| D,J                                                                                                                                                                                                                                                                              | Stacked      | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 15     | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 18 | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 21 <sup>3</sup> | 11.4 <sup>2</sup> (12.4 <sup>1,2</sup> ) x 21 |
| 1. supported only if no-decoupling capacitor are placed in between the DRAMs<br>2. 0.4 mm DRAM to DRAM spacing<br>3 Heat sink attachment may modify the max DRAM length that will fit to 18.6mm<br>4. Heat sink attachment may modify the max DRAM width that will fit to 11.5mm |              |                                                   |                                               |                                                            |                                               |



Note: Double circles indicate the location of support balls of Variation DM-z  
Gray circles indicate the balls for stacked only

## DDR2 SDRAM Fully Buffered DIMM Design Specification

Architecture

## Architecture

## Advanced Memory Buffer Pin Description

| Pin Name                                                    | Pin Description                                                                                                               | Count      |
|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|------------|
| FB-DIMM Channel Signals                                     |                                                                                                                               | <b>99</b>  |
| SCK                                                         | System Clock Input, positive line                                                                                             | 1          |
| $\overline{\text{SCK}}$                                     | System Clock Input, negative line                                                                                             | 1          |
| PN[13:0]                                                    | Primary Northbound Data, positive lines                                                                                       | 14         |
| $\overline{\text{PN}}[13:0]$                                | Primary Northbound Data, negative lines                                                                                       | 14         |
| PS[9:0]                                                     | Primary Southbound Data, positive lines                                                                                       | 10         |
| $\overline{\text{PS}}[9:0]$                                 | Primary Southbound Data, negative lines                                                                                       | 10         |
| SN[13:0]                                                    | Secondary Northbound Data, positive lines                                                                                     | 14         |
| $\overline{\text{SN}}[13:0]$                                | Secondary Northbound Data, negative lines                                                                                     | 14         |
| SS[9:0]                                                     | Secondary Southbound Data, positive lines                                                                                     | 10         |
| $\overline{\text{SS}}[9:0]$                                 | Secondary Southbound Data, negative lines                                                                                     | 10         |
| FBDRES                                                      | To an external precision calibration resistor connected to Vcc                                                                | 1          |
| DDR2 Interface Signals                                      |                                                                                                                               | <b>175</b> |
| DQS[8:0]                                                    | Data Strobes, positive lines                                                                                                  | 9          |
| $\overline{\text{DQS}}[8:0]$                                | Data Strobes, negative lines                                                                                                  | 9          |
| DQS[17:9]/DM[8:0]                                           | Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.                               | 9          |
| $\overline{\text{DQS}}[17:9]$                               | Data Strobes (x4 DRAM only), negative lines                                                                                   | 9          |
| DQ[63:0]                                                    | Data                                                                                                                          | 64         |
| CB[7:0]                                                     | Checkbits                                                                                                                     | 8          |
| A[15:0]A, A[15:0]B                                          | Addresses. A10 is part of the pre-charge command                                                                              | 32         |
| BA[2:0]A, BA[2:0]B                                          | Bank Addresses                                                                                                                | 6          |
| $\overline{\text{RASA}}$ , $\overline{\text{RASB}}$         | Part of command, with $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , and $\overline{\text{CS}}[1:0]$ .                    | 2          |
| $\overline{\text{CASA}}$ , $\overline{\text{CASB}}$         | Part of command, with $\overline{\text{RAS}}$ , $\overline{\text{WE}}$ , and $\overline{\text{CS}}[1:0]$ .                    | 2          |
| $\overline{\text{WEA}}$ , $\overline{\text{WEB}}$           | Part of command, with $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , and $\overline{\text{CS}}[1:0]$ .                   | 2          |
| ODTA, ODTB                                                  | On-die Termination Enable                                                                                                     | 2          |
| CKE[1:0]A, CKE[1:0]B                                        | Clock Enable (one per rank)                                                                                                   | 4          |
| $\overline{\text{CS}}[1:0]A$ , $\overline{\text{CS}}[1:0]B$ | Chip Select (one per rank)                                                                                                    | 4          |
| CLK[3:0]                                                    | CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use. | 4          |
| $\overline{\text{CLK}}[3:0]$                                | Negative lines for CLK[3:0]                                                                                                   | 4          |
| DDRC_C14                                                    | DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.                                                                | 1          |
| DDRC_B18                                                    | DDR Compensation: Resistor connected to common return pin DDRC_C14                                                            | 1          |
| DDRC_C18                                                    | DDR Compensation: Resistor connected to common return pin DDRC_C14                                                            | 1          |
| DDRC_B12                                                    | DDR Compensation: Resistor connected to V <sub>SS</sub>                                                                       | 1          |
| DDRC_C12                                                    | DDR Compensation: Resistor connected to V <sub>DD</sub>                                                                       | 1          |

## Advanced Memory Buffer Pin Description

| SPD Bus Interface Signals                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                        | 5          |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------------|
| SCL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Serial Presence Detect (SPD) Clock Input                                                               | 1          |
| SDA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | SPD Data Input / Output                                                                                | 1          |
| SA[2:0]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | SPD Address Inputs, also used to select the DIMM number in the AMB                                     | 3          |
| Miscellaneous Signals                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                        | 163        |
| PLLTSTO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | PLL Clock Observability Output                                                                         | 1          |
| VCCAPLL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Analog VCC for the PLL. Tied with low pass filter to VCC.                                              | 1          |
| VSSAPLL                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Analog VSS for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM.               | 1          |
| TEST_pin#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Leave floating on the DIMM                                                                             | 6          |
| TESTLO_pin#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Tie to ground on the DIMM <sup>2</sup>                                                                 | 5          |
| BFUNC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Tie to ground to set functionality as "buffer on DIMM."                                                | 1          |
| RESET                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | AMB reset signal                                                                                       | 1          |
| NC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands. | 129        |
| RFU                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Reserved for Future Use                                                                                | 18         |
| Power/Ground Signals                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                        | 213        |
| V <sub>CC</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | AMB Core Power (1.5 Volt)                                                                              | 24         |
| V <sub>CCFBD</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | AMB Channel I/O Power (1.5 Volt)                                                                       | 8          |
| V <sub>DD</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | AMB DRAM I/O Power (1.8 Volt)                                                                          | 24         |
| V <sub>DDSPD</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | SPD Power (3.3 Volt)                                                                                   | 1          |
| V <sub>SS</sub>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Ground                                                                                                 | 156        |
| <b>Total</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                        | <b>655</b> |
| <ol style="list-style-type: none"> <li>1. System Clock Signals SCK and <math>\overline{\text{SCK}}</math> switch at one half the DRAM CK/<math>\overline{\text{CK}}</math> frequency.</li> <li>2. TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes on prototype DIMMs: each pin should have a zero ohm resistor pulldown to ground, and an unpopulated resistor pullup to VCC. These resistors can be replaced on production DIMMs with a direct connection to ground.</li> </ol> |                                                                                                        |            |

## DDR2 SDRAM Fully Buffered DIMM Design Specification

Architecture

## Pin Assignments for the Advanced Memory Buffer (AMB) (Top View)

655-Ball LFBGA 0.8 mm x 0.8 mm pitch [MO-TBD]

## Left Side

|    | 1                         | 2                        | 3                       | 4                        | 5                        | 6                        | 7                         | 8                         | 9                        | 10                       | 11                       | 12                      | 13                       | 14                       | 15                       |
|----|---------------------------|--------------------------|-------------------------|--------------------------|--------------------------|--------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|-------------------------|--------------------------|--------------------------|--------------------------|
| A  |                           |                          | V <sub>SS</sub>         | DQ26                     | DQ12                     | V <sub>DD</sub>          | DQS10                     | DQ13                      | V <sub>DD</sub>          | $\overline{\text{DQS1}}$ | DQ10                     | V <sub>DD</sub>         | TEST                     | V <sub>DD</sub>          | V <sub>DD</sub>          |
| B  |                           | V <sub>DD</sub>          | DQS3                    | $\overline{\text{DQS3}}$ | V <sub>SS</sub>          | DQ14                     | $\overline{\text{DQS10}}$ | V <sub>SS</sub>           | DQ11                     | DQS1                     | V <sub>SS</sub>          | DDRC                    | TESTLO                   | V <sub>DD</sub>          | V <sub>SS</sub>          |
| C  | V <sub>SS</sub>           | DQS2                     | DQ18                    | V <sub>SS</sub>          | DQ4                      | $\overline{\text{DQS9}}$ | V <sub>SS</sub>           | DQ15                      | DQ9                      | V <sub>SS</sub>          | DQ8                      | DDRC                    | V <sub>SS</sub>          | DDRC                     | DQS17                    |
| D  | DQ19                      | $\overline{\text{DQS2}}$ | V <sub>SS</sub>         | DQ16                     | DQ24                     | V <sub>SS</sub>          | DQS9                      | DQ7                       | V <sub>SS</sub>          | DQ3                      | DQS0                     | V <sub>SS</sub>         | $\overline{\text{DQS8}}$ | DQS8                     | V <sub>DD</sub>          |
| E  | DQ21                      | V <sub>SS</sub>          | DQ17                    | DQ29                     | V <sub>SS</sub>          | DQ25                     | DQ6                       | V <sub>SS</sub>           | DQ5                      | DQ1                      | V <sub>SS</sub>          | DQ0                     | CB1                      | V <sub>SS</sub>          | CB2                      |
| F  | V <sub>SS</sub>           | DQ20                     | DQ23                    | V <sub>SS</sub>          | DQ31                     | DQ27                     | V <sub>SS</sub>           | TESTLO                    | TEST                     | V <sub>SS</sub>          | $\overline{\text{DQS0}}$ | DQ2                     | V <sub>DD</sub>          | CB0                      | CB3                      |
| G  | $\overline{\text{DQS11}}$ | DQS11                    | NC                      | NC                       | NC                       | V <sub>SS</sub>          | DQS12                     | $\overline{\text{DQS12}}$ | NC                       | NC                       | NC                       | BFUNC                   | RFU                      | RFU                      | RFU                      |
| H  | DQ22                      | V <sub>SS</sub>          | NC                      | NC                       | NC                       | DQ28                     | DQ30                      | V <sub>SS</sub>           | NC                       | NC                       | NC                       | V <sub>SS</sub>         | V <sub>DD</sub>          | V <sub>SS</sub>          | V <sub>DD</sub>          |
| J  | V <sub>SS</sub>           | CLK2                     | NC                      | NC                       | NC                       | BA1A                     | V <sub>SS</sub>           | CKE1A                     | NC                       | NC                       | NC                       | V <sub>DD</sub>         | V <sub>SS</sub>          | V <sub>DD</sub>          | V <sub>SS</sub>          |
| K  | $\overline{\text{CLK2}}$  | CLK0                     | NC                      | NC                       | NC                       | V <sub>SS</sub>          | $\overline{\text{WEA}}$   | RASA                      | NC                       | NC                       | NC                       | V <sub>SS</sub>         | V <sub>CC</sub>          | V <sub>SS</sub>          | V <sub>CC</sub>          |
| L  | $\overline{\text{CLK0}}$  | V <sub>SS</sub>          | NC                      | NC                       | NC                       | A0A                      | CKE0A                     | V <sub>SS</sub>           | NC                       | NC                       | NC                       | V <sub>CC</sub>         | V <sub>SS</sub>          | V <sub>CC</sub>          | V <sub>SS</sub>          |
| M  | ODT0A                     | RFU                      | NC                      | NC                       | NC                       | $\overline{\text{CASA}}$ | V <sub>SS</sub>           | BA2A                      | NC                       | NC                       | NC                       | V <sub>SS</sub>         | V <sub>CC</sub>          | V <sub>SS</sub>          | V <sub>CC</sub>          |
| N  | $\overline{\text{CS1A}}$  | $\overline{\text{CS0A}}$ | NC                      | NC                       | NC                       | V <sub>SS</sub>          | BA0A                      | A10A                      | NC                       | NC                       | NC                       | V <sub>CC</sub>         | V <sub>SS</sub>          | V <sub>CC</sub>          | V <sub>SS</sub>          |
| P  | A6A                       | V <sub>SS</sub>          | NC                      | NC                       | NC                       | A2A                      | A1A                       | A3A                       | NC                       | NC                       | NC                       | V <sub>SS</sub>         | V <sub>CC</sub>          | V <sub>SS</sub>          | V <sub>CC</sub>          |
| R  | V <sub>SS</sub>           | A8A                      | NC                      | NC                       | NC                       | A11A                     | V <sub>SS</sub>           | A5A                       | NC                       | NC                       | NC                       | V <sub>CC</sub>         | V <sub>SS</sub>          | V <sub>CC</sub>          | V <sub>SS</sub>          |
| T  | A4A                       | A13A                     | NC                      | NC                       | NC                       | V <sub>SS</sub>          | A9A                       | A7A                       | NC                       | NC                       | NC                       | V <sub>SS</sub>         | V <sub>CC</sub>          | V <sub>SS</sub>          | V <sub>CC</sub>          |
| U  | PN0                       | $\overline{\text{PN0}}$  | NC                      | NC                       | NC                       | A15A                     | A14A                      | A12A                      | NC                       | NC                       | NC                       | RFU                     | V <sub>CCFBD</sub>       | V <sub>SS</sub>          | V <sub>SS</sub>          |
| V  | PN1                       | $\overline{\text{PN1}}$  | V <sub>SS</sub>         | SN0                      | $\overline{\text{SN0}}$  | V <sub>CCFBD</sub>       | V <sub>SS</sub>           | V <sub>CCFBD</sub>        | V <sub>SS</sub>          | RFU <sup>a</sup>         | RFU <sup>a</sup>         | V <sub>CCFBD</sub>      | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>          |
| W  | PN2                       | $\overline{\text{PN2}}$  | V <sub>SS</sub>         | SN1                      | $\overline{\text{SN1}}$  | $\overline{\text{SN3}}$  | $\overline{\text{SN4}}$   | $\overline{\text{SN5}}$   | $\overline{\text{SN13}}$ | $\overline{\text{SN12}}$ | $\overline{\text{SN6}}$  | $\overline{\text{SN7}}$ | $\overline{\text{SN8}}$  | $\overline{\text{SN9}}$  | $\overline{\text{SN10}}$ |
| Y  | PN3                       | $\overline{\text{PN3}}$  | V <sub>SS</sub>         | SN2                      | $\overline{\text{SN2}}$  | SN3                      | SN4                       | SN5                       | SN13                     | SN12                     | SN6                      | SN7                     | SN8                      | SN9                      | SN10                     |
| AA | V <sub>SS</sub>           | PN4                      | $\overline{\text{PN4}}$ | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>           | V <sub>SS</sub>           | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>         | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>          |
| AB |                           | V <sub>SS</sub>          | RESET                   | $\overline{\text{PN5}}$  | $\overline{\text{PN13}}$ | RFU <sup>a</sup>         | $\overline{\text{PN12}}$  | $\overline{\text{PN6}}$   | $\overline{\text{PN7}}$  | $\overline{\text{PN8}}$  | $\overline{\text{PN9}}$  | V <sub>SSAPLL</sub>     | V <sub>CCAPLL</sub>      | $\overline{\text{PN10}}$ | $\overline{\text{PN11}}$ |
| AC |                           |                          | V <sub>SS</sub>         | PN5                      | PN13                     | RFU <sup>a</sup>         | PN12                      | PN6                       | PN7                      | PN8                      | PN9                      | FBDRES                  | PLL<br>TSTO              | PN10                     | PN11                     |
|    | 1                         | 2                        | 3                       | 4                        | 5                        | 6                        | 7                         | 8                         | 9                        | 10                       | 11                       | 12                      | 13                       | 14                       | 15                       |

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

## Right Side

|    | 16                        | 17                       | 18                        | 19                      | 20                        | 21                      | 22                       | 23                       | 24                      | 25                      | 26                        | 27                       | 28                        | 29              |
|----|---------------------------|--------------------------|---------------------------|-------------------------|---------------------------|-------------------------|--------------------------|--------------------------|-------------------------|-------------------------|---------------------------|--------------------------|---------------------------|-----------------|
| A  | V <sub>DD</sub>           | TEST                     | V <sub>DD</sub>           | DQ52                    | DQS15                     | V <sub>DD</sub>         | DQ49                     | $\overline{\text{DQS6}}$ | V <sub>DD</sub>         | DQ48                    | DQ38                      | V <sub>DD</sub>          |                           |                 |
| B  | V <sub>DD</sub>           | TEST                     | DDRC                      | V <sub>SS</sub>         | $\overline{\text{DQS15}}$ | DQ53                    | V <sub>SS</sub>          | DQS6                     | DQ50                    | V <sub>SS</sub>         | $\overline{\text{DQS13}}$ | DQS13                    | V <sub>SS</sub>           |                 |
| C  | $\overline{\text{DQS17}}$ | V <sub>SS</sub>          | DDRC                      | DQ54                    | V <sub>SS</sub>           | DQ55                    | DQ51                     | V <sub>SS</sub>          | DQS7                    | DQ56                    | V <sub>SS</sub>           | DQ46                     | $\overline{\text{DQS14}}$ | V <sub>DD</sub> |
| D  | CB6                       | CB7                      | V <sub>SS</sub>           | DQS16                   | DQ63                      | V <sub>SS</sub>         | DQ59                     | $\overline{\text{DQS7}}$ | V <sub>SS</sub>         | DQ36                    | DQ44                      | V <sub>SS</sub>          | DQS14                     | DQ47            |
| E  | V <sub>SS</sub>           | CB5                      | $\overline{\text{DQS16}}$ | V <sub>SS</sub>         | DQ61                      | DQ57                    | V <sub>SS</sub>          | DQ58                     | DQ39                    | V <sub>SS</sub>         | DQ33                      | DQ45                     | V <sub>SS</sub>           | DQ41            |
| F  | CB4                       | V <sub>DD</sub>          | DQ62                      | DQ60                    | V <sub>SS</sub>           | TEST                    | TEST                     | V <sub>SS</sub>          | DQ37                    | DQ35                    | V <sub>SS</sub>           | $\overline{\text{DQS5}}$ | DQ43                      | V <sub>SS</sub> |
| G  | TESTLO                    | RFU                      | RFU                       | NC                      | NC                        | NC                      | DQS4                     | $\overline{\text{DQS4}}$ | V <sub>SS</sub>         | NC                      | NC                        | NC                       | DQS5                      | DQ40            |
| H  | V <sub>SS</sub>           | V <sub>DD</sub>          | V <sub>SS</sub>           | NC                      | NC                        | NC                      | V <sub>SS</sub>          | DQ34                     | DQ32                    | NC                      | NC                        | NC                       | V <sub>SS</sub>           | DQ42            |
| J  | V <sub>DD</sub>           | V <sub>SS</sub>          | V <sub>DD</sub>           | NC                      | NC                        | NC                      | $\overline{\text{RASB}}$ | V <sub>SS</sub>          | RFU                     | NC                      | NC                        | NC                       | $\overline{\text{CLK3}}$  | V <sub>SS</sub> |
| K  | V <sub>SS</sub>           | V <sub>CC</sub>          | V <sub>SS</sub>           | NC                      | NC                        | NC                      | ODT0B                    | $\overline{\text{CS1B}}$ | V <sub>SS</sub>         | NC                      | NC                        | NC                       | $\overline{\text{CLK1}}$  | CLK3            |
| L  | V <sub>CC</sub>           | V <sub>SS</sub>          | V <sub>CC</sub>           | NC                      | NC                        | NC                      | V <sub>SS</sub>          | $\overline{\text{CASB}}$ | $\overline{\text{WEB}}$ | NC                      | NC                        | NC                       | V <sub>SS</sub>           | CLK1            |
| M  | V <sub>SS</sub>           | V <sub>CC</sub>          | V <sub>SS</sub>           | NC                      | NC                        | NC                      | $\overline{\text{CS0B}}$ | V <sub>SS</sub>          | BA1B                    | NC                      | NC                        | NC                       | CKE0B                     | V <sub>SS</sub> |
| N  | V <sub>CC</sub>           | V <sub>SS</sub>          | V <sub>CC</sub>           | NC                      | NC                        | NC                      | A0B                      | A2B                      | V <sub>SS</sub>         | NC                      | NC                        | NC                       | BA0B                      | BA2B            |
| P  | V <sub>SS</sub>           | V <sub>CC</sub>          | V <sub>SS</sub>           | NC                      | NC                        | NC                      | V <sub>SS</sub>          | A4B                      | A1B                     | NC                      | NC                        | NC                       | V <sub>SS</sub>           | CKE1B           |
| R  | V <sub>CC</sub>           | V <sub>SS</sub>          | V <sub>CC</sub>           | NC                      | NC                        | NC                      | A6B                      | V <sub>SS</sub>          | A10B                    | NC                      | NC                        | NC                       | A3B                       | V <sub>SS</sub> |
| T  | V <sub>SS</sub>           | V <sub>CC</sub>          | V <sub>SS</sub>           | NC                      | NC                        | NC                      | A11B                     | A9B                      | V <sub>SS</sub>         | NC                      | NC                        | NC                       | A7B                       | A5B             |
| U  | V <sub>SS</sub>           | V <sub>CCFBD</sub>       | RFU                       | NC                      | NC                        | NC                      | A8B                      | A15B                     | A14B                    | SA0                     | SCL                       | SDA                      | $\overline{\text{PS8}}$   | PS8             |
| V  | V <sub>CCFBD</sub>        | V <sub>SS</sub>          | V <sub>CCFBD</sub>        | V <sub>SS</sub>         | V <sub>CCFBD</sub>        | RFU <sup>a</sup>        | RFU <sup>a</sup>         | V <sub>SS</sub>          | A13B                    | A12 B                   | SA2                       | SA1                      | $\overline{\text{PS7}}$   | PS7             |
| W  | V <sub>SS</sub>           | $\overline{\text{SS0}}$  | $\overline{\text{SS1}}$   | $\overline{\text{SS2}}$ | $\overline{\text{SS3}}$   | $\overline{\text{SS4}}$ | $\overline{\text{SS9}}$  | $\overline{\text{SS5}}$  | $\overline{\text{SS6}}$ | $\overline{\text{SS7}}$ | $\overline{\text{SS8}}$   | V <sub>SS</sub>          | $\overline{\text{PS6}}$   | PS6             |
| Y  | V <sub>SS</sub>           | SS0                      | SS1                       | SS2                     | SS3                       | SS4                     | SS9                      | SS5                      | SS6                     | SS7                     | SS8                       | V <sub>SS</sub>          | $\overline{\text{PS5}}$   | PS5             |
| AA | V <sub>SS</sub>           | V <sub>SS</sub>          | V <sub>SS</sub>           | V <sub>SS</sub>         | V <sub>SS</sub>           | V <sub>SS</sub>         | V <sub>SS</sub>          | V <sub>SS</sub>          | V <sub>SS</sub>         | V <sub>SS</sub>         | V <sub>SS</sub>           | V <sub>SS</sub>          | $\overline{\text{PS9}}$   | PS9             |
| AB | V <sub>SS</sub>           | $\overline{\text{SN11}}$ | V <sub>SS</sub>           | SCK                     | TESTLO                    | $\overline{\text{PS0}}$ | $\overline{\text{PS1}}$  | $\overline{\text{PS2}}$  | $\overline{\text{PS3}}$ | $\overline{\text{PS4}}$ | RFU <sup>a</sup>          | V <sub>DDSPD</sub>       | V <sub>SS</sub>           |                 |
| AC | RFU                       | SN11                     | V <sub>SS</sub>           | $\overline{\text{SCK}}$ | TESTLO                    | PS0                     | PS1                      | PS2                      | PS3                     | PS4                     | RFU <sup>a</sup>          | V <sub>SS</sub>          |                           |                 |
|    | 16                        | 17                       | 18                        | 19                      | 20                        | 21                      | 22                       | 23                       | 24                      | 25                      | 26                        | 27                       | 28                        | 29              |

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Advanced Memory Buffer (AMB) DRAM Interface Specifications

Please refer to the AMB Specification for all technical requirements.

The following specifications for the AMB constitute the subset which is critical for proper operation of the DDR2 SDRAM interface..

## Critical AMB Specifications

| Symbol        | Parameter                                                 | Type   | $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$ |      | Units | Notes |
|---------------|-----------------------------------------------------------|--------|---------------------------------------------|------|-------|-------|
|               |                                                           |        | Min                                         | Max  |       |       |
| $t_{SU}$      | DQ to DQS/ $\overline{DQS}$ setup time (read)             | Input  |                                             | -425 | ps    | 1     |
| $t_H$         | DQ to DQS/ $\overline{DQS}$ hold time (read)              | Input  |                                             | 825  | ps    | 1     |
| $t_{DVBamb}$  | AMB Data Valid Before DQS                                 | Output | 470                                         |      | ps    | 1     |
| $t_{DVAamb}$  | AMB Data Valid After DQS                                  | Output | 470                                         |      | ps    | 1     |
| $t_{CVBamb}$  | C/A/CNTL Valid Before Clock                               | Output | 1030                                        |      | ps    | 1     |
| $t_{CVAamb}$  | C/A/CNTL Valid After Clock                                | Output | 890                                         |      | ps    | 1     |
| $t_{DQSKamb}$ | DQS/ $\overline{DQS}$ -to-CK/ $\overline{CK}$ output skew | Output | -190                                        | 190  | ps    | 1     |
| $C_{IN}$      | Input Capacitance (DQ/DQS/ $\overline{DQS}$ )             |        | 2.0                                         | 2.5  | pF    | 1     |

Note 1: The timing numbers are for example only. Design should be based on the latest AMB component specifications

## AMB Sourcing

This document is not intended to be an approved vendor list for support components. Although it is recommended that all DDR2 SDRAM FBDIMM AMBs meet the specifications documented above, it is up to each DIMM producer to select the AMB and AMB vendors which meet these requirements.

## DDR2 Fully Buffered DIMM Details

### DDR2 SDRAM Module Configurations (Reference Designs)

| Raw Card Version | DIMM     |              | SDRAM   |              | # of SDRAMs | SDRAM Package Type | # of Ranks | # of Banks in SDRAM | # of Address bits row/col/Bank |
|------------------|----------|--------------|---------|--------------|-------------|--------------------|------------|---------------------|--------------------------------|
|                  | Capacity | Organization | Density | Organization |             |                    |            |                     |                                |
| A                | 256MB    | 32Mx72       | 256Mbit | 32Mx8        | 9           | 60 Ball FBGA       | 1          | 4                   | 13/10/2                        |
|                  | 512MB    | 64Mx72       | 512Mbit | 64Mx8        | 9           | 60 Ball FBGA       | 1          | 4                   | 14/10/2                        |
|                  | 1GB      | 128Mx72      | 1Gbit   | 128Mx8       | 9           | 60 Ball FBGA       | 1          | 8                   | 14/10/3                        |
|                  | 2GB      | 256Mx72      | 2Gbit   | 256Mx8       | 9           | 60 Ball FBGA       | 1          | 8                   | 15/10/3                        |
|                  | 4GB      | 512Mx72      | 4Gbit   | 512Mx8       | 9           | 60 Ball FBGA       | 1          | 8                   | 16/10/3                        |
| B                | 512MB    | 64Mx72       | 256Mbit | 32Mx8        | 18          | 60 Ball FBGA       | 2          | 4                   | 13/10/2                        |
|                  | 1GB      | 128Mx72      | 512Mbit | 64Mx8        | 18          | 60 Ball FBGA       | 2          | 4                   | 14/10/2                        |
|                  | 2GB      | 256Mx72      | 1Gbit   | 128Mx8       | 18          | 60 Ball FBGA       | 2          | 8                   | 14/10/3                        |
|                  | 4GB      | 512Mx72      | 2Gbit   | 256Mx8       | 18          | 60 Ball FBGA       | 2          | 8                   | 15/10/3                        |
|                  | 8GB      | 1Gx72        | 4Gbit   | 512Mx8       | 18          | 60 Ball FBGA       | 2          | 8                   | 16/10/3                        |
| C                | 512MB    | 64Mx72       | 256Mbit | 64Mx4        | 18          | 60 Ball FBGA       | 1          | 4                   | 13/11/2                        |
|                  | 1GB      | 128Mx72      | 512Mbit | 128Mx4       | 18          | 60 Ball FBGA       | 1          | 4                   | 14/11/2                        |
|                  | 2GB      | 256Mx72      | 1Gbit   | 256Mx4       | 18          | 60 Ball FBGA       | 1          | 8                   | 14/11/3                        |
|                  | 4GB      | 512Mx72      | 2Gbit   | 512Mx4       | 18          | 60 Ball FBGA       | 1          | 8                   | 15/11/3                        |
|                  | 8GB      | 1Gx72        | 4Gbit   | 1Gbx4        | 18          | 60 Ball FBGA       | 1          | 8                   | 16/11/3                        |
| D, J, E, H       | 1GB      | 64Mx72       | 256Mbit | 64Mx4        | 36          | 63 Ball FBGA       | 2          | 4                   | 13/11/2                        |
|                  | 2GB      | 128Mx72      | 512Mbit | 128Mx4       | 36          | 63 Ball FBGA       | 2          | 4                   | 14/11/2                        |
|                  | 4GB      | 256Mx72      | 1Gbit   | 256Mx4       | 36          | 63 Ball FBGA       | 2          | 8                   | 14/11/3                        |
|                  | 8GB      | 512Mx72      | 2Gbit   | 512Mx4       | 36          | 63 Ball FBGA       | 2          | 8                   | 15/11/3                        |
|                  | 16GB     | 1Gx72        | 4Gbit   | 1Gbx4        | 36          | 63 Ball FBGA       | 2          | 8                   | 16/11/3                        |

### DDR2 Fully Buffered DIMM Design File Releases

'Reference' design file updates will be released as needed. This Fully Buffered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated. The following table outlines the most recent design file releases.

| Raw Card Version | Specification Revision | Applicable Design File | Notes |
|------------------|------------------------|------------------------|-------|
| A                | 0.5                    | TBD                    | TBD   |
| B                | 0.5                    | TBD                    | TBD   |
| C                | 0.4                    | TBD                    | TBD   |
| D                | 0.4                    | TBD                    | TBD   |
| E                | 0.41                   | TBD                    | TBD   |
| H                | 0.5                    | TBD                    | TBD   |

| Raw Card Version | Specification Revision | Applicable Design File | Notes |
|------------------|------------------------|------------------------|-------|
| J                | 0.3                    | TBD                    | TBD   |

## DDR2 SDRAM Fully Buffered DIMM Design Specification

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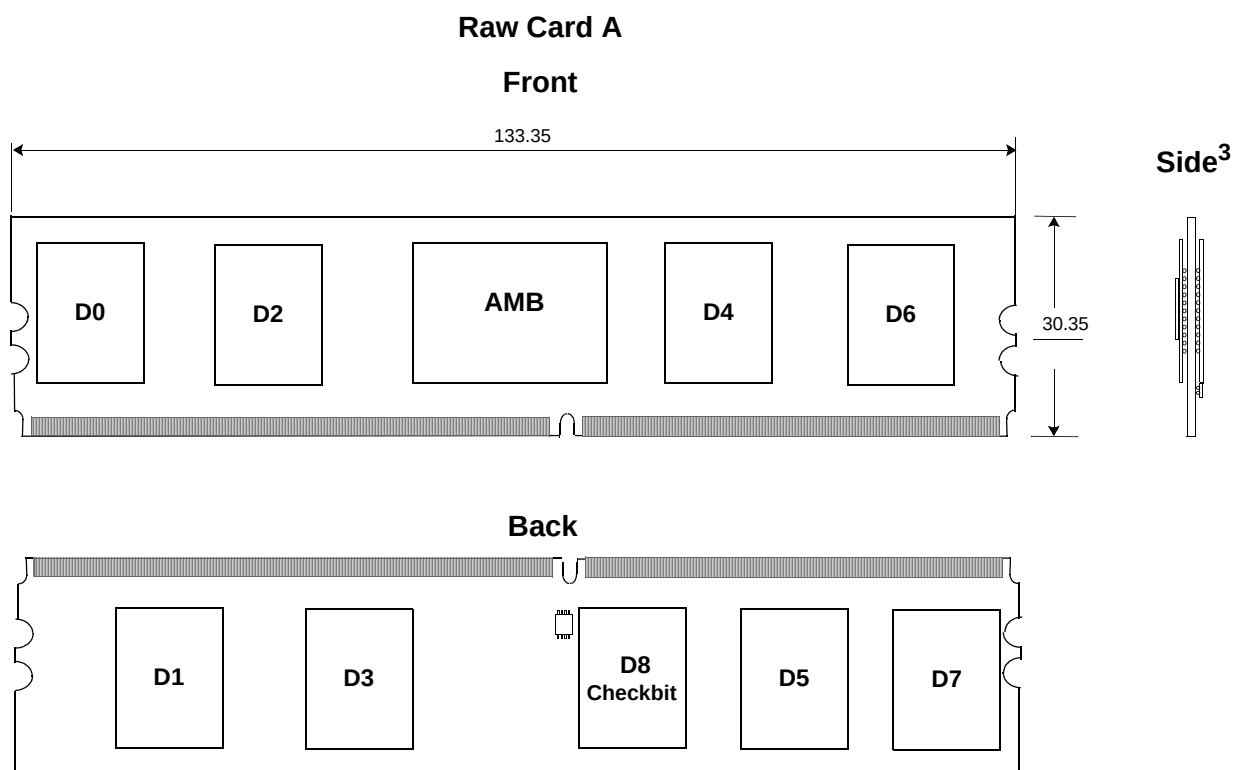
### Component Types and Placement

Components shall be surface mounted on one or both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR2 SDRAM devices must be located near the device power pins.

The following layouts suggest placement for the Raw Cards. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

This example is for reference only; please refer to JEDEC standard MO-256 for details.

## DDR2 SDRAM Fully Buffered DIMM Design Specification



**Note 1:** All dimensions (in mm) are typical unless otherwise stated.

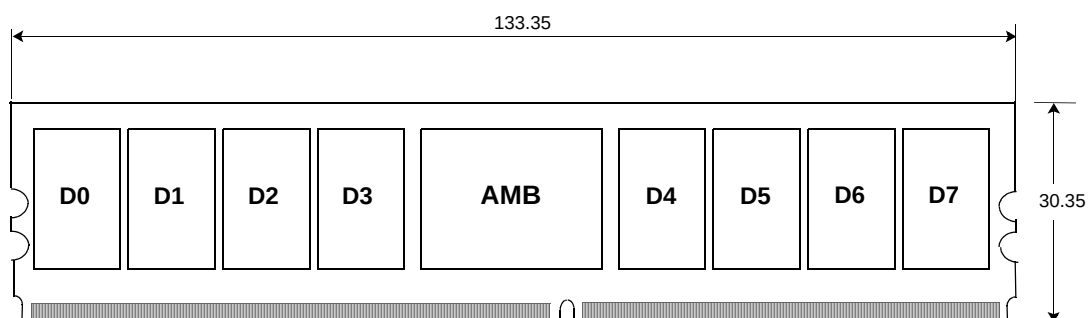
**Note 2:** Support for 16.5 mm wide by 21.9 mm tall DRAM footprint.

**Note 3:** Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

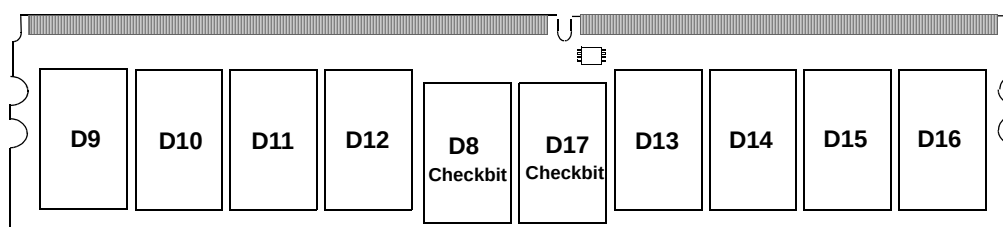
## DDR2 SDRAM Fully Buffered DIMM Design Specification

## Raw Cards B and C

## Front



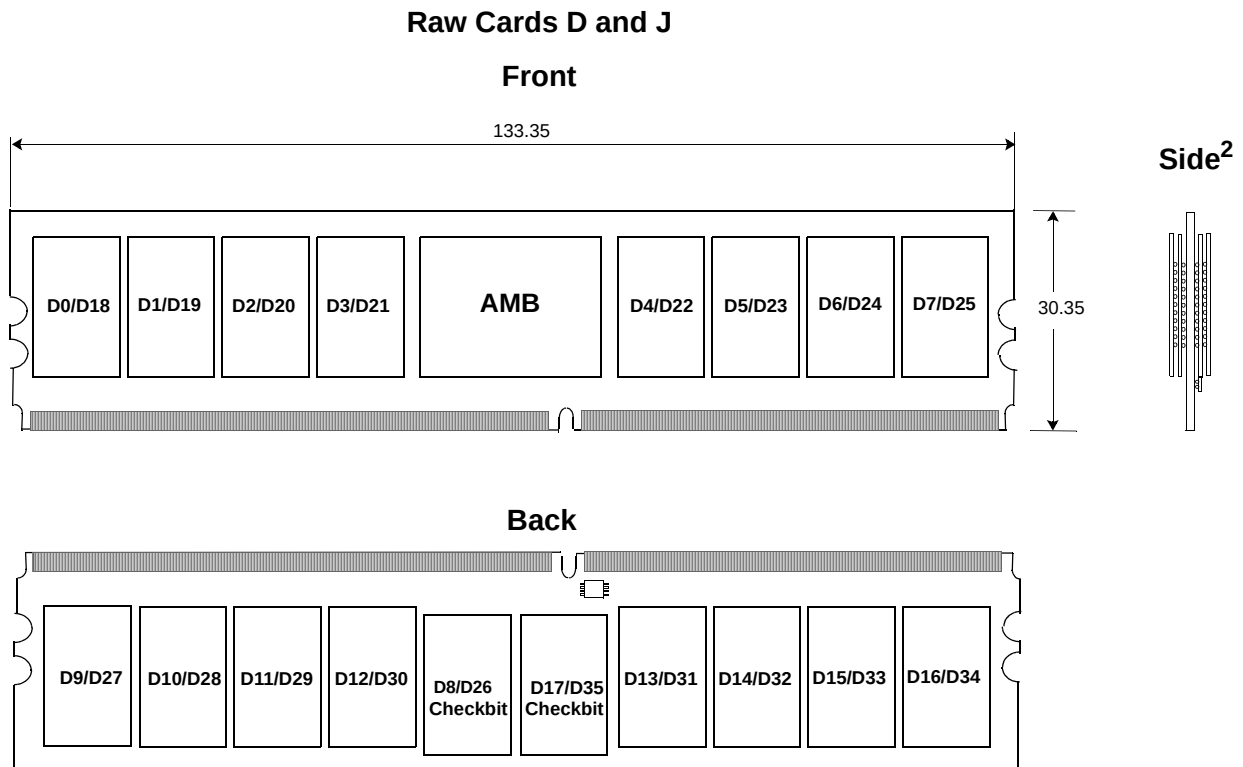
## Back

Side<sup>2</sup>

**Note 1:** All dimensions (in mm) are typical unless otherwise stated.

**Note 2:** Heat Spreader Assembly not shown,  
refer to MO-256 for thickness dimensions.

## DDR2 SDRAM Fully Buffered DIMM Design Specification



**Note 1:** All dimensions (in mm) are typical unless otherwise stated.

**Note 2:** Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.