

JEDEC STANDARD

FBDIMM: Architecture and Protocol

JESD206.01

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FBDIMM: Architecture and Protocol

(From JEDEC Board Ballot, JCB-06-49, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Document Organization

The next four chapters of the FBD Channel Specification cover Channel Overview (Chapter 2), Initialization (Chapter 3), Channel Protocol (Chapter 4) and Reliability, Availability, and Serviceability (RAS) (Chapter 5).

1.1 List of Terms and Abbreviations

This document uses the following terms and abbreviations:

Note that the terms chipset and memory controller are used interchangeably throughout the rest of this document. The term motherboard is used as a generic term to describe the PCB onto which the memory controller is mounted. Actual implementations could have distributed memory controllers mounted on separate memory boards.

Table 1-1 — Terms and Definitions

TERM	Definition
AMB	Advanced Memory Buffer
Chip disable	An ECC encoding specifically tailored for memory such that the data from any defective memory device can be reconstructed from some aggregate of surviving memory devices. Corrects data from failed device.
Bit Lane	A differential pair of signals in one direction.
D+ and D-	The D+ and D- terms used in this document are used to indicate the two conductors or signals of a differential signaling pair.
DDR	Double Data Rate (SDRAM)
DDR Branch	The minimum aggregation of DDR channels which operate in lock-step to support error correction. Two channels per branch supports x8 chip disable ECC. A rank spans a branch.
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an addr/cntrl channel
DDR Data channel	A DDR data channel consists of 72 bits of data, divided into 18 data groups
DDR Data group	Each data group consists of 4 data signals and a differential strobe pair
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR Channel.
DIMM Stack	Dual-ranked x4 DRAM DIMM physical topology: refers to two physical rows of DRAM “stacked” one above another
DRAM Page (Row)	The DRAM cells selected by the Row Address
DPM	Defects per million
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code.
EMI	Electro-magnetic interference
FBD	Fully Buffered DIMM

Table 1-1 — Terms and Definitions (Cont'd)

TERM	Definition
Frame	Group of bits containing commands or data
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBD channel
ISI	Inter Symbol Interference
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, DDR SDRAM Specification
Link	A dual-simplex communications path between two components. The collection of two Ports and their interconnecting bit lanes.
Mesochronous	Same frequency with unknown (but fixed) phase relation.
NB	Northbound
Northbound	The direction of signals running from the farthest DIMM toward the host.
Page Replace a.k.a. Page Miss, Row Hit / Page Miss	An access to a row that has another page open. The page must be transferred back from the sense amps to the array, and the bank must be pre-charged.
Page Hit	An access to an open page, or DRAM row. The data can be supplied from the sense amps at low latency.
Page Miss (Empty Page)	An access to a page that is not buffered in sense amps and must be fetched from DRAM array.
PLL	Phase Locked Loop
Port	In physical terms, a group of transmitters and receivers physically located on the same chip that define one end of a Link.
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one or two physical sets of memory, called ranks. Note that single rank or dual rank is different from single-sided or double-sided, e.g. a single rank DIMM build from x4 DRAM devices is actually double-sided. It is also common practice to distribute the 9 devices of an x8 DIMM between both sides of the DIMM to enhance the thermal performance of the module.
Resample	A resampler repeater is a serial data in and serial data out node that attenuates jitter by re-generating the serial data using a clock recovered from the incoming data stream derived from a common reference clock. It also resets the voltage budget of the re-transmitted data.
Resync	A resync repeater is a serial data in and serial data out node that re-synchronizes data to a local clock after it has been sampled with a recovered clock derived from a common reference clock. The local clock is also generated from the same reference clock by a PLL multiplier. A drift compensation buffer is inserted between the two clock domains which absorbs the maximum link delay change over worst case voltage and temperature changes. Both the jitter and voltage budgets for the re-transmitted data are reset.
RPD	Return Path Discontinuity
SB	Southbound
SDRAM	Synchronous Dynamic Random Access Memory
SI	Signal Integrity
Serial Present Detect (aka SMBus protocol)	A 2-signal serial bus used to read and write control registers in the AMB and SDRAM

Table 1-1 — Terms and Definitions (Cont'd)

TERM	Definition
SMBus	System Management Bus. Controlled by a system management controller to read and write configuration registers. Limited to 100KHz.
Southbound	The direction of signals running from the host controller toward the DIMMs.
SSC	Spread Spectrum Clocking. Utilized to lower EMI
SSO	Simultaneously Switching Outputs
SSTL_18	Series Stub Terminated Logic for 1.8V
Throttled	Temporarily prohibiting memory accesses when a thermal or electrical limit has been reached.
Unit Interval	Average time interval between voltage transitions of a signal
Vss	Ground (0V)
Vddq	I/O buffer voltage for DDR-II buffers. Nominally 1.8V

1.2 Revision History

This document has been released in the following revisions:

Table 1-2 — Revision History

Version	Date	Changes
0.0	12/3/2003	Original revision
0.1	2/13/2004	Revision of all chapters to incorporate feedback
0.1a	5/3/2004	Added JEDEC Ballot Comments 2.1.3: added detail to SMBus addressing 3. Increased calibration time 3.1.2: added detail on determining clock train violaiton 3.3.3: Tx termination to remain on in disable state 3.3.3: Clarified disable state actions by reording table 3-8 3.3.4 & 3.3.5: Command to data fraction delay added in. 3.3.5 & 3.3.7: AMB with Last_AMB flag set loops back data 3.3.6: specified host operation in sending TS2 patterns 3.3.6: Clarified Mege_Disable bit funtionality 3.3.9.1: De-Emphasis disabled during calibrate 4.2.5 Table 4-41: corrected ERC and EL0s duration
	3/16/2005	Added Editorial changes from September 2004 JEDEC meeting Added Ballot changes from March 2005 JEDEC meeting

1.3 Related Documents

Table 1-3 — Related Documents

Document	Revision	Description
FBD Connector Specification	Na	Connector physical parameters: pinout, footprint, mechanical drawing, and requirements
FBD Signaling Specification		PTP link parameters: signaling, I/O, and AC and DC parameters
FBD AMB Specification	Na	AMB Characteristics: pinout, package type, mechanical outline, footprint, AC/DC specs, power/thermal requirements, buffer TPT, special feature requirements (e.g. thermal sensor), & basics DFT
FBD DIMM Specification	Na	FBD DIMM module parameters: multiple raw card designs, block diagrams, net topologies, routing details, timing budget, pin out, mech. Outline, stack up, and SPD requirements
SMBus	2.0	System Management Bus Specification http://smbus.org/specs/smbus20.pdf
DDRII JEDEC Spec		JEDEC DDR II SDRAM Data Sheet JC-42.3

2 Fully Buffered DIMM Overview

Higher CPU speeds are driving the need for higher memory bandwidth. Looking beyond DDR2-533, the existing “stub bus” architecture becomes unworkable. The number of DRAM devices per channel has been trending toward fewer devices per channel. This reduction in capacity reduces performance. Platform cost restrictions limit DRAM pin count increases, routing restrictions limits adding channels to maintain capacity, and differing DRAM interfaces require unique motherboard developments and products.

Fully Buffered DIMM (FBD) addresses these requirements by providing a high-bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM that creates a pay-as-you-go cost structure. Memory device capacity remains high and total memory capacity scales with DRAM bit density.

This chapter describes the FBD Channel topology, physical signaling, clocking and data flow.

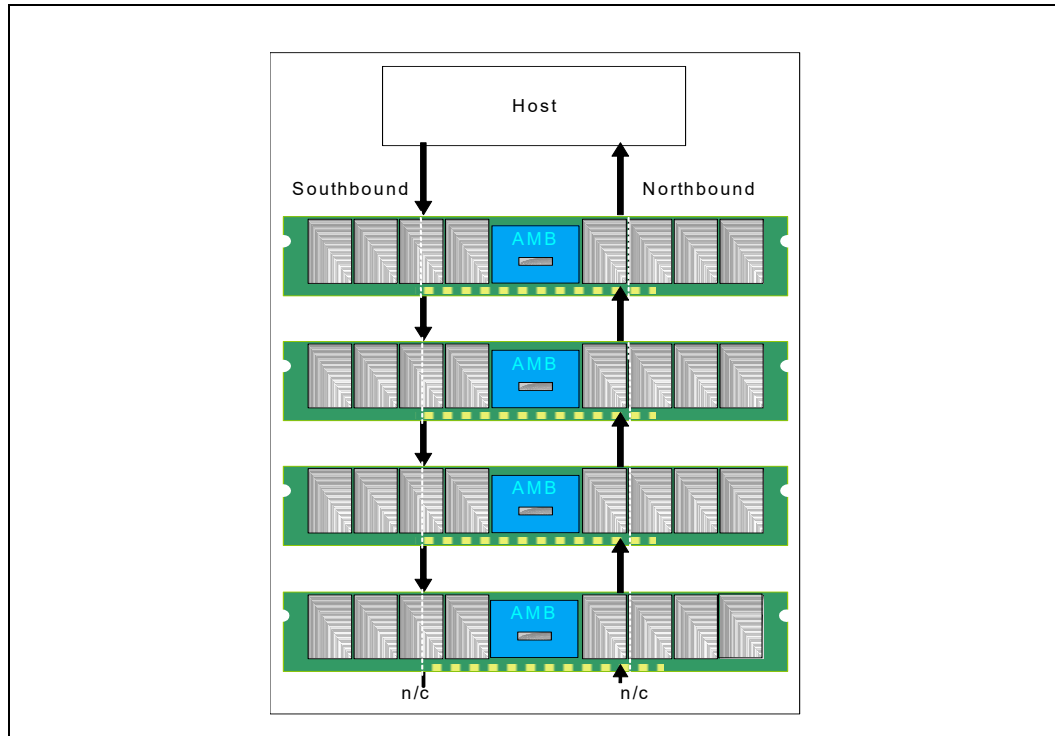
2.1 Memory Channel

The FBD channel provides a communication path from a host controller to an array of DRAM devices. The DRAM devices are buffered behind one or more Advanced Memory Buffer (AMB) devices. The physical isolation of the DRAM devices from the channel enables the flexibility to enhance the communication path to significantly increase the reliability and availability of the memory subsystem.

2.1.1 Link Widths

Figure 2-1 shows a logical diagram of the FBD channel’s southbound and northbound data paths. The channel interconnect actually consists of two unidirectional links: one in the southbound direction and the other in the northbound direction. The southbound data path running from the host to the DIMMs is 10 logical signals wide, and the northbound data path running from the DIMMs back to the host is 14, 13, or 12 logical signals wide. The width of the northbound link is application dependent. The host may support the link width or widths needed to provide the appropriate error detection coverage needed for the intended application. An AMB device on a non-ECC DIMM must support the 12 logical signal width. An AMB device on an ECC DIMM must support the 13 and 14 bit widths.

The southbound link may be operated in fail-over mode to map out a bad bit lane if supported by the host. The 14 or 13 bit width northbound link may be operated in fail-over mode to map out a bad bit lane if supported by the host. An AMB is required to support fail-over on the southbound link, and is required to support fail-over on the northbound link if ECC mode is supported (14 and 13 bit widths).

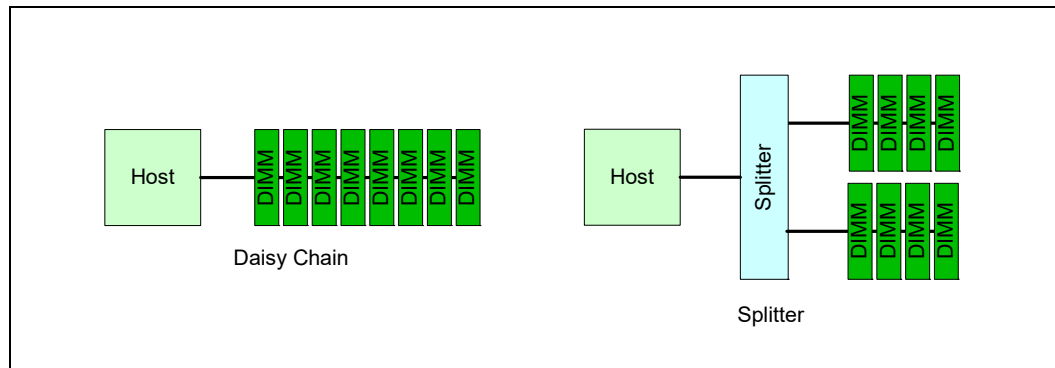
Figure 2-1 — FBD Channel Southbound and Northbound Paths

2.1.2 Topologies

The FBD channel uses a daisy-chain topology to provide expansion from a single DIMM per channel to up to 8 DIMMs per channel. The host sends data on the southbound link to the first DIMM where it is received and re-driven to the second DIMM. On the southbound data path each DIMM receives the data and again re-drives the data to the next DIMM until the last DIMM receives the data. The last DIMM in the chain initiates the transmission of data in the direction of the host (a.k.a. northbound). On the northbound data path each DIMM receives the data and re-drives the data to the next DIMM until the host is reached.

More than 8 buffer devices may be located on a channel. Up to 8 of these may be DRAM DIMMs and the remainder may be repeaters, splitters, or logic analyzer buffers. Figure 2-2 shows two possible topologies that could be supported by FBD. The Daisy Chain topology has the lowest initial cost but latency to the last DIMM is longer than in the splitter topology. The splitter topology has higher initial latency and cost but provides lower latency when fully populated. While a splitter device is theoretically possible, this specification does not define the mechanisms needed to support a splitter.

Figure 2-2 — Sample FBD Channel Topologies



2.1.3 AMB Addressing

Each AMB on the channel must have a unique identity to be addressable by the system. The four SA[3:0] signal pins on the AMB determines its function and address. Table 2-4 defines the function of the AMB based upon the value on the SA[3:0] selection pins. The most significant pins determine if the AMB is mapped into the address space as a DRAM buffer, a repeater, or a Logic Analyzer Interface Buffer. For DIMM modules the value on the lower 3 pins is determined by the value on the corresponding SA[2:0] DIMM connector pins. These are shared with the Serial Presence Detect EEPROM and give the AMB and the EPROM unique SMBus addresses. The SA[3:0] pins also indicate to the AMBs which DIMM Select (DS [3:0] field) they should respond to during FBD DRAM and Channel commands. Only the DRAM buffers and the repeaters are addressable on the FBD channel, the Logic Analyzer Interface buffers are only addressable through the SMBus. The DS[3:0] field in FBD commands is not used by the Logic Analyzer Interface buffers and this allows the DS[3:0] value of 0Fh to be used as a broadcast address to all DRAM DIMM and Repeater AMBs on the channel for Write Config Reg commands.

Table 2-4 — AMB Addressing

AMB BFUNC pin	AMB SA[2:0] pins	DIMM SA[2:0] pins	SMBus Type/ Addr	DS[3:0] command field	Status Return Lane	AMB Function
0	000	000	B0h / B1h	0	0	DRAM DIMM 0
0	001	001	B2h / B3h	1	1	DRAM DIMM 1
0	010	010	B4h / B5h	2	2	DRAM DIMM 2
0	011	011	B6h / B7h	3	3	DRAM DIMM 3
0	100	100	B8h / B9h	4	4	DRAM DIMM 4
0	101	101	BAh / BBh	5	5	DRAM DIMM 5
0	110	110	BCh / BDh	6	6	DRAM DIMM 6
0	111	111	BEh / BFh	7	7	DRAM DIMM 7
1	000	n/a	30h / 31h	8	8	Repeater 0
1	001	n/a	32h / 33h	9	9	Repeater 1
1	010	n/a	34h / 35h	A	10	Repeater 2
1	011	n/a	36h / 37h	B	11	Repeater 3
1	100	n/a	38h / 39h	n/a	none	Logic Analyzer Interface 0
1	101	n/a	3Ah / 3Bh	n/a	none	Logic Analyzer Interface 1
1	110	n/a	3Ch / 3Dh	n/a	none	Logic Analyzer Interface 2
1	111	n/a	3Eh / 3Fh	n/a	none	Logic Analyzer Interface 3

The SMBus Type/Addr column is shown with the Read/Write bit included as the LSB. It is constructed as: {[!BFUNC],[DEV TYPE],SA[2:0],RW} where BFUNC is 0 on DRAM buffers and 1 on repeaters and logic analyzer interfaces. DEV TYPE is three bit field defined to be 3b011 for buffer (AMB) devices. RW is the read/write bit.

Note that DRAM commands on the channel only specify DS[2:0] since only AMB addresses 0 through 7 are used as DIMMs. DS[3] is assumed to be 0 for these commands. The Write Config Reg and Read Config Reg commands specify DS[3:0]

The Status Return Lane is the northbound lane onto which the AMB will merge its data during a Status Frame, which is in response to a southbound Sync Frame.

By convention the AMB addresses increase the farther away from the host the AMB is located on the channel. System firmware may be simplified if the system vendor adheres to this convention.

2.1.4 SMBus Interface

Each AMB on the channel must have an SMBus controller. The SMBus controller in each AMB is a target only controller and is used by the system as an out-of-band access path to the configuration registers. This out-of-band path is available to the system to set initialization parameters, to facilitate AMB/DIMM testing, and provide enhanced fault isolation. Conflicts between in-band and out-of-band accesses to configuration registers must be avoided at the system level.

2.2 Physical Layer

The physical layer of the FBD channel uses high-speed point-to-point links. The signaling is dual simplex, allowing simultaneous data communications in both directions, over low-voltage differential pairs. This section gives a short overview of the FBD channel physical layer. For details refer to the *FBD Signaling Specification*.

Table 2-2 shows the total number of high-speed signals and the corresponding number of physical pins required for the full 14-bit northbound FBD port option on the FBD DIMM. As the signals are differential each high-speed signal requires two pins. The high-speed signals include the 10 southbound signal pairs that carry command, address, data and CRC, and the 14 northbound signal pairs that carry status, data and CRC. In addition there is one signal pair in each direction reserved for future use as forwarded clocks. This makes the total number of high-speed signals equal to 52 per port on the FBD DIMM.

In addition to the high-speed FBD channel signals, each FBD channel agent receives a pair of differential reference clock signals from a common clock source. Each AMB must also support an SMBus port.

Table 2-5 — FBD DIMM Port High-Speed Signal Pin Count (Full 14-bit NB Option)

	Southbound		Northbound	
	Signals	Pins	Signals	Pins
Data path	10	20	14	28
Spare pins for forwarded clocks ^a	1	2	1	2
Total high speed channel pins	52			

- a. The current FBD physical layer does not utilize forwarded clocks. To allow the potential use of forwarded clocks in a future version of the FBD physical layer, pins at the FBD DIMM connector are held in reserve for that purpose.

2.3 Clocking

This chapter describes the FBD channel clocking architecture. The two main aspects of clocking are clock distribution and data sampling at the input receivers.

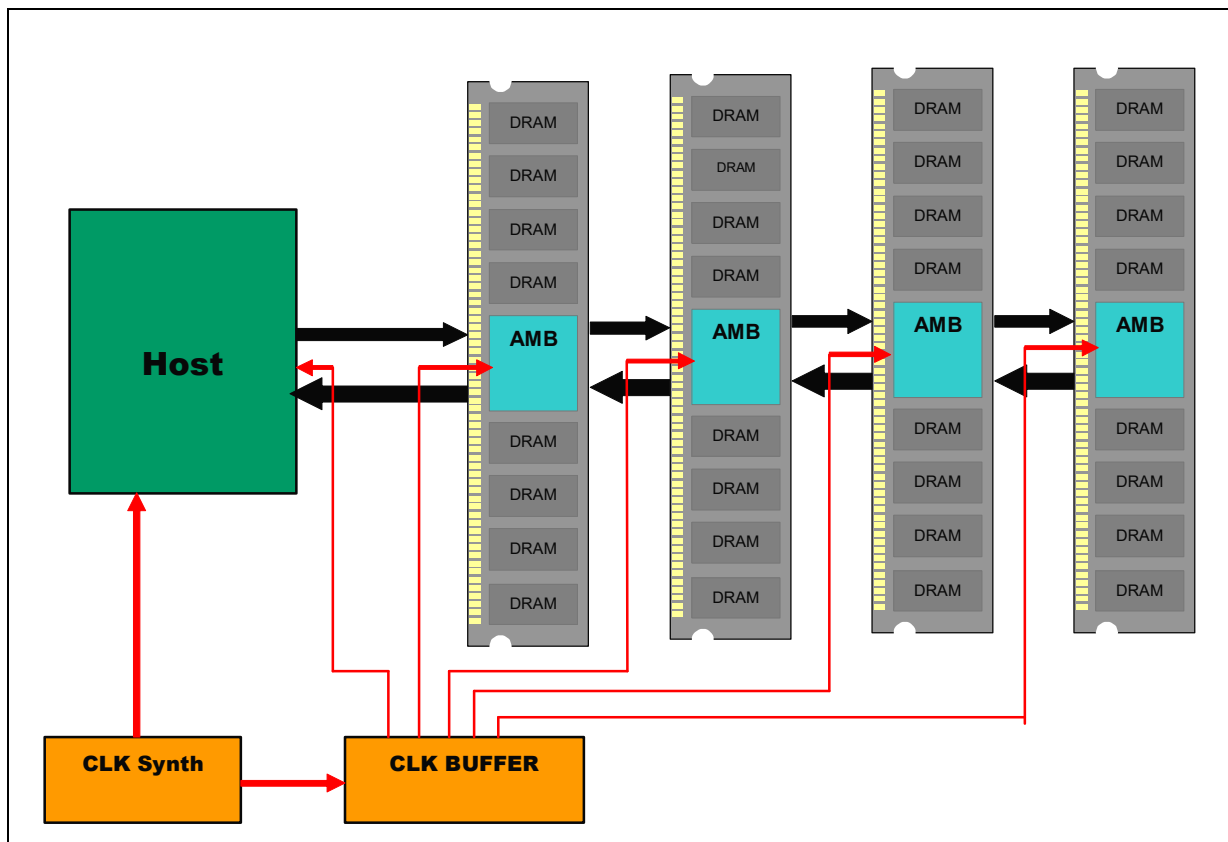
2.3.1 Clock Distribution

A low-jitter reference clock is routed to the host and each AMB from a common clock source on the system board. The reference clock is used to generate the internal buffer clocks and the clocks to the DRAMs located on each DIMM. The frequency of the reference clocks is equal to the DRAM base clock divided by two. For example for DDR2-667 DRAM devices the reference clock frequency would be 166.67 MHz. The reference clocks to the host and each AMB do not have any fixed phase relationship to each other thus simplifying PCB routing since no length matching is required. It is required that all the reference clocks for a given FBD channel originate from a single clock source, e.g. a common clock synthesizer or clock oscillator, thereby ensuring that there is no frequency mismatch or frequency drift between FBD agents. It is a requirement for the FBD channel to operate in the presence of Spread Spectrum Clocking (SSC), which is commonly used to reduce EMI.

The requirements of the reference clock are defined in the *FBD Signaling Specification*.

Figure 2-3 shows a generic example of a clock distribution for a simple single channel FBD platform. The reference clocks for the FBD memory subsystem are generated by the same low-cost CMOS clock components used with non-FBD systems.

Figure 2-3 — Clock Distribution Block Diagram



2.3.2 Receiver Data Sampling

In order to capture the channel data, an FBD agent needs to generate receiver sampling clocks that have a known phase relationship with the received data. FBD allows significant variation in the length of each data bit lane to simplify the channel routing and minimize the length of the longest bit lane. Because of this bit lane skew each receiver needs to 'derive' its own sampling clock from the data stream. A synchronous reference clock is provided that may be used to generate these receiver sampling clocks. A future version of the FBD channel may use forwarded clocks to derive the receiver sampling clocks.

To keep the sampling clock at the receiver in sync with the received data stream without adding the latency of traditional 8b/10b encoding, the FBD physical layer will use dynamic training to track the data. This dynamic training requires a minimum edge density on the bit lanes. To guarantee this edge density in the face of worst-case data patterns the host must periodically send training frames onto the southbound channel. The south most DIMM will correspondingly generate training frames onto the northbound channel to guarantee the required edge density. A density of 6 transitions within 512 transfers or unit intervals (UI) on the channel is required for clock training.

2.3.3 Voltage Temperature Compensation FIFO

The data received on each bit lane is deskewed and passed into the core clock domain of the AMB. The core clock domain generates the clock reference to the DRAM devices and this clock is not adjusted following channel initialization. The timing of data received on each bit lane may drift relative to the core clock domain and a voltage temperature compensation FIFO (VT FIFO) is required to compensate for this drift. The FIFO is pre loaded with a few data bits during channel initialization. The number of buffered data bits in the VT FIFO varies during channel operation to compensate for temperature and voltage changes.

2.3.4 Daisy-Chain Retiming and Data Merge

For a low-latency memory channel it is critical that each data bit is received by the AMB and re-driven to the next AMB or host with minimum delay. The receiver and driver in this critical path are located inside the AMB IO Cell to minimize the delay through the AMB. Every AMB on the channel receives the data from the host even if the data is intended for an upstream AMB. The quality of the signal received by the AMB IO Cell has been degraded by channel distortion and must be re-clocked before it is sent to the next DIMM. The signal is sampled by the receive latch within a very narrow setup/hold timing window and immediately driven out with a clean open data eye. No bit lane de-skew operation is performed during each daisy-chain re-drive. Bit lane skew is allowed to accumulate as the data is sent from AMB to AMB. Latency through the AMB is significantly reduced by not performing a bit lane de-skew operation in each hop. Each AMB or the host receives the data from all of the bit lanes and performs a bit lane de-skew operation before using the data.

The northbound channel has the unique requirement that data from the intermediate DIMMs must be merged into the northbound data stream in such a way as to not introduce any bit-to-bit jitter between the data supplied from the different DIMM. This is done by a well timed multiplexer in the receiver-to-driver signal path and a common transmitter flip-flop. When the AMB logic determines that it is to supply read data on the link, it aligns the data with the northbound frame and signals the AMB IO Cell to multiplex the data into the data stream. The high-speed circuits to switch the multiplexer between the received data comparator and the data serializer are located in the AMB IO Cell. Data is always merged on frame boundaries.

2.3.5 DRAM Clock Generation

The DRAM data interface clock on each DIMM is generated internal to the AMB as a 2x multiple of the reference clock.

2.3.6 DRAM Data Return

The DRAM devices are programmed to return a burst of data on the DRAM data lines a specific number of clocks following a Read Command. The AMB receives the data along with data strobe signals from each DRAM device and captures the data into a data receive latch. The AMB drives the read data onto the northbound channel. The read data propagates through the northbound daisy chain to reach the host. From the host's point of view the sequence of commands it sends to the DRAM and the time slot (frame) that the data arrives back at the host is deterministic. The host performs a training sequence during initialization to determine the number of DRAM base clocks in the round trip. The host may internally delay the received read data to align the data to the internal host core clock.

Intermediate DIMMs must time driving their read data onto the northbound channel to align with the frame timing of the data from the farthest DIMM. Each AMB contains a read data FIFO that is adjusted by logic in the AMB to delay the local read data the appropriate amount. The exact implementation of this logic is design specific. The added delay through the FIFO on the southernmost (last) DIMM is normally set to zero by the host. The delay through the FIFO on the last DIMM may be set to a non-zero value to accommodate a slower FBD DIMM in between the last DIMM and the host.

The channel may be initialized so that the host will receive the DRAM read data returned from any of the DIMMs on a channel arrive back at the host after the same number of DRAM base clocks. A Variable Read Latency capability is also supported which allows the DRAM data from DIMMs closer to the host to be returned earlier than DRAM data returned from the last DIMM. The host will see the round trip flight time from command to data change slightly as the dynamic tracking mechanism adjusts for thermal and voltage drift. A drift compensation FIFO may eliminate this.

2.4 Host Memory Interface

The Host Memory Interface (HMI) is a hypothetical subsystem used as a framework to define the host functions. The FBD Architecture Specification does not require an actual FBD memory interface to be implemented as described in this chapter.

The HMI is the controller agent on the FBD channel and is responsible for initiating and tracking all FBD channel commands. The HMI interfaces the FBD channel to the Host Logic.

The HMI may implement a memory mapped IO mechanism or implement the conventional CFC/CF8 I/O space-based mechanism (or both) for accessing the AMB configuration registers. The HMI generates Channel commands on the FBD channel to access registers in the AMB devices.

The HMI may implement a write queue structure to track write transactions until status information from the AMBs indicate the write operations completed successful. The main purpose of the HMI write buffer is to hold onto the write data for multiple outstanding write operations in case of an error and the need to retry the write operations.

The HMI may also contain error checking and error handling functionality for inbound frames.

The HMI is encouraged but not required to provide the following functions:

It is recommended that the HMI perform error handling of read and write commands, including retrying read and write requests, and checking for errors in read return data.

It is recommended that the HMI implement the Fast Reset mechanism to affect a purge of HMI and FBD channel state and then attempt to recover from intermittent errors.

2.5 Advanced Memory Buffer (AMB)

The Advanced Memory Buffer (AMB) is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel. A complete detail description of the AMB is contained in the *FBD AMB Specification*. The goal of this chapter is to provide a basic overview of the AMB interface.

The AMB is a memory interface that connects to an array of DRAM devices to the FBD channel. The AMB is a target device on the channel responding to channel commands directed to this AMB and forwarding channel command to other AMB devices on the channel.

All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management.

The AMB is expected to perform the following functions:

Support channel initialization procedures as defined in the Initialization Chapter to align the clocks and the frame boundaries, and verify channel connectivity,

Support the forwarding of southbound and northbound frames, servicing requests directed to this specific AMB or DIMM, as defined in the Protocol Chapter, and merging the return data into the northbound frames,

If the AMB is the last, southern-most, DIMM, perform the responsibilities of the last AMB on the channel,

Detect errors on the channel and report them to the host memory controller,

Support the FBD configuration register set as defined in the *FBD AMB Specification* Register Chapters,

Act as a DRAM memory buffer for all read, write, and configuration accesses addressed to this DIMM,

Provide a write buffer FIFO,

Support an SMBus protocol interface for access to the AMB configuration registers, and

Provide an interface for a thermal sensor as defined in the *FBD AMB Specification*.

2.6 Options

The FBD specification defines a small number of options to support the requirements of different applications. The capabilities of the AMB are communicated to the host during the initialization process in the TS2 training pattern and in bits readable in the Features register in the AMB.

2.6.1 Number of FBD Lanes

Southbound lanes:

It is recommended that a Host Controller implement 10 bit lanes with fail-over to 9 lanes. A host controller may choose to not implement fail-over, or to only implement 9 bit lanes, as is appropriate to the application.

The AMB must support 10 southbound bit lanes with the capability to fail-over to 9 lanes.

Northbound lanes:

There are 5 modes of operation for the northbound lanes as defined in Table 2-6:

Table 2-6 — Northbound Bit Lane Options

Mode	Memory ECC	Channel CRC	Fail Over Capable
14-lane mode	8 bit ECC	12 bit CRC	Yes
14-lane failover	8 bit ECC	6 bit CRC	No (failed over)
13-lane mode	8 bit ECC	6 bit CRC	Yes
13-lane failover	8 bit ECC	No CRC	No (failed over)
12-lane mode	No ECC	6 bit CRC	No

Note: 14-lane fail over and 13-lane mode operate with the same frame format. 13-lane fail over does NOT use the same frame format as 12-lane mode. 13-lane fail over maintains memory ECC without channel CRC protection, while 12-lane mode is designed for non-ECC DIMMs.

The Host controller may implement any combination of northbound modes, depending on the RAS requirements of the application.

An AMB may support all 4 ECC northbound modes: 14-lane mode, 14-lane failover mode, 13-lanes mode, and 13-lane failover mode as a group, or support just the 12-lane mode, or support all 5 modes.

2.6.2 ECC and non-ECC DIMMs

It is desirable to minimize the number of DIMM types in the market to just two kinds, ECC and non-ECC. This reduces the flexibility that can be allowed for AMBs in order to guarantee operation of DIMMs of the proper type in all systems. The DIMM will operate in ECC mode if any of the 4 ECC northbound modes are selected during initialization. The DIMM will operate in non-ECC mode if the 12-lane mode is selected during initialization.

ECC DIMMs:

An AMB that supports ECC must support all 4 ECC northbound modes: 14-lane mode, 14-lane failover mode, 13-lanes mode, and 13-lane failover mode. This assures that the DIMM will work with all ECC host controllers, and avoid confusion in the marketplace with different levels of RAS within ECC DIMMs. In ECC mode the AMB will interpret a Command+Wdata frame as containing a 72-bit data payload.

Non-ECC DIMMs:

An AMB that supports non-ECC must support 12-lane mode and the Data Mask write operations to memory. This provides a 6-bit channel CRC on northbound frames, but no fail-over capability. In non-ECC mode the AMB will interpret a Command+Wdata frame as containing 8 Data Mask bits and a 64-bit data payload.

2.6.3 Variable Read Latency

An AMB may support the Variable Read Latency feature that allows the data from DIMMs closer to the host to provide read data sooner than DIMM farther away from the host. The Variable Read Latency feature is implemented with the Command_to_Data_Decr register in the AMB. A bit in the Features register in the AMB indicates if this feature is supported. Refer to the Initialization Chapter for details. It is possible for Variable Read Latency to be used with a mixture AMBs with and without support, especially if the closer DIMMs support it.

2.6.4 L0s State

An AMB may support the L0s low latency power saving state. A bit in the Features register in the AMB indicates if this feature is supported. If any DIMM indicates that it does not support L0s, the host controller should not attempt to put the channel into L0s. An AMB which indicates that it supports L0s must implement the L0s register and be able to respond to the L0s command and ignore inputs on lanes since they may be powered down.

2.6.5 Protocol Variants

It is desirable to provide a mechanism to support the addition of future protocol variants to the FB-DIMM specification. This section defines the mechanisms in the various areas of the FB-DIMM Architecture & Protocol Specification that accommodate future protocol variants. Details of the protocol variant must be captured in a protocol variant specific addendum.

2.6.5.1 SPD content

The SPD EEPROM contains two bytes that identify to the boot firmware what protocols are supported by the DIMM. A bit map is present in the "Supported Protocols" bytes to identify which protocols are supported. More than one bit may be set if the DIMM supports more than one protocol.

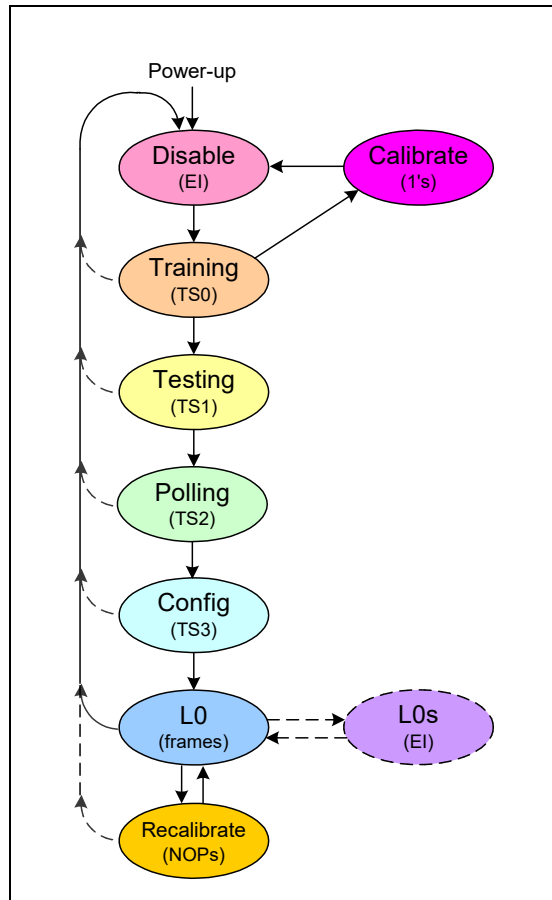
- Bit 0 = 1 indicates that the DDR2 Base non_ECC Protocol is supported (10 SB & 12 NB bit lanes).
- Bit 1 = 1 indicates that the DDR2 Base ECC Protocol is supported (10 SB, 13 NB & 14 NB bit lanes).
- Bit 2 = 1 indicates that the DDR3 Base non_ECC Protocol is supported (10 SB & 12 NB bit lanes).
- Bit 3 = 1 indicates that the DDR3 Base ECC Protocol is supported (10 SB, 13 NB & 14 NB bit lanes).
- Bits 4-15 are reserved for future protocol variants.

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3 Channel Initialization

This chapter defines the process of initializing the FBD channel. The FBD initialization process generally follows the top to bottom sequence of state transitions shown in the high level AMB Initialization Flow diagram in Figure 3-4. The host must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state. The value in parenthesis in each state bubble indicates the condition/activity of the links during these states.

Figure 3-4 — AMB Initialization Flow Diagram



The states in the AMB Initialization Flow diagram are:

Disable – The channel is inactive and the interface signals are in a low power Electrical Idle condition.

Training – The initial bit alignment and frame alignment training is done in this state.

Testing – Each bit lane is individually tested in this state.

Polling – The channel capabilities of the individual AMB devices are communicated in this state.

Config – The channel width configuration is communicated to the AMB devices in this state.

L0 – The channel is active and frames of information are flowing between the host and the AMB devices.

Recalibrate – The channel is momentarily idled to allow TX and Rx circuits to be recalibrated.

L0s – The channel is in a low-latency power saving condition. (Optional)

Each bit lane is initialized (mostly) independently to support fault tolerance. The transitions in the figure represent the transitions of the AMB core logic state machine and are taken when the transition event is detected on the minimum required number of southbound bit lanes. The chain of FBD links connecting the host to the AMBs must each be initialized to establish the timing for broadcasting data frames in the southbound direction and for merging data frames in the northbound direction. The AMBs on the channel are generally initialized as a group but because each AMB is individually addressable many alternate initialization sequences may be employed.

In this chapter, southbound may be abbreviated as SB and northbound may be abbreviated as NB.

The FBD channel uses the timing parameters defined in Table 3-7 while sequencing through channel initialization.

Table 3-7 — Channel Initialization Timing Parameters

Timing Parameter	Value	Description
tCalibrate	960K frames (~2ms)	Calibration Interval: This value indicates the minimum amount of time the host will provide for the channel Rx and Tx circuits to perform initial electrical calibration steps following a hardware reset event.
tClkTrain	42 frames	Clock Training Interval: This value defines the period of time in which a minimum number of transitions must occur on each bit lane in order to ensure the clock tracker circuits remain locked on the data stream. (Based on 6 transitions within 512 UI)
tBitLock	119 frames	Bit Lock Interval: This value defines the maximum time an AMB may take to acquire bit lock on incoming TS0 patterns on a bit lane by bit lane basis and pass the TS0 pattern to the Tx outputs. This parameter is not used as a timeout but is provided as a requirement to limit the time it takes for a Fast Reset sequence to complete.
tFrameLock	154 frames	Frame Lock Interval: This value defines the maximum time an AMB may take to acquire frame lock on incoming TS0 patterns and be prepared to receive a TS1 pattern. This parameter is not used as a timeout but is provided as a requirement to ensure that intermediate AMBs acquire frame lock before the host starts sending TS1 patterns.
tEIPropagate	60nS 16 frames at 533 20 frames at 667 24 frames at 800	Channel Electrical Idle Propagate: This value defines the maximum time an AMB may take to detect an Electrical Idle on the Rx inputs and propagate the Electrical Idle to the Tx outputs.
tDisable	DDR: 533 / 667 / 800: 512M: 492 / 603 / 714 1Gbit: 504 / 618 / 732 2Gbit: 540 / 663 / 786 4Gbit: 511 / 751 / 892 in Frames.	Channel Disable Interval: This value defines the minimum amount of time the host will provide for the Electrical Idle condition to propagate to all AMBs on the channel to put them into the Disable state. It is calculated as $12 \cdot tEIPropagate \cdot 2 + \text{Self Refresh Entry}$.

The maximum skew between lanes of the high speed interface is specified in the AMB specification.

3.1 Reset and Inband Control “Signals”

This section describes special mechanisms used to control the AMB state while the host controller sequences the FBD channel through the initialization sequence.

3.1.1 RESET# Signal

The RESET# signal acts as a hardware reset and immediately puts the AMB into a known state. The AMB Initialization FSM is put into the Disable state and the NB Tx outputs are put into Electrical Idle regardless of the state of the NB Rx inputs. All “sticky” bits are set to their default values. The CKE signals to the DRAM devices are driven inactive to turn off the DRAM output drivers. DRAM specific mechanisms in the AMB may generate additional signal transitions to the DRAM devices to make sure that they do not hang in an unknown state. The AMB specification for each DRAM technology defines any DRAM specific mechanisms. If the DRAMs were in self refresh prior to RESET# being asserted, they will remain in self refresh through the hardware reset. The host must wait until the power and the reference clock to the AMBs have been stable for greater than or equal to 1ms before transitioning the channel out of the Disable state. The relationship between supply voltage, reference clock and the RESET# signal is defined in the *FBD AMB Specification*.

3.1.2 Inband Control “Signals”

There are no dedicated control signals implemented on an FBD channel. Two different channel characteristics are exploited to deliver inband control information on the FBD channel wires when no clock timing has been established between the host and the AMBs:

Electrical Idle (EI): During normal channel operation the Tx outputs are enabled and a differential voltage is present on each bit lane. In Electrical Idle the Tx outputs source insignificant current and the termination resistors at the receiver pull both signals of the differential pair to ground. The Rx inputs can detect if both differential inputs are near ground to receive inband control information. The specification of the voltage levels used for detection is defined in the *FBD Signaling Specification*.

Clock Training Violation: During normal channel operation the southbound bit lanes contain a minimum number of transitions every tClkTrain frames to keep the clock tracking circuits on each bit lane locked to the data stream. It is the absence of these periodic bit lane transitions that is used by the host to communicate control information. The AMB detects a clock training violation by the lack of sync frames sent from the host. See the AMB specification for details.

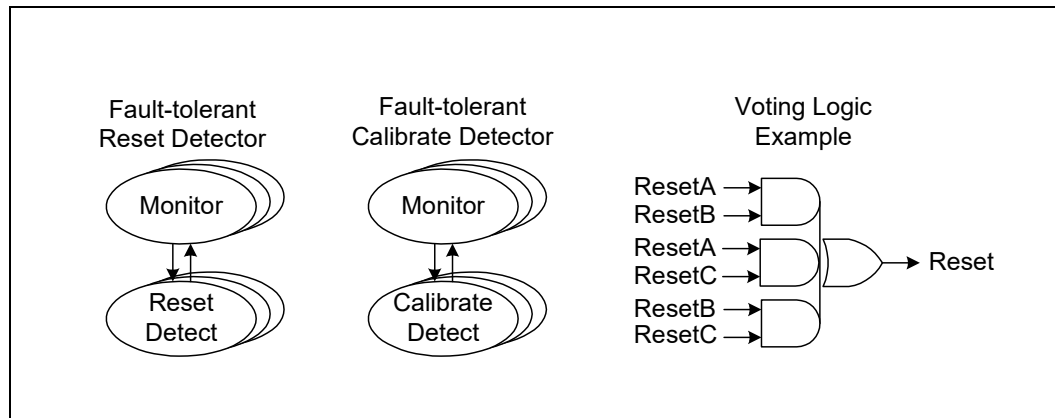
3.1.3 Inband Reset Event Detector

The host communicates a *reset event* to the AMBs by putting its SB Tx outputs into an Electrical Idle condition. These reset events do not put the AMB into a hardware reset condition, and thus allow the retention of sticky state information.

For high reliability, it is assumed that any of the channel bit lanes could be faulty and the FBD link must still function properly in the presence of a single bit lane failure (actually one in each direction). The reset event must be detectable even if any one of the bit lanes is in Electrical Idle, stuck at zero, stuck at one, or is transitioning with an erroneous pattern. To guarantee that any single bit lane failure will not prevent the reset events from being delivered, a fault-tolerant reset detection mechanism is required. The required mechanism uses three Reset Event Detectors to monitor the 3 least significant SB bit lanes. The outputs of the three reset detectors are routed to each state machine in the AMB and each state machine uses voting logic similar to the example in Figure 3-5 to decide if a reset event is present. Electrical Idle present on at least 2 of 3 bit lanes is detected as a reset event. This redundant delivery of reset guarantees that the reset event is delivered even if any of the three bit lanes is bad or if any one of the Reset Event Detectors is faulty.

The detection of a reset event is different than a hardware reset, and does not put all internal AMB registers into a known state. In all cases except the L0s state the detection of a reset event will cause the AMB internal state machines to complete any current activities, perform clean up operations, and make an orderly transition to the Disable state. In the L0s state the channel is disabled to save power and the reset event detectors are ignored. The AMB is in the L0s state for less than or equal to tClkTrain and transitions back to the L0 state where the reset event is then detected.

Figure 3-5 — In-band Control Signal Detectors



3.1.4 Inband Calibrate Event Detector

The host communicates a *calibrate event* to the AMBs by sending a continuous stream of 1's on all southbound bit lanes for a time greater than or equal to $t_{\text{Calibrate}}$. A clock training violation will occur and trigger the event in the AMBs.

Following any hardware reset, the transmitters and receivers must be calibrated to adjust them for optimum performance. Before this calibration is performed only gross logic one and logic zero states can be communicated to the AMBs. Similar to the Reset Event Detectors, the Calibrate Event Detectors on each AMB monitor the 3 least significant SB bit lanes and a continuous stream of 1's for a time greater than or equal to two times t_{ClkTrain} on at least 2 of 3 bit lanes is detected as a calibration event. The Calibrate Event Detectors are used to transition the AMBs from the Training state to the Calibrate state.

3.2 Training Sequence Ordered-sets

Before the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs. Instead of channel commands, training sequences are sent on each bit lane to communicate with the AMBs in a serial fashion. Training sequences are composed of ordered sets used for initializing bit alignment, frame alignment, bit lane testing, and to exchange Physical Layer initialization/configuration parameters. Training sequences are sent serially on all bit lanes in parallel. The host must send the training sequences bit aligned on all SB bit lanes. The host must repetitively send a stream of training sequences to the AMBs during each training state. The host generally receives a corresponding stream of training sequence from the AMBs to indicate that the SB training sequence has been correctly received. The reception of the training sequence from the AMBs provides reliable notification to the host that the requested training has completed and that the host may transition the channel to the next state. The host transitions the channel to the next state by changing the type of training sequence it is repetitively sending on the channel. The host must transition from one type of training sequence to another without any dead time between the sequences.

Training sequences are defined using 12-bit groups. Training sequence patterns are sent serially starting from the LSB (bit 0) to MSB (bit 11) within each group and in sequential group order from group 0 to n .

The training sequences and any data values in the training sequences must be detected by the AMBs on 2 or more of the 3 least significant SB bit lanes before any state transitions are taken by the AMBs. This insures that a bad bit lane or a transient bit failure does not cause the AMB to falsely respond to the sequence. Voting logic similar to that shown in Figure 3-5 may be used to filter out bit lane or transient bit failure.

After initialization, the groups of bits received on multiple SB bit lanes are combined into the frames used to communicate Channel and DRAM commands to the AMBs.

There are 4 defined training sequences:

TS0 – Used in the Training state for initial link training.

TS1 – Used in the Testing state to perform an electrical stress test of the individual channel bit lanes.

TS2 – Used during the Polling state to determine the round trip latency of the channel and to test that each individual AMB can perform data merge properly.

TS3 –Used in the Config state to communicate the channel configuration to the AMBs.

3.3 Channel Initialization Sequence

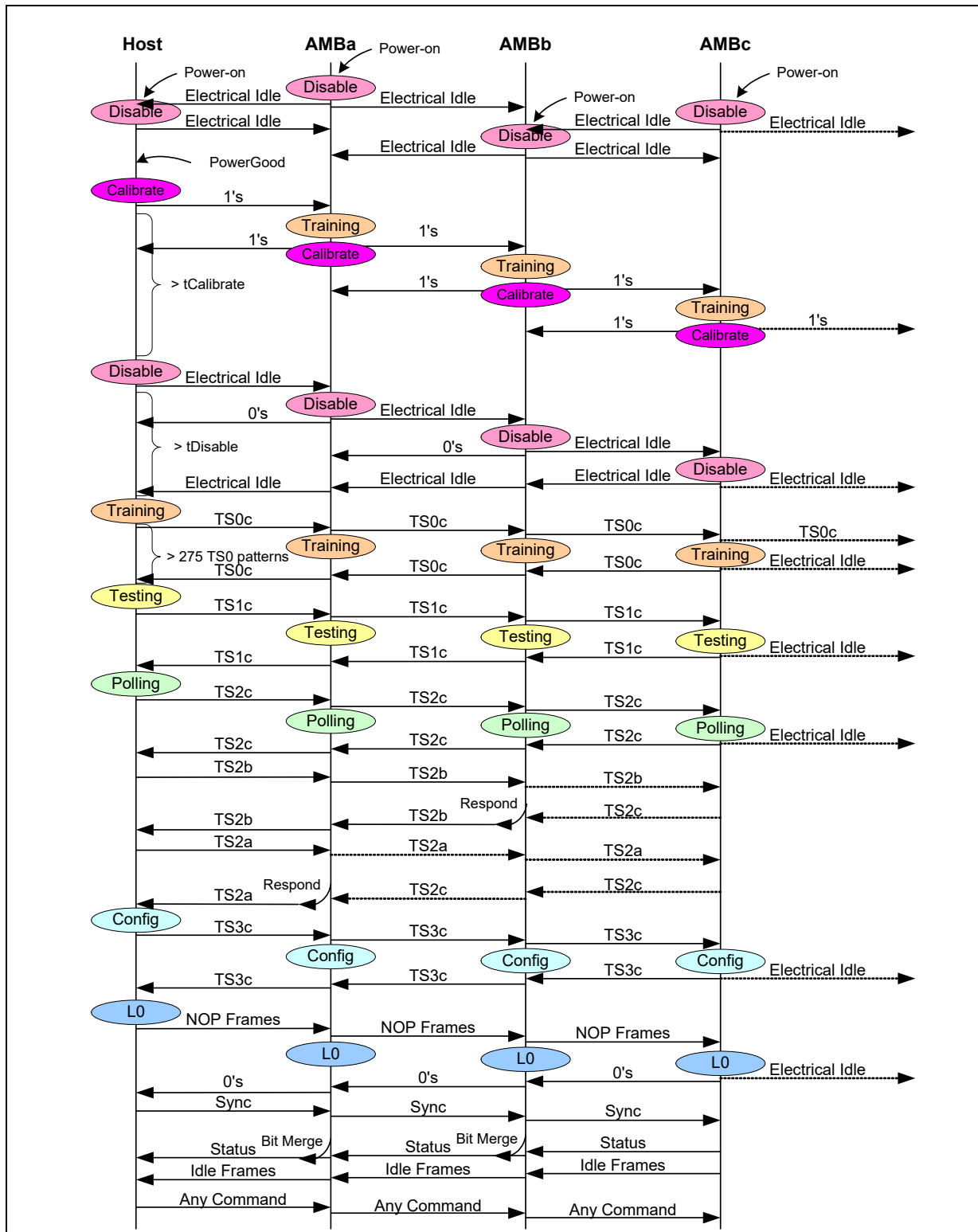
The host controller sequences the FBD channel through the initialization sequence. The AMB devices on each DIMM monitor in-band signals from the host and use events and patterns on these signals to transition from one state to another. If the channel fails to initialize properly the host may transition the channel back to the Disable state and try again a number of times before reporting a failure to the system.

It is undesirable to continuously drive high frequency signals into un-terminated transmission lines because of the EMI that is generated and the power that is wasted. To avoid this the host must return to the Disable state if the channel does not properly initialize.

Figure 3-6 shows the graphical representation of the “full” initialization sequence for a 3 AMB configuration. This representation shows the data traffic on each link. The placement down the page indicates the timing of the initialization sequence of events. The bubbles on the various timelines represent state transitions.

Note that the AMBs may be powered up in any sequence and will remain in the disabled state until instructed by the host to transition to the next state.

Figure 3-6 — Initialization Sequence Flow

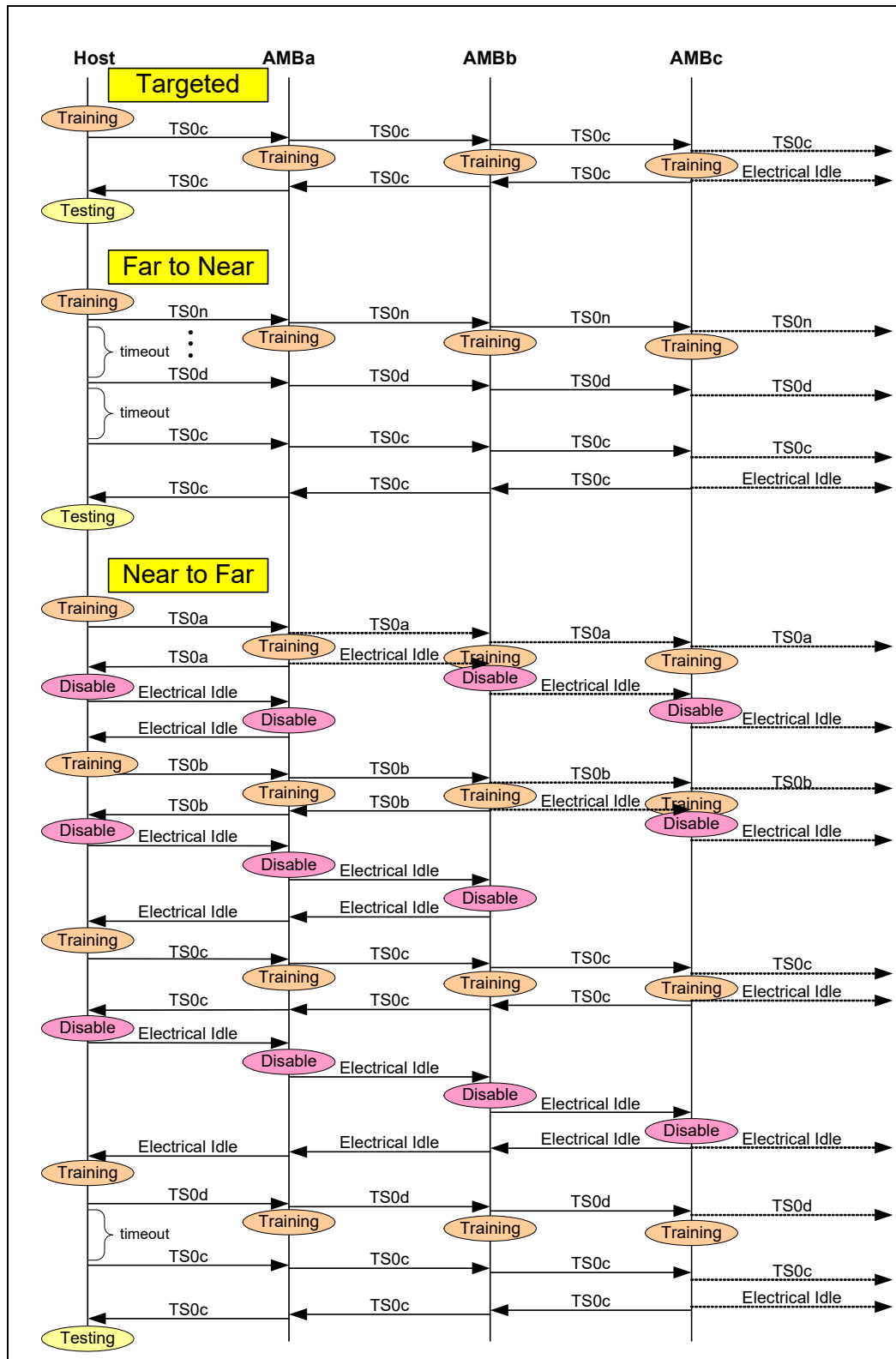


The above example illustrates a ‘targeted’ AMB discovery method that uses system information such as access to the SPD EPROM on the DIMMs to determine the last DIMM position. Figure 3-7 illustrates the above ‘targeted’ AMB discovery method and two alternative discovery methods; ‘near to far’, and ‘far to near’. Either of these alternative discovery methods may be used based on system requirements.

The ‘far to near’ method starts at the farthest DIMM location supported by the platform and searches toward the host until an AMB is found. If no AMB is found the host must timeout after 1ms and try the next closer DIMM.

The ‘near to far’ method adds an AMB at a time starting closest to the host. Each time the host changes from one AMB to the next the northbound clock and alignment must be reestablished. The channel must transition back to the Disable state to initialize the clock trackers so they will reestablish lock with the new northbound timing. After the host walks past the last DIMM it backs up and establishes the northbound timing using the last AMB found.

Figure 3-7 — Alternative AMB Discovery Sequence Flows



3.3.1 Firmware Transition Control

The channel initialization and configuration sequence may be controlled by a hardware state machine or directed by firmware. To provide a flexible mechanism for dealing with a variety of FBD channel failure conditions it is recommended that the channel initialization and configuration process be controlled by firmware.

It is recommended that implementation specific control registers be included in the host to allow firmware to step through the initialization steps and perform the following functions:

- Put the SB Tx outputs into Electrical Idle.
- Drive SB Tx outputs to all ones.
- Detect if the NB port is receiving Electrical Idle.
- Drive TS0 patterns with an arbitrary AMB_ID value.
- Receive TS0 patterns and read the returned AMB_ID value
- Drive TS1 patterns with an arbitrary AMB_ID value and with a sequence of electrical stress test patterns on each bit lane. Registers to hold an arbitrary 24-bits of Test Parameter values are recommended.
- Receive TS1 electrical stress test patterns and check the patterns.
- Test the NB bit lanes and report NB test results.
- Drive TS2 patterns.
- Receive TS2 patterns and determine the round trip channel delay.
- Drive TS3 patterns with channel configuration values.
- Receive TS3 patterns and check the returned values.
- Set the Last_AMB_ID value.
- Set the Hot_Add_AMB_ID value
- Set the Fast_Reset_Flag value.
- Set the Recalibrate_Duration value.
- Set the L0s_Duration value.
- Transition the channel to the L0 state and send the first Sync command.

It is expected but not required that the host will implement a Hot-Add initialization sequence in firmware after a DIMM has been added to the system. The *FBD AMB Specification* Register chapter defines the AMB configuration registers that perform the Hot-Add Initialization functions. This register model may be duplicated in the host for similar control of the entire channel.

3.3.2 AMB Internal State Variables

A number of internal flags and timers are referenced in the following sections. These flags and timers are implementation specific and included in the state tables to describe internal AMB state that may or may not be visible in defined AMB registers. These flags and timers include:

- Last_AMB_Flag – set in the last AMB to enable unique properties of the AMB in this position.
- First_Sync_Received_Flag – set to disable further initialization of the Idle/Alert Frame LFSR.

- Idle/Alert Frame LFSR – a counter in each AMB used to generate Idle and Alert frames on the NB channel.
- Alert_Flag – a flag that indicated that this AMB detected an error and is or was generating NB Alert frames.
- Recalibrate_Timer – a timer that keeps track of how long the AMB has been in the Recalibrate state.
- L0s_Timer – a timer that keeps track of how long the AMB has been in the L0s state.

3.3.3 Disable State

The channel is forced into the Disable state during hardware reset. The host may put the channel into the Disable state at any time and from any other state other than L0s by putting the three least significant Tx outputs into Electrical Idle. The host must not put the channel into the Disable state from the L0 state until any DRAM write operations have had time to complete. Channel initialization always starts in the Disable state.

State Table Definitions

- “Disable Rx inputs” means that the input receiver termination is still enabled, the high-speed receiver circuitry may be turned off to reduce power consumption, and the receivers are not required to provide any data. The Electrical Idle detectors may be on or off as specified in the state tables.
- “Disable Tx outputs” means that the current/voltage sources are turned off. The Tx termination remains on to inhibit noise on the high speed lanes for robust detection of electrical idle. Other transmitter circuitry may be turned off to reduce power consumption.

Table 3-8 defines the actions of the AMBs during the Disable state.

Table 3-8 — Disable State

	AMB
Entry Condition	Hardware reset <i>or</i> Electrical Idle detected on 2of3 LSB SB Rx inputs.
Action	Upon Hardware Reset the following actions are performed: — Terminate any commands in progress including Self Refresh entry sequence. If the DRAMs were in Self Refresh prior to the hardware reset, the Self Refresh mode will be maintained. If they were not in Self Refresh prior to the hardware reset, data may be lost. — Reset all memory elements to default values, including “sticky” bits. — Reset all logic to the default state. — Disable SB Rx inputs except Electrical Idle detectors on 3 LSB inputs — Disable SB Tx outputs — Disable NB Rx inputs including Electrical Idle detectors — Disable NB Tx outputs Upon entry from other than hardware reset — If transitioning from the Testing, Polling, Config, L0, L0s, or Recalibrate states, put the DRAMs into Self Refresh — Disable SB Rx inputs except Electrical Idle detectors on 3 LSB inputs — Disable SB Tx outputs — If Electrical Idle not yet detected on 2of3 LSB NB Rx inputs or the DRAM Self Refresh entry has not yet completed • Continue to put DRAMs into Self Refresh • Disable NB Rx inputs except Electrical Idle detectors on 3 LSB inputs • Leave NB Tx outputs enabled and drive logic 0’s — Else (EI detected on 2of3 LSB NB Rx inputs and DRAM Self Refresh entry completed) • Disable NB Rx inputs including Electrical Idle detectors • Disable NB Tx outputs • Reset “non-sticky” memory elements to their default values. Memory elements not involved in self refresh entry or EI detection could be reset earlier in this process if desired. • Reset all logic to the default state
Exit Condition & Next States	Transition to the Training state if hardware reset condition removed and a non-Electrical Idle condition detected on 2of3 LSB SB Rx inputs, <i>else</i> wait.

At the transition into the Disable state from any active state the “sticky” status bits held in status registers are frozen to reflect the state of the interface before the transition. Channel commands are required to change the individual sticky bits. Refer to the *FBD AMB Specification* Register chapter for the definition of the sticky bits in the AMB status registers.

When transitioning into the Disable state from another state other than because of a hardware reset, the AMBs will only disable NB Tx outputs if Electrical Idle is detected on 2of3 LSB NB Rx inputs. In the Disable state the last AMB detects that no AMB is south of its position and disable its NB Tx outputs. The next closer AMB to the host will detect this condition and disable its NB Tx outputs. Each intermediate AMB will continue this process until the AMB closest to the host disables its NB Tx outputs. At this point the host can be assured that all of the AMBs are in the Disable state and that all of the DRAM devices have been put into Self Refresh. In high-availability applications, the host must implement a timeout to attempt channel initialization even if the Electrical Idle condition is not detected from the channel to prevent a faulty AMB in the chain from allowing a subset of the memory subsystem from being initialized.

The channel may stay in the Disable state indefinitely while the host is held in reset by external conditions. The host must wait for the NB Rx inputs to detect that the channel is in Electrical Idle indicating that the AMBs are all in the Disable State plus a minimum of 100 frames before taking the channel out of the Disable state. In high-availability

applications, the host may proceed after a timeout period. The length of the host timeout is platform specific but must be larger than the maximum time it takes for the AMBs to transition to the Disable state. If the host Fast_Reset_Flag is reset the host must transition the channel to the Calibrate state to perform the calibration of the channel transmitters and receivers. The host drives logic ones for a period equal to or greater than tCalibrate to signal to the AMBs that they should transition to the Calibrate state and to give them time to complete the calibration operation (Full Reset). The AMBs will momentarily transition from the Disable state into the Training state until the Calibrate Event Detectors recognize the calibrate event and then transition into the Calibrate state.

3.3.4 Training State

The host drives a repetitive series of TS0 patterns to transition the AMBs from the Disable state to the Training state and to perform initial link training. The host may detect that the last AMB has acquire frame lock when TS0 patterns are received on the required number of NB Rx inputs. Table 3-9 defines the TS0 format. Bit patterns in TS0 are used to perform bit lock and frame lock. The pattern is mostly filled with an alternating 1010 pattern to align the clock trackers with the incoming data stream. The sequence generally has logic zeroes in the even bit positions and logic ones in the odd bit positions. The beginning of the sequence is identified by the header pattern shown in the table below and is used to establish the alignment of the serial data onto frame boundaries.

The AMB_ID field identifies which AMB should initiate the northbound data stream and send a TS0 pattern northbound to the host.

Table 3-9 — Training Sequence – TS0 (Training)

Group #	Description	Value [11:0]
0	TS0 Header: Continuous string of 9 ones identifies the start of the TS0 sequence.	Bit [11:0]: 12b'1011 1111 1110 ↑ ↑ MSB LSB
1	Control: Bit [4:0] – training pattern Bit [11,9,7,5] – AMB_ID — Host indicates which AMB should return a TS0 pattern. — AMB returns this value. Bit [10,8,6] – training pattern	Bit [4:0]: 5b'0 1010 Bit [5]: AMB_ID value bit 0 Bit [6]: 1b'0 Bit [7]: AMB_ID value bit 1 Bit [8]: 1b'0 Bit [9]: AMB_ID value bit 2 Bit [10]: 1b'0 Bit [11]: AMB_ID value bit 3
11-2	10 groups of clock training patterns	Bit [11:0]: 12b'1010 1010 1010

Table 3-10 estimates the amount of time a fully populated channel may take to complete initial training. Based on this estimate and providing a little margin, the host must send a minimum of 275 TS0 patterns before switching to TS1 patterns to give all intermediate AMBs time to acquire frame lock.

Table 3-10 — Training Duration Estimate at DDR2-667

State	Duration per AMB	Duration for 12 AMBs on the channel (Frames)	Description
EI deassertion detection	10 frames	120	Time to detect data being driven on the SB Rx inputs.
Bit lock	119 frames	1428	Time to lock on the SB input bit stream and start to forward to the next AMB.

Table 3-10 — Training Duration Estimate at DDR2-667 (Cont'd)

State	Duration per AMB	Duration for 12 AMBs on the channel (Frames)	Description
Last AMB frame lock	13 TS0 patterns	154	Time for the last AMB to deskew its bit lanes, align its core clock, and start sending TS0 patterns NB
EI deassertion detection	10 frames	120	Time to detect data being driven on the NB Rx inputs.
Bit lock	119 frames	1428	Time to lock on the NB input bit stream and start to forward to the next AMB.
Host frame lock	13 TS0 patterns	154	Time for host to align to deskew its bit lanes and align its frame boundaries
Total frames		3404	Approximate number of frames for training.
Total TS0 patterns		284	Approximate number of TS0 patterns needed for training.

Table 3-11 defines the actions of the AMBs while in the Training state. Each AMB determines its AMB_ID number using the SMBus address strap pins. Refer to section 2.1.3 for the SMBus address to AMB_ID mapping.

Table 3-11 — Training State

	AMB
Entry Condition	Entry from Disable state if reset conditions are removed and exit from Electrical Idle detected on 2of3 LSB SB Rx inputs
Action	The following actions are performed: — Enable SB Rx inputs including Electrical Idle detectors • If SB bit lock (on a bit lane by bit lane basis) – Enable SB Tx output – Forward SB data patterns • Else – Leave SB Tx output disabled — Establish core clock alignment and drive a stable clock to the DRAM devices — If the TS0 header and AMB_ID field are received on 2of3 LSB SB Rx inputs, and the AMB_ID value matches the AMB number • Set the Last_AMB_Flag • Disable SB Tx outputs (they were momentarily enabled) • Disable NB Rx inputs including Electrical Idle detectors • Enable NB Tx outputs • Loopback or generate NB TS0 on all supported bits using the Command to Data fractional frame delay — Else • Enable NB Rx inputs including Electrical Idle detectors • If NB bit lock (on a bit lane by bit lane basis) – Enable NB Tx output – Forward NB data patterns (initial NB TS0 pattern may be truncated) • Else, – Leave NB Tx output disabled
Exit Condition & Next States	Transition to Calibrate state if 1's detected on 2of3 LSB SB Rx inputs for greater than 2 times tClkTrain frames, <i>else</i>, transition to Testing state if SB TS1 header is received on 2of3 LSB SB Rx inputs, <i>else</i>, transition to Disable state if Electrical Idle detected on 2of3 LSB SB Rx inputs, <i>else</i> wait.

The host controller must send at least 4 TS0 sequences after the final supported northbound lane is detected to exit electrical idle.

3.3.4.1 Southbound Clock Training

After any reset event the southbound clock tracking state machines are initialized and must reacquire a lock on the received data timing. This is referred to as bit lock.

Southbound clock alignment is performed in the Training state. In this state all of the southbound bit lanes are enabled and the host sends frames of data filled with a pattern rich in bit transitions. During this time the clock tracking state machines on each bit lane lock their clock trackers to the transitions in the pattern. The pattern has a long sequence of alternating ones and zeroes. Proper synchronization is attained when all even data bits in this field are received as zeroes and all odd data bits are received as ones.

The TS0 pattern is not forwarded from the first AMB to the second AMB until the first AMB has locked its clock tracker. The clock tracking state machines in each AMB in turn locks onto the TS0 pattern as its input pattern stabilizes. A chain of up to 12 AMBs is supported to accommodate large memory configurations and configurations that use channel repeaters or have a logic analyzer component in the chain. Each AMB must be able to resolve clock alignment and send a stable waveform to the next southern AMB in a time less than tBitLock.

After a time greater than or equal to tBitLock times 12 the clock trackers on all functional southbound bit lanes should have locked and are tracking slow variations in the channel clock timing.

3.3.4.2 Southbound Bit Lane Deskew and Core Clock Training

Southbound bit lane deskew and core clock alignment are also performed in the Training state. The TS0 pattern has a unique header pattern that is used to identify the beginning of the ordered set. The beginning of the TS0 pattern is used to align the bit lanes even if the skew between bit lanes is greater than several frame times.

The AMB must ensure that the DRAM clock is stable at the DRAM devices before generating or forwarding the TS0 pattern to the host.

3.3.4.3 Northbound Clock Training

After any reset event the northbound clock timing must be reestablished. During northbound clock alignment, the specified AMB on the channel sends a TS0 pattern northbound on all supported bit lanes. The data pattern at the host is not stable until all of the intermediate AMBs have locked their clock trackers. Each AMB must be able to resolve clock alignment and send a stable waveform to the next northern AMB in a time less than tBitLock.

3.3.4.4 Northbound Host Bit Lane Deskew and Alignment to Core Clock

The host performs northbound bit lane deskew and alignment to its core clock while in the Training state.

Northbound frame alignment is performed in the Training state. This frame alignment is not changed after being established in the Training state. Any subsequent return timing changes are always made in full frame increments.

3.3.5 Testing State

The host drives a TS1 pattern to transition the AMBs from the Training state to the Testing state and may send an arbitrary number of TS1 patterns to test the channel.

The DRAM clock is stable at the DRAM devices before entering the Testing state. When entering the Testing state, if the DISREXIT configuration bit is not set, the AMBs assert the CKE to all DRAMs attached to the AMBs to cause the DRAM devices to exit Self Refresh. Following hardware RESET, the DISREXIT bit is set, preventing the DRAMs from exiting self refresh. The host controller will reset the bit prior to the fast reset in which it wants the DRAMs to exit self refresh. Commands must not be immediately sent to DDR2 SDRAMs after exiting Self Refresh until two parameters are satisfied:

tXSNR is the minimum time from exiting Self Refresh before a non-Read command is executed and is defined as $tXSNR = tRFC + 10ns$ ($tRFC$ = refresh to active/Refresh command time = 75 to 195ns for 256Mb to 2Gb devices, device technology dependent).

tXSRD is the minimum time from exiting Self Refresh before a Read command is executed and is specified as 200 tCK.

The host must not send commands to the DDR2 SDRAM devices until the tXSNR and tXSRD parameters have been satisfied. The host must also not transition the channel back into the Disable state, which causes the AMBs to issue commands to put the DDR2 SDRAMs into Self Refresh, until the tXSNR parameter has been satisfied. The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

Table 3-13 defines the format of the TS1 pattern. The TS1 pattern is used to perform an electrical stress test of the channel bit lanes and has a platform specific length.

A host supporting a transient-error-tolerant initialization sequence must at least repeat TS1 patterns SB until it detects NB properly framed TS1 headers followed by control with the proper AMB_ID on any given lane.

A host that supports persistent-fault-tolerant initialization must at least repeat TS1 patterns SB until multiple properly framed TS1 patterns on 2of3 LSBs are returned. Note that a single SB lane fault plus a single NB lane fault may prevent the host from receiving TS1 patterns on 2of3 LSBs on one of the SB to NB mapping selections. In this case