

JEDEC STANDARD

Radio Front End - Baseband Digital Parallel (RBDP) Interface

JESD207.01

(Editorial Revision of JESD207, March 2007)

JANUARY 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2022
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

This page intentionally left blank

RADIO FRONT END–BASEBAND (RF-BB) INTERFACE**Contents**

	Page
1 Scope.....	1
2 References	2
3 Terminology.....	3
3.1 Terms and definitions.....	3
3.2 Acronyms and abbreviations	4
3.3 Numeric representation	4
4 Data path Functional layer	5
4.1 Data path signals	5
4.1.1 MCLK (Driven from RFIC to BBIC)	5
4.1.2 FCLK (Driven from BBIC to RFIC)	5
4.1.3 TXNRX (Driven from BBIC to RFIC).....	6
4.1.4 ENABLE (Driven from BBIC to RFIC).....	6
4.1.5 DIQ[11:10], DIQ[9:0] (Bidirectional)	7
4.2 Data bus idle and turnaround periods.....	7
4.3 Data path functional timing.....	8
4.3.1 Transmit burst.....	8
4.3.2 Receive burst	9
4.3.3 Data path timing parameters	9
5 Control Plane Functional layer	11
5.1 Control Plane signals.....	11
5.1.1 CPCLK (Driven from BBIC to RFIC).....	11
5.1.2 CPCSBB (Driven from BBIC to RFIC)	11
5.1.3 CPSDO, CPSDI and CPDIO	12
5.2 Control plane functional timing.....	13
5.2.1 Single transactions	13
5.2.2 Extended data transactions.....	14
5.2.2 Extended data transactions (cont'd).....	15
5.2.3 Control plane timing parameters.....	15
5.3 Control plane clock frequency bands	16
6 Electrical layer.....	17
6.1 Absolute maximum ratings	17
6.2 Normal operating conditions	17
6.3 DC characteristics	17
6.4 AC characteristics	18
6.5 Timing parameter measurement.....	18
Annex A Data path applications and resulting sample/data/clock rates	19
A.1 Mandatory rates.....	19
A.2 Optional rates	20
Annex B (Informative) Description of TXNRX and ENABLE burst control signalling.....	21
B.1 Pulse synchronisation fault recovery.....	22
Annex C Recommended PCB characteristics and component slew rates	23
Annex D Recommended component pin ordering.....	24

RADIO FRONT END-BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE**Contents****FIGURES**

Figure 1 — RBDP interface data path signals and layers.....	1
Figure 2 — RBDP interface control plane signals and layers	2
Figure 3 — Data path transmit burst start.....	8
Figure 4 — Data path transmit burst finish	8
Figure 5 — Data path receive burst start	9
Figure 6 — Data path receive burst finish	9
Figure 7 — Data path timing constraints summary	10
Figure 8 — Control plane 4-wire and 3-wire single transactions	13
Figure 9 — Extended transactions with 3 data fields	14
Figure 10 — Control plane timing constraints summary.....	15
Figure 11 — Timing parameter measurement	18
Figure 12 — TXNRX/ENABLE conceptual FSM	21
Figure 13 — Recommended BBIC/RFIC pin ordering	24

TABLES

Table 1 — Data path timing constraint values.....	10
Table 2 — Control plane extended data transaction performance gains.....	15
Table 3 — Control plane timing constraint values	16
Table 4 — Absolute maximum ratings.....	17
Table 5 — Normal operating conditions	17
Table 6 — DC characteristics	17
Table 7 — AC characteristics	18
Table 8 — Mandatory interface rates : 2T2R or 1T2R, 2x Fs	19
Table 9 — Mandatory interface rates : 1T1R, 2x Fs	19
Table 10 — Optional interface rates : 2T2R or 1T2R, 2x Fs.....	20
Table 11 — Optional interface rates : 1T1R, 2x Fs.....	20
Table 12 — PCB trace characteristics	23

RADIO FRONT END-BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE

Foreword

This standard establishes the requirements for a RF-BB Digital Parallel (RBDP) interface between a Radio Front-end integrated circuit (RFIC) and a BaseBand (BBIC) integrated circuit. The interface definition includes both data path transfers and control plane transactions. Included are requirements for electrical/physical signaling and logical/functional operation. These requirements are intended to ensure that multiple RFIC and BBIC components can interoperate across a common IC interface.

Introduction

This interface definition is intended for applications where the RFIC and BBIC are mounted on the same PCB, connected by relatively short PCB traces. A typical example would be a wireless networking NIC realized on a PCMCIA ExpressCard or Mini-PCI card format.

1.1 Data Path Overview

The data path interface is a (relatively) low-speed parallel-bus digital interface that has been defined primarily for wireless networking applications, transferring baseband I and Q waveform digital data samples in both directions between the BBIC and RFIC. The design envelope for the data path interface includes system configurations with both one and two RF/antenna paths in each direction : specifically, this includes 1T1R, 1T2R and 2T2R systems.

The data path interface consists of fourteen or sixteen single-ended LVCMOS digital signals, including clocks, control signals and data bus signals. The data bus width is matched to the baseband sample width being used : 10-bit sample widths are mandatory while 12-bit sample widths are optional. The data bus is bi-directional and alternates between transmit and receive transfer bursts, so the interface definition supports TDD or half-duplex FDD wireless networking system operation. The clock rates and interface transfer speeds support system architectures with up to 2x Nyquist over-sampling (including 802.16 WiMAX “sampling factor” expansion) for 20MHz channel bandwidths for up to 2 RF/antenna paths within the RFIC.

Figure 1 illustrates the RBDP data path interface.

1.2 Data Path Features

1. Data path clock and data rate controlled by RFIC (configured by BBIC) up to 90 MHz and 180 MSps
2. Data width matched to baseband sample width – 10 or 12 bits
3. Raw data path interface transfer bandwidth up to 1.8 or 2.2 Gbps
4. Double data rate (DDR) source-synchronous data path transfer timing
5. Low latency (single baseband complex sample period) data transfer
6. Low implementation complexity
7. Low power idle modes

1.3 Control Plane Overview

The control plane interface consists of three or four single-ended LVCMOS digital signals, including clock, chip-select and 1-bit serial data signals. The data signaling can be implemented either as two separate unidirectional signals or as a single bi-directional signal, but whichever is used, the data transfer is always half-duplex. The interface definition supports non-overlapping memory-mapped register read or write transactions with 8b-wide data fields. An extended transaction format allows multiple data fields to be transferred in a single transaction, reducing overhead and increasing efficiency and throughput.

Figure 2 illustrates the control plane board-level connections for the RBDP interface.

1.4 Control Plane Features

1. Clock rate and serial transfer rate controlled by BBIC up to 50 MHz
2. 1-bit command + 7-bit address control field format
3. Flexible transaction format using one or more 8-bit data fields per transaction allows per-transaction optimization of latency or bandwidth
 - a. minimum 325ns transaction latency with 8-bit data transactions (maximum 24 Mbps data rate)
 - b. data rates above 40 Mbps can be achieved with extended transactions (see section 5.2.2)
4. Serial clock can be stopped between transactions, reducing control plane power consumption to negligible levels

RADIO FRONT END–BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE

(From JEDEC Board Ballot JCB-07-18, formulated under the cognizance of the JC-61 Committee on Wireless Interface Network.)

1 Scope

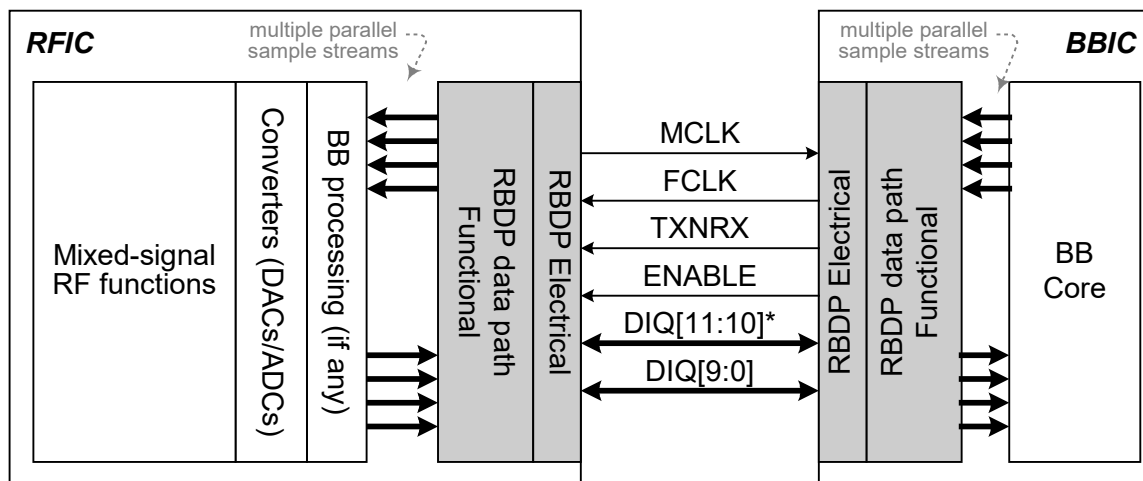
The normative information in this standard is intended to provide a technical design team to implement data path and control plane interface functions for an RFIC component and/or a BBIC component such that these components will operate correctly with each other (at the interface level), when designed to this specification. Additional information is provided in the annexes to help illustrate the normative material.

This document addresses the following interface topics for each of the data path and control plane definitions :

- 1) Electrical : time and amplitude specifications for individual signal transitions and related groups of signal transitions;
- 2) Functional : data path transfer burst format and control plane transaction format

This document defines a parallel data path and a serial control plane which together enable the bi-directional transfer of data and control/status information between the RFIC and the BBIC. The interface definition covers electrical signaling, digital timing, bit ordering and field formatting requirements to promote basic interoperability between multiple vendors. The interface definition does not extend to the level of automatic discovery of component capabilities which would be required to enable true “plug-n-play” operation.

Figure 1 illustrates the data path board-level connections and the layering of functions described by this interface definition (in the gray-shaded boxes) as well as a conceptual view of the internal connections for the interface logic blocks within the RFIC and BBIC.

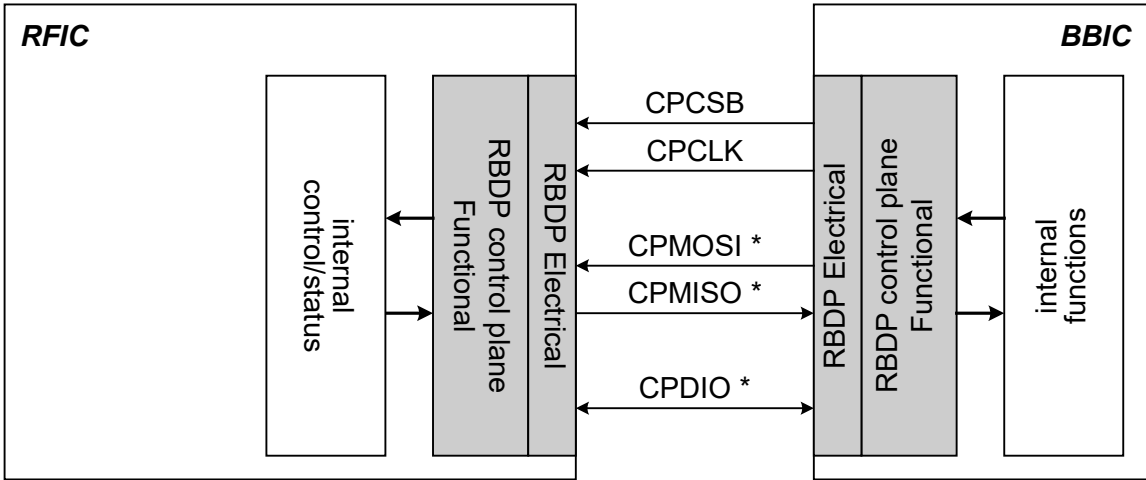


* DIQ[11:10] are optional, implemented if support for 12-bit baseband sample widths is required.

Figure 1 — RBDP interface data path signals and layers

1 Scope (cont'd)

Figure 2 illustrates the control plane board-level connections and the layering of functions described by this interface definition (in the gray-shaded boxes) as well as a conceptual view of the internal connections for the interface logic blocks within the RFIC and BBIC.



* The serial data transfer may be implemented using a single bidirectional pin CPDIO instead of two unidirectional pins CPMOSI and CPMISO.

Figure 2 — RBDP interface control plane signals and layers

2 References

Informative

The following standards contain provisions that, through references in the text, are informative in this standard. At the time of publication, the editions indicated were valid. All standards are subject to revisions.

<latest versions of 802.11 and 802.16 at time of publication>.

Normative

JESD76, *Description of 1.8 V CMOS Logic Devices*, April 2000

JESD8-7A, *1.8 V ± 0.15 V (Normal Range) and 1.2 V - 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*, October 2001

3 Terminology

For the purpose of this standard, the following terms, definitions, acronyms and abbreviations apply.

3.1 Terms and definitions

baseband frequencies: Low frequencies neighboring and including 0 Hz. These frequencies are represented with real In-Phase (I) and Quadrature (Q) parts or together as a complex signal. In this document, the word “baseband” will usually refer to a baseband processor (part of the BBIC in this interface).

(baseband) complex sample: one related pair of I and Q data words for one radio path, Q following I consecutively across the data path interface

complex sample rate: the minimum FFT sample rate required to support the system’s radio channel bandwidth. Defined by the wireless networking PHY standard concerned: e.g., 802.11 (= 2x Channel Bandwidth) or 802.16 (2x Sampling Factor x Channel Bandwidth). See Annex A for an illustration of applications of this interface definition and resulting sample rates, data rates and clock frequencies.

control plane transaction: a sequence of signal transitions on the control plane interface such that a single complete control plane read or write operation is executed

deskew: The act of aligning a clock with incoming data so that the clock edge can be used to latch data in the middle of the data eye.

data plane transfer burst: a sequence of transitions on the data plane signals which results in one or more baseband sample being communicated in either direction between the RFIC and the BBIC

interface baseband sample rate: the rate at which complex samples are transferred across the data path interface. May be either 1x, 2x or 4x the complex sample rate, depending upon system configuration. See Annex A for an illustration of applications of this interface definition and resulting sample rates, data rates and clock frequencies.

interface data rate (per pin): the number of bits transferred per DIQ signal per second. Must always be at least 2x, 4x or 8x the complex sample rate, depending upon system configuration.

radio: A device or a group of devices that translates the information bandwidth between baseband and the radio frequency portion of the spectrum.

sample: one data word, either I or Q, transferred across the data path interface.

receive direction: Direction of data flow across the interface, from the RFIC to the BBIC.

transmit direction: Direction of data flow across the interface, from the BBIC to the RFIC.