

JEDEC STANDARD

Low Power Double Data Rate 2 (LPDDR2)

JESD209-2F

(Revision of JESD209-2E, April 2011)

JUNE 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Contents

Scope	1
Package ballout & addressing	2
LPDDR2 12x12 PoP 2-channel 2x32 package ballout	2
LPDDR2 14x14 PoP 2-channel 2x32 package ballout	3
LPDDR2 14x14 0.5 mm ball pitch Dualx32 Channel PoP ballout using variation VEEBDC for MO-273.	4
LPDDR2 12x12 PoP 1-channel x32 package ballout using MO-273	5
LPDDR2 10x10 PoP 1-channel x32 package ballout using variation VAABCB for MO-273A .	6
79-ball x16 LPDDR2 0.5mm pitch package ballout (Discrete/MCP)	7
134-ball x16/x32 LPDDR2 package ballout (Discrete/MCP)	8
162-ball x16/x32 LPDDR2 and SDR-Flash package ballout	9
180-ball x16/x32 LPDDR2, SDR-Flash, and e-MMC package ballout	11
121-ball x16 LPDDR2, SDR Flash-NVM, and e-MMC package ballout	11
LPDDR2 Pad Sequence	12
Input/output functional description	13
LPDDR2 SDRAM Addressing.....	15
LPDDR2 NVM Addressing	15
Functional description	21
Simplified LPDDR2 Bus Interface State Diagram	22
Simplified LPDDR2-SX State Diagram	24
Simplified LPDDR2-N Simplified Bus State Diagram	26
Power-up, Initialization, and Power-Off	29
Mode Register Definition	33
LPDDR2-N Software Interface	48
Overlay Window	48
Data Byte Lane Assignment for Overlay Window Register	54
LPDDR2-NVM Operations	55
Nomenclature	56
Acronyms	57
Conventions	58
Overlay Window Enable and Disable.....	59
Dual operations and multiple partition architecture	81
LPDDR2 Command Definitions and Timing Diagrams	86
Activate Command	82
LPDDR2 Command Input Signal Timing Definition	84
Read and Write access modes	86
Burst Read Command	87
Burst Write Operation	95
Burst Terminate	100
Write Data Mask	104
LPDDR2-N: Preactive operation	106
LPDDR2-SX: Precharge operation	110
LPDDR2-SX: Refresh command	118
LPDDR2-SX: Self Refresh operation	125
Mode Register Read Command	128

Contents

Mode Register Write Command	133
Power-down	139
LPDDR2-SX: Deep Power-Down	146
Input clock stop and frequency change	147
No Operation command	148
Truth tables	148
LPDDR2-SDRAM Truth Tables	151
LPDDR2-N: Truth Tables	156
Data Mask Truth Table	159
Absolute Maximum Ratings	160
Absolute Maximum DC Ratings	160
AC & DC Operating Conditions	161
Recommended DC Operating Conditions	161
Input Leakage Current	162
Operating Temperature Range	162
AC and DC Input Measurement Levels	163
AC and DC Logic Input Levels for Single-Ended Signals	163
Vref Tolerances	164
Input Signal	165
AC and DC Logic Input Levels for Differential Signals	167
Differential Input Cross Point Voltage	170
Slew Rate Definitions for Single-Ended Input Signals	171
Slew Rate Definitions for Differential Input Signals	171
AC and DC Output Measurement Levels	172
Single Ended AC and DC Output Levels	172
Differential AC and DC Output Levels	172
Single Ended Output Slew Rate	173
Differential Output Slew Rate	174
Overshoot and Undershoot Specifications	175
Output buffer characteristics	176
RONPU and RONPD Resistor Definition	177
Input/Output Capacitance	183
Input/Output Capacitance	183
IDD Specification Parameters and Test Conditions	185
IDD Measurement Conditions	185
IDD Specifications	187
Electrical Characteristics and AC Timing	190
Clock Specification	190
Period Clock Jitter	193
LPDDR2-SX Refresh Requirements by Device Density	196
AC Timings	197
CA and CS _n Setup, Hold and Derating	206
Data Setup, Hold and Slew Rate Derating	212

LOW POWER DOUBLE DATA RATE 2 (LPDDR2)

(From JEDEC Board ballot JCB-13-23, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memory.)

1 Scope

This document defines the LPDDR2 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. This standard covers the following technologies: LPDDR2-S2A, LPDDR2-S2B, LPDDR2-S4A, LPDDR2-S4B, LPDDR2-N-A, and LPDDR2-N-B. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant 64 Mb through 8 Gb for x8, x16, and x32 SDRAM devices as well as 64 Mb through 32 Gb for x8, x16, and x32 for NVM devices. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR-NVM (N07-NV1A). Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare the LPDDR2 Standard.

2 Package ballout & addressing

2.1 LPDDR2 12x12 PoP 2-channel 2x32 package ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSSa/b	VDD2_a	DQ30_a	DQ29_a	VSSQ_	DQ26_a	DQ25_a	VSSQ_	DQS3_c	VSSQ_	DQ14_a	DQ13_a	VSS_a	VDD1_a	VDD2_a	DQ11_a	DQ10_a	DQ9_a	DQS1_t	DM_1_a	VDDQ_	DQS0_t	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS_a/	DNU
B	VSSQ_	VACC	DQ31_a	VDDQ_	DQ28_a	DQ27_a	VDDQ_	DQ24_a	VDDQ_	DQS3_t	DM3_a	DQ15_a	VDDQ_	VSSQ_	Vref(DQ	VDD2_a	DQ12_a	VDDQ_	DQ8_a	DQS1_c	VSSQ_	DM_0_a	DQS0_c	VSSQ_	VDDQ_	DQ5_a	DQ2_a	VACC	VSSQ_
C	VDD1_a	DQ16_b																										VDD1_a	VDD2_a
D	DQ17_b	VDDQ_																										DQ1_a	VDDQ_
E	DQ18_b	DQ19_b																										VSSQ_	DQ0_a
F	VSSQ_	DQ20_b																										DM2_a	VDDQ_
G	DQ21_b	VDDQ_																										DQS2_t	DQS2_c
H	DQ22_b	DQ23_b																										VSSQ_	DQ23_a
J	VSSQ_	VDDQ_																										VDDQ_	DQ22_a
K	DQS2_c	DQS2_t																										DQ20_a	DQ21_a
L	DM2_b	DQ0_b																										DQ19_a	VSSQ_
M	DQ1_b	VSSQ_																										VDDQ_	DQ18_a
N	DQ2_b	VDD1_b																										DQ16_a	DQ17_a
P	VSS_b	VSS_b																										VDD2_b	VDD1_b
R	VDD1_b	Vref(DQ																										VSS_b	CA0_b
T	VDD2_b	VDD2_b																										VDDCA	CA1_b
U	VDDQ_	DQ3_b																										Vref(CA	CA2_b
V	DQ4_b	VSSQ_																										VSSCA	CA3_b
W	DQ6_b	DQ5_b																										CA4_b	CSB1_b
Y	VDDQ_	DQ7_b																										CSB0_b	CKE1_b
A	DQS0_t	DQS0_c																										VSSCA	CKE0_b
A	DM0_b	VSSQ_																										CK_t_b	CK_c_b
A	VDDQ_	DM1_b																										VDDCA	CA5_b
A	DQS1_c	DQS1_t																										CA7_b	CA6_b
A	DQ8_b	VSSQ_																										CA8_b	VDDCA
A	DQ9_b	VDDQ_																										VSSCA	CA9_b
A	DQ10_b	DQ11_b																										VDD2_a	ZQ_b
A	VSSQ_	VDD1_a	VDD2_a	DQ13_b	VSSQ_	DQ15_b	DM3_b	DQS3_t	VDDQ_	DQ26_b	DQ27_b	VDDQ_	DQ30_b	VSSQ_	VDD2_a	Vref(CA	CA9_a	VSSCA	CA7_a	CA6_a	CK_c_a	VDDCA	CKE0_a	CSB0_a	CA3_a	CA2_a	CA1_a	VDD1_a	VSSCA
A	DNU	VSS_a/	DQ12_b	VDDQ_	DQ14_b	VDDQ_	VSSQ_	DQS3_c	DQ24_b	DQ25_b	VSSQ_	DQ28_b	DQ29_b	DQ31_b	VDD1_a	VSS_a	ZQ_a	CA8_a	VDDCA	CA5_a	CK_t_a	VSSCA	CKE1_a	CSB1_a	CA4_a	VDDCA	CA0_a	VSS_a/	DNU

NOTE 1: 12x12 mm, 0.4mm pitch, 29 rows

NOTE 2: 216 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

2.2 LPDDR2 14x14 PoP 2-channel 2x32 package ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A	DNU	VSSa/b	VDD2_a/	VSSQ_b	DQ29_b	DQ28_b	VSSQ_b	DQ25_b	DQ24_b	DQS3_c	DM3_b	DQ15_b	VSSQ_b	DQ13_b	DQ11_b	VSSQ_b	DQ9_b	DQS1_c	DM1_b	VSSQ_b	VSS_a/b	VDD2_a/	DQS0_c	DQ7_b	VSSQ_b	VSS_a/b	DNU
B	VDD1_a/	VACC	VDDQ_b	DQ31_b	DQ30_b	VDDQ_b	DQ27_b	DQ26_b	VDDQ_b	DQS3_t	VSSQ_b	VDDQ_b	DQ14_b	DQ12_b	VDDQ_b	DQ10_b	DQ8_b	DQS1_t	VDDQ_b	Vref(DQ)	VDD1_a/	DM0_b	DQS0_t	VDDQ_b	DQ6_b	VACC	VDD2_a/
C	DQ16_a	DQ17_a																								DQ5_b	DQ4_b
D	DQ18_a	VDDQ_a																								VDDQ_b	DQ3_b
E	VSSQ_a	DQ20_a	DQ19_a																						DQ2_b	DQ1_b	VSSQ_b
F	DQ21_a	VDDQ_a																							VDDQ_b	DQ0_b	
G	VSSQ_a	DQ22_a	DQ23_a																					DM2_b	DQS2_t	VSSQ_b	
H	DQS2_t	DQS2_c																							DQS2_c	DQ23_b	
J	VSSQ_a	DM2_a	DQ0_a																						DQ21_b	DQ22_b	VSSQ_b
K	DQ1_a	VDDQ_a																							VDDQ_b	DQ20_b	
L	VSSQ_a	DQ2_a	DQ3_a																						DQ19_b	DQ18_b	VSSQ_b
M	DQ4_a	VDDQ_a																							VDD2_a/	DQ17_b	
N	VSSQ_a	DQ5_a	DQ6_a																						DQ16_b	VDDQ_b	VSSQ_a
P	DQ7_a	VDDQ_a																							VDDCA_	CA0_a	
R	VSSQ_a	DQS0_c	DQS0_t																						CA1_a	CA2_a	VSSCA_
T	DM0_a	VDDQ_a																							CA3_a	CA4_a	
U	VSS_a/b	VSSQ_a	Vref(DQ)																						CS0_n	CS1_n	VSS_a/b
V	VDD2_a/	VDD1_a/																								CKE0_a	CKE1_a
W	VSS_a/b	VDD2_a/	DM1_a																						CK_c_a	CK_t_a	VSSCA_
Y	DQS1_c	DQS1_t																							VDDCA_	CA5_a	
A	VSSQ_a	DQ9_a	DQ10_a																						Vref(CA)	CA6_a	VDD2_a/
A	DQ8_a	VDDQ_a																							CA7_a	VSS_a/b	
A	VSSQ_a	DQ11_a	DQ12_a																						CA8_a	CA9_a	VSSCA_
A	DQ13_a	DQ14_a																							VDDCA_	VDD2_a/	
A	VSSQ_a	DQ15_a																							VDD1_a/	ZQ_a	
A	VSS_a/b	VDDQ_a	DM3_a	DQS3_t	DQS3_c	DQ25_a	DQ27_a	VDDQ_a	DQ29_a	DQ31_a	VDD2_a/	VDD1_a/	VDDCA_	CA9_b	CA7_b	VDD2_a/	Vref(CA)	VDDCA_	CK_t_b	CKE1_b	CS0_n	CA4_b	VDDCA_	CA2_b	CA0_b	VDD2_a/	VSS_a/b
A	DNU	VDD2_a/	VSSQ_a	VDDQ_a	DQ24_a	DQ26_a	VSSQ_a	DQ28_a	DQ30_a	VSSQ_a	VSS_a/b	ZQ_b	VSSCA_	CA8_b	CA6_b	CA5_b	VSS_a/b	VSSCA_	CK_c_b	CKE0_b	CS1_n	VSSCA_	CA3_b	CA1_b	VSS_a/b	VDD1_a/	DNU

NOTE 1: 14x14 mm, 0.5mm pitch, 27 rows
NOTE 2: 220 Ball Count
NOTE 3: Top View, A1 in Top Left Corner
NOTE 4: See JESD21-C, Section TBD

2.3 LPDDR2 14x14 0.5 mm ball pitch Dualx32 Channel PoP ballout using variation VEEBDC for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	DNU	VSSA/b	VDD2_a/	DQ31_a	VDDQ_a	VSSQ_a	DQ26_a	DQ24_a	DQS3_t	DM3_a	DQ15_a	DQ13_a	VSSQ_a	VDDQ_a	DQ8_a	VSSQ_a	Vref(DQ)	VDD1_a/	VDDQ_a	VSSQ_a	DQ7_a	DQ5_a	VSSQ_a	VDDQ_a	VDD1_a/	VSSQ_a	DNU	
B	VSSQ_b	VACC	VSSQ_a	DQ30_a	DQ29_a	DQ27_a	VDDQ_a	VSSQ_a	DQS3_c	VSSQ_a	DQ14_a	DQ12_a	DQ11_a	DQ9_a	DQS1_c	VDDQ_a	VSS_a/b	VDD2_a/	DQS0_c	DM0_a	DQ6_a	DQ4_a	DQ3_a	DQ1_a	DQ0_a	VACC	VSS_a/b	
C	VDD1_a/	DQ16_b			DQ28_b		DQ25_a		VDDQ_a		VDDQ_a		DQ10_a		DQS1_t		DM1_a		DQS0_t		VDDQ_a		DQ2_a			DM2_a	VDD2_a/	
D	DQ17_b	VDDQ_b																								VDDQ_a	DQS2_c	
E	DQ18_b	DQ19_b	VSSQ_b																						VSSQ_a	DQS2_t	DQ23_a	
F	DQ20_b	DQ21_b																								DQ22_a	VDDQ_a	
G	VDDQ_b	DQ22_b	DQ23_b																						DM21_a	DQ20_a	VSSQ_a	
H	VSSQ_b	DQS2_t																								DM19_a	DQ18_a	
J	DQS2_c	VDDQ_b	DM2_b																						VDDQ_b	DQ17_b	DQ16_a	
K	VSSQ_b	DQ0_b																								VSSQ_a	VDD2_a/	
L	DQ1_b	VDDQ_b	DQ2_b																						CA0_b	VDD1_a/	VSS_a/b	
M	DQ3_b	VSSQ_b																								CA1_b	VSSCA_	
N	DQ4_b	DQ5_b	VDDQ_b																							CA3_b	CA2_b	VDDCA_
P	DQ6_b	DQ7_b																									CA4_b	CSB1_b
R	VDDQ_b	DQS0_t	DQS0_c																							CKE0_b	CSB0_b	CKE1_b
T	VSSQ_b	VSS_a/b																									CK_c_b	CK_t_b
U	Vref(DQ)	VSS_a/b	DM0_b																							VDD2_a/	VDDCA_	VSSCA_
V	VDD1_a/	VDD1_a/																									VSS_a/b	Vref(CA)
W	DM1_b	VDD2_a/	VDD2_a/																							CA5_b	VDDCA_	VSSCA_
Y	VDDQ_b	VSSQ_b																									CA7_b	CA6_b
A	DQS1_c	DQS1_t	DQ8_b																						VDD2_a/	CA9_b	CA8_b	
A	VDDQ_b	DQ9_b																								VSS_a/b	ZQ_b	
A	DQ10_b	DQ11_b	VSSQ_b																						DNU	DNU	VDD1_a/	
A	DQ13_b	DQ12_b																								DNU	DNU	
A	VDD1_a/	DQ14_b			VSSQ_b		DQ27_b		DQ30_b		VDD2_a/		CA6_a		CA5_a		VDD2_a/		CA4_a		VSS_a/b		DNU			DNU	DNU	
A	VSSQ_b	VDDQ_b	DQ15_b	VDDQ_b	DQS3_t	DQ25_b	DQ26_b	DQ28_b	VDDQ_b	VSSQ_b	VSS_a/b	CA9_a	CA7_a	VDDCA_	VSS_a/b	VDDCA_	CK_t_a	CKE0_a	CSB0_a	CA2_a	VSSCA_	CA0_a	VDD2_a/	DNU	DNU	DNU	DNU	
A	DNU	VSS_a/b	VDD2_a/	DM3_b	DQS3_c	DQ24_b	VDDQ_b	VSSQ_b	DQ29_b	DQ31_b	VDD1_a/	ZQ_a	CA8_a	VSSCA_	Vref(CA)	VSSCA_	CK_c_a	CKE1_a	CSB1_a	CA3_a	VDDCA_	CA1_a	VDD1_a/	DNU	DNU	DNU	DNU	

NOTE 1: 14x14 mm, 0.5mm pitch, 27 rows

NOTE 2: 240 Ball Count, internal row partially populated

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

2.4 LPDDR2 12x12 PoP 1-channel x32 package ballout using MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	DNU	DNU	RDY,R/B_n, WAIT_n	CLK CLKm	ADQ11 DAT6m	VCCmm	ADQ10 DAT4m	ADQ9 DAT2m	VCCQmm	ADQ8 DAT0m	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_c	VDD1	VSS	DNU	DNU
B	DNU	DNU	VDD1	ADQ3 DAT7m	VSSmm	ADQ2 DAT5m	ADQ1 DAT3m	VSSmm	ADQ0 DAT1m	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	DM3	VDD2	DNU	DNU
C	VSS	VDD2																				DQ15	VSSQ
D	ADQ12	ADQ4																				VDDQ	DQ14
E	ADQ13	ADQ5																				DQ12	DQ13
F	VCCQmm VDDImm	VSSmm																				DQ11	VSSQ
G	ADQ14	ADQ6																				VDDQ	DQ10
H	ADQ15	ADQ7																				DQ8	DQ9
J	VCCmm	VSSmm																				DQS1_t	VSSQ
K	WE_n	OE_n/ RE_n																				VDDQ	DQS1_c
L	RP_n, RST_n,	AVD_n, ADV_n,																				VDD2	DM1
M	CE_n	VSS																				Vref(DQ)	VSS
N	INT,WP_n	VDD1																				VDD1	DM0
P	ZQ	Vref(CA)																				DQS0_c	VSSQ
R	VSS	VDD2																				VDDQ	DQS0_t
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	VSSQ
V	VSSCA	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CK_c	CK_t																				DQ1	VSSQ
AA	VSS	VDD2																				VDDQ	DQ0
AB	DNU	DNU	CS0_n	CS1_n	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_t	VDDQ	DM2	VDD2	DNU	DNU
A C	DNU	DNU	CKE0	CKE1	VSS	CA0	CA2	VDDCA	VSSmm	VDDmm	VACC	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2_c	VDD1	VSS	DNU	DNU

Flash Memory (eMMC/MuxOneNand/NAND/AADMuxNOR)
ADD/CTRL

LPDDR2 DQ

LPDDR2 CA

Power

Ground

Do Not Use

ZQ

Clock

Ball Location	Mux OneNand	eMMC	Raw NAND	ADD-Mux NOR	Comment
A3	RDY / WAIT_n	CMDm	R/B_n	WAIT	
A4	CLK	CLKm	NC	CLK	
K1	WE_n	NC	WE_n	WE_n	
K2	OE_n	NC	RE_n	OE_n	
L1	RP_n	RST_n (v4.4)	CLE	RST_n / DPD	DPD must be configured active high via
L2	AVD_n	NC	ALE	ADV_n	
N1	INT	NC	WP_n	WP_n	

NOTE 1: 12x12 mm, 0.5mm pitch, 23 rows

NOTE 2: 168 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

2.5 LPDDR2 10x10 PoP 1-channel x32 package ballout using variation VAABCB for MO-273A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	DNU	DNU	VSS	VSSQ	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_c	DM3	VSSQ	DQ14	DQ13	DQ11	VSS	DNU	DNU
B	DNU	DNU	VSS	VDD2	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_t	VDDQ	DQ15	VDDQ	DQ12	VDD2	VSS	DNU	DNU
C	ZQ	VDD1																VDD1	DQ10
D	CA9	CA8																DQ9	VDDQ
E	VSSCA	VDDCA																VSSQ	DQ8
F	CA7	CA6																DQS1_t	DQS1_c
G	CA5	VDD2																VDDQ	DM1
H	VDD1	Vref(CA)																VDD2	VSSQ
J	VSS	VDDCA																VSS	VDD2
K	CK_t	CK_c																Vref(DQ)	VSS
L	VSS	VSSCA																VDD1	VDD1
M	CKE1	CKE0																VDD2	VSSQ
N	CS1_n	CS0_n																VDDQ	DM0
P	CA3	CA4																DQS0_t	DQS0_c
R	VDDCA	CA2																VSSQ	DQ7
T	CA1	VSSCA																DQ6	VDDQ
U	CA0	VDD1																VDD1	DQ5
V	DNU	VACC	VSS	VDD2	DQ17	DQ18	VSSQ	DQ21	DQ22	VSSQ	DQS2_t	VDDQ	DQ0	VDDQ	DQ3	VDD2	VSS	DNU	DNU
W	DNU	DNU	VSS	VSSQ	DQ16	VDDQ	DQ19	DQ20	VDDQ	DQ23	DQS2_c	DM2	VSSQ	DQ1	DQ2	DQ4	VSS	DNU	DNU

LPDDR2 DQ

LPDDR2 CA

Power

Ground

Do Not Use

ZQ

Clock

NOTE 1: 10x10 mm, 0.5mm pitch, 19 rows

NOTE 2: 136 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

2.6 79-ball x16 LPDDR2 0.5mm pitch package ballout (Discrete/MCP)

	1	2	3	4	5	6	7	8	9
A	NC	CA9	VDD2	VDD1	VSSQ	DQ14	DQ12	VDD2	NC
B	CA7	CA8	ZQ	VSS	DQ15	DQ13	VDDQ	VSSQ	DQ11
C	CA5	CA6						DQ10	DQ9
D	VDDCA	VSSCA			CKE2 CS3_n	VSSQ	DQS1_t	DQ8	VDDQ
E	VDD2	Vref(CA)			CKE1	VDDQ	DQS1_c	DM1	VSS
F	VSS	VSSCA			CKE0	VSS	VDD1	VDD2	Vref(DQ)
G	VDDCA	CK_t			CS1_n	VSSQ	DQS0_c	DM0	VDD1
H	CK_c	CS0_n			CS2_n	VDDQ	DQS0_t	DQ7	VDDQ
J	CA4	CA3						DQ5	DQ6
K	CA2	CA1	VACC	VSS	DQ0	DQ2	VDDQ	VSSQ	DQ4
L	NC	CA0	VDD2	VDD1	VSSQ	DQ1	DQ3	VDD2	NC

LPDDR2 DQ

LPDDR2 CA

Power

Ground

Do Not Use/No Connect

ZQ

Clock

NOTE 1: 0.5mm pitch, 11 rows

NOTE 2: 79 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: The ZQ-ball used when operating above 200 MHz is limited to a 5pF load (typically 2 die using CKE0,1 and CS0,1)

NOTE 5: See JESD21-C, Section 3.12.1

2.7 134-ball x16/x32 LPDDR2 package ballout (Discrete/MCP)

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU
B	DNU	NC	VACC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
C	VDD1	VSS	ZQ1	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
D	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3_t NC	DQS3_c NC	VSSQ
E	VSSCA	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
F	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
G	VDD2	CA5	Vref(CA)	NB	DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ
H	VDDCA	VSS	CK_c	NB	DM1	VDDQ	NB	NB	NB	NB
J	VSSCA	NC	CK_t	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
K	CKE0	CKE1	CKE2	NB	DM0	VDDQ	NB	NB	NB	NB
L	CS0_n	CS1_n	CS2_n	NB	DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ
M	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
N	VSSCA	VDDCA	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
P	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2_t NC	DQS2_c NC	VSSQ
R	VDD1	VSS	VACC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
T	DNU	NC	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
U	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU

Ball Definition where 2 labels are present	
1st Row	x32 device
2nd Row	x16

	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

NOTE 1: 0.5mm (x32) or 0.65mm pitch (x32, x16), 17 rows

NOTE 2: 134 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.1

2.8 162-ball x16/x32 LPDDR2 and SDR-Flash package ballout

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WP _n WP _n DAT0	CLE CLE DAT6	VCCN VCCN VDDIm	IO4 DQ4 DAT5	IO7 DQ7 DAT3	VCCN VCCN VCCm	DNU	DNU
B	DNU	VCCN VCCN VCCm	IO11 DQS DAT1	ALE ALE DAT7	RE _n RE _n CLKm	IO5 DQ5 DAT4	IO14 NC DAT2	IO15 NC VCCQm	VSS	DNU
C	IO10 NC RST _n	IO1 DQ1 NC	IO3 DQ3 VSSQm	WE _n WE _n NC	R/B _n R/B _n CMD	IO6 DQ6 NC	NB	NB	NB	NB
D	IO8 NC NC	IO0 DQ0 NC	IO2 DQ2 NC	CE _n CE _n NC	IO12 NC NC	IO13 NC NC	NB	NB	NB	NB
E	VSS	IO9 NC NC	VACC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
F	VDD1	VSS	ZQ1	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
G	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3 _t NC	DQS3 _c NC	VSSQ
H	VSSCA	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
J	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	Vref(CA)	NB	DQS1 _c	DQS1 _t	DQ10	DQ9	DQ8	VSSQ
L	VDDCA	VSS	CK _c	NB	DM1	VDDQ	NB	NB	NB	NB
M	VSSCA	NC	CK _t	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
N	CKE0	CKE1	CKE2	NB	DM0	VDDQ	NB	NB	NB	NB
P	CS0 _n	CS1 _n	CS2 _n	NB	DQS0 _c	DQS0 _t	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSSCA	VDDCA	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
U	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2 _t NC	DQS2 _c NC	VSSQ
V	VDD1	VSS	VACC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
W	DNU	NC	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
Y	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU

SDR NVM Ball Definition where 3 labels are present	
1st Row	NVM device
2nd Row	ONFI
3rd Row	device
LPDDR2 Ball Definition where 2 labels are present	
1st Row	x32 device
2nd Row	x16 device

	Flash Memory (eMMC/NVM/ONFI) ADD/CTRL
	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

NOTE 1: 0.5mm (x32, x16) or 0.65mm pitch (x32, x16), 20 rows

NOTE 2: 162 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.1

2.9 180-ball x16/x32 LPDDR2, SDR-Flash, and e-MMC package ballout

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	WP_n	CLE	VCCN	IO4 DQ4	IO7 DQ7	VCCN	DNU	DNU
B	DNU	VCCN	IO11 DQS	ALE	RE_n	IO5 DQ5	IO14 NC	IO15 NC	VSS	DNU
C	IO10 NC	IO1 DQ1	IO3 DQ3	WE_n	R/B_n	IO6 DQ6	NB	NB	NB	NB
D	IO8 NC	IO0 DQ0	IO2 DQ2	CE_n	IO12 NC	IO13 NC	NB	NB	NB	NB
E	VSS	IO9 NC	VACC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
F	VDD1	VSS	ZQ1	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
G	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3_t NC	DQS3_c NC	VSSQ
H	VSSCA	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
J	VDDCA	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
K	VDD2	CA5	Vref(CA)	NB	DQS1_c	DQS1_t	DQ10	DQ9	DQ8	VSSQ
L	VDDCA	VSS	CK_c	NB	DM1	VDDQ	NB	NB	NB	NB
M	VSSCA	NC	CK_t	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
N	CKE0	CKE1	CKE2	NB	DM0	VDDQ	NB	NB	NB	NB
P	CS0_n	CS1_n	CS2_n	NB	DQS0_c	DQS0_t	DQ5	DQ6	DQ7	VSSQ
R	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
T	VSSCA	VDDCA	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
U	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2_t NC	DQS2_c NC	VSSQ
V	VDD1	VSS	VACC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
W	VCCm	VDDIm	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
Y	VSS	DAT2	CMD	DAT6	DAT1	NB	NB	NB	NB	NB
AA	DNU	VCCQm	DAT4	CLKm	DAT0	VCCm	NB	NB	NB	DNU
AB	DNU	DNU	DAT3	DAT5	DAT7	VCCQm	RST_n	VSS	DNU	DNU

SDR NVM Ball Definition where 2 labels are present	
1st Row	NVM device
2nd Row	ONFI device
LPDDR2 Ball Definition where 2 labels are present	
1st Row	x32 device
2nd Row	x16 device

	Flash Memory (eMMC/NVM/ONFI) ADD/CTRL
	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

NOTE 1: 0.5mm (x32, x16) or 0.65mm pitch (x32, x16), 22 rows

NOTE 2: 180 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.1

2.10 121-ball x16 LPDDR2, SDR Flash-NVM, and e-MMC package ballout

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	DAT2 ADQ9 DQ2	DAT5 ADQ2 DQ5	VDDI VCCQx	VCC	VDD2	VSS	VDDQ	NC	NC
B	NC	VSSx	DAT3 ADQ1 DQ3	DAT6 ADQ11 DQ6	DAT7 ADQ3 DQ7	VSSx	VDD1	DQ15	DQ14	VSSQ	NC
C	VCCQ	DAT0 ADQ8 DQ0	DAT4 ADQ10 DQ4		CLK e CLK o,f DQS i	CMD e RDY o WAIT f	RST_n e,f RP_n o CLE n,i		DQ11	DQ12	DQ13
D	VDD2	DAT1 ADQ0 DQ1								DQ10	VSSQ
E	VSS	ZQ	CA9						DQ8	DQ9	VDDQ
F	VDD1	CA8			VCCx	VSSx	WE_n CLK i			DQS1_t	VSSQ
G	VSSCA	CA7	CA6		- ADQ12 DQ12	OE_n o,f RE_n n,i W/R_n i	CE_n		DQS1_c	DM1	VDDQ
H	VDDCA	CA5			ADQ13 DQ13	ADQ6 DQ11	ADQ4 DQ9		Vref(DQ)	VDD2	
J	VDD2	Vref(CA)	VSS		ADQ14 DQ14	ADQ7 DQ10	ADQ5 DQ8		DQS0_c	DM0	VDD1
K	CK_t	CK_c			ADQ15 DQ15	VSSx	VCCx			DQS0_t	VDDQ
L	CS0_n	CS1_n	CS2_n						DQ7	DQ6	VSSQ
M	CA4	CA3								DQ5	VDDQ
N	VDDCA	CA2	CA1		CKE0	AVD_n o ADV_n f ALE n,i	- INT o WP_n f,n,i		DQ3	DQ2	VSSQ
P	NC	VSSCA	CA0	CKE2	CKE1	VACC VPP	DQ0	DQ1	DQ4	VSSQ	NC
R	NC	NC	VSS	VDD2	VDD1	VSS	VDD2	VSS	VDDQ	NC	NC

SDR NVM Ball Definition where 3 labels are present	
1st Row	eMMC (e)
2nd Row	OneNAND (o) / AAD Nor (f)
3rd Row	Raw NAND (n) / ONFI2 (i)

	Flash Memory (eMMC/Raw NAND/One- NAND)
	LPDDR2 DQ
	LPDDR2 CA
	Power
	Ground
	Do Not Use/NC/No Ball
	ZQ
	Clock

Ball	eMMC (e)	OneNAND (o) AAD NOR (f)	NAND (n)	NAND DDR (i)
-	DAT[7:0]	ADQ[15:0]	DQ[15:0]	DQ[15:0]
C5	CLK	CLK	-	DQS
C6	CMD	RDY / WAIT	R/B_n	R/B_n
C7	RST_n	RP_n/RST_n	CLE	CLE
F7	-	WE_n	WE_n	WE_n, CLK
G6	-	OE_n	RE_n	RE_n, W/R_n
G7	-	CE_n	CE_n	CE_n
N6	-	AVD_n/ADV_n	ALE	ALE
N7	-	INT / WP_n	WP_n	WP_n

VSSx/VCCx represents common Flash VSS/VCC

NOTE 1: 0.5mm pitch, 15 rows

NOTE 2: 121 Ball Count

NOTE 3: Top View, A1 in Top Left Corner

NOTE 4: See JESD21-C, Section 3.12.2

2.12 Input/output functional description

2.12.1 Pad Definition and Description

Table 2 — Pad Definition and Description

Name	Type	Description
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Table 60 for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code. See Table 60 for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code. See Table 60 for command code descriptions.
DQ0-DQ7 (x8) DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	Data Inputs/Output: Bi-directional data bus
DQS0_t, DQS0_c (x8) DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x8, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0 (x8) DM0-DM1 (x16) DM0 - DM3 (x32)	Input	Input Data Mask: For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.

Name	Type	Description
DM0/DNV0 (x8) DM0/DNV0-DM1/DNV1 (x16) DM0/DNV0 - DM3/DNV3 (x32)	I/O	Input Data Mask/Data Not Valid: For LPDDR2 devices that support the DNV feature, DM/DNV is bidirectional (used for write and read data). It is output with read data, input with write data. DM/DNV is the input mask signal for write data and is an output signal validating a read burst. For data write accesses: Input data is masked when DM/DNV is sampled HIGH coincident with DQ input data during a WRITE access. DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31. For data read accesses: See 5.4.2 for detailed description of DNV functionality. DNV0, DNV1, DNV2, and DNV3 are driven coincident with output read data. DNV0, DNV1, DNV2, and DNV3 are driven with the same value and shall be sampled with DQS0, DQS1, DQS2, and DQS3 respectively. The DM/DNV loading shall match the DQ and DQS_t (or DQS_c) loading.
V _{DD1}	Supply	Core Power Supply 1: Core power supply for LPDDR2-N and LPDDR2-SX devices.
V _{DD2}	Supply	Core Power Supply 2: Core power supply for LPDDR2-S2B, LPDDR2-S4 and LPDDR2-N-B devices.
V _{DDCA}	Supply	Input Receiver Power Supply: Power supply for CA0-9, CKE, CS _n , CK _t , and CK _c input buffers.
V _{DDQ}	Supply	I/O Power Supply: Power supply for Data input/output buffers.
V _{ACC}	Supply	NVM Acceleration Supply: NVM device specific embedded operation acceleration. V _{ACC} enables some NVM device specific functionality. When not used for NVM device specific functionality, V _{ACC} shall be driven to a level of V _{DD1} .
V _{REF(CA)}	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA0-9, CKE, CS _n , CK _t , and CK _c input buffers.
V _{REF(DQ)}	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
V _{SS}	Supply	Ground
V _{SSCA}	Supply	Ground for Input Receivers
V _{SSQ}	Supply	I/O Ground
ZQ	I/O	Reference Pin for Output Drive Strength Calibration

NOTE 1 Data includes DQ and DM.

2.13 LPDDR2 SDRAM Addressing

Table 3 — LPDDR2 SDRAM Addressing

Items		64Mb	128Mb	256Mb	512Mb	1Gb		2Gb		4Gb	6Gb	8Gb
Device Type		S2/S4	S2/S4	S2/S4	S2/S4	S2	S4	S2	S4	S2/S4	S2/S4	S2/S4
Number of Banks		4				4	8	4	8	8		
Bank Addresses		BA0-BA1				BA0-BA1	BA0-BA2	BA0-BA1	BA0-BA2	BA0-BA2		
$t_{REFI}(us)^{*2}$		15.6	15.6	7.8	7.8	7.8	7.8	3.9	3.9	3.9	3.9	3.9
x8	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14 ^{*4}	R0-R14
	Column Addresses ^{*1}	C0-C8	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10	C0-C10	C0-C10	C0-C11	C0-C11	C0-C11
x16	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14 ^{*4}	R0-R14
	Column Addresses ^{*1}	C0-C7	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10
x32	Row Addresses	R0-R11	R0-R11	R0-R12	R0-R12	R0-R13	R0-R12	R0-R14	R0-R13	R0-R13	R0-R14 ^{*4}	R0-R14
	Column Addresses ^{*1}	C0-C6	C0-C7	C0-C7	C0-C8	C0-C8	C0-C8	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9

NOTE 1 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 2 t_{REFI} values for all bank refresh is $T_c = -25 \sim 85 \text{ }^{\circ}\text{C}$, T_c means Operating Case Temperature

NOTE 3 Row and Column Address values on the CA bus that are not used are “don’t care.”

NOTE 4 No memory present at addresses with R13=R14=HIGH. ACT command with R13=R14=HIGH is ignored (NOP). Write to R13=R14=HIGH is ignored (NOP).

2.14 LPDDR2 NVM Addressing

2.14.1 Three-Phase Addressing

The memory controller delivers an array address to the memory in three phases (See [Figure 1](#) and [Figure 2](#)). The [Table 60](#) defines the required assignment of logical address bits to CA pins. Scrambling of the logical address bits in any order different than those described in the Command truth table is prohibited.

During a Preactive command, part of a row address (driven on the CA input pins) is stored in a Row Address Buffer (RAB) selected by BA2-BA0.

During an Activate command, BA2-BA0 select an RAB to retrieve the first part of the row address. Meanwhile, the remainder of the row address is driven on the CA input pins. These two parts of the row address select one row from the memory array. Activate also causes internal sensing circuits to transfer that memory content into a Row Data Buffer (RDB) also selected by BA2-BA0.

An {RAB, RDB} pair selected by BA2-BA0 is referred to as a Row Buffer (RB). BA2-BA0 do not address any portion of the array and only select an RAB into which address is placed and/or an RDB into which data is placed. The controller may use any value of BA2-BA0 for any array location.

During a Read or Write command BA2-BA0 selects an RDB, and the column address is driven on the CA input pins to choose the starting address of the read or write burst.

The Preactive command is optional when the desired RAB already contains the desired partial row address. The Activate command is optional when the desired RDB already contains the desired memory content.

Upon completion of Device Auto-Initialization, all Row Buffers are in the Idle state, and RABs contain 0x0000 and all RDBs contain indeterminate values.

2.5.1 Three-Phase Addressing (cont'd)

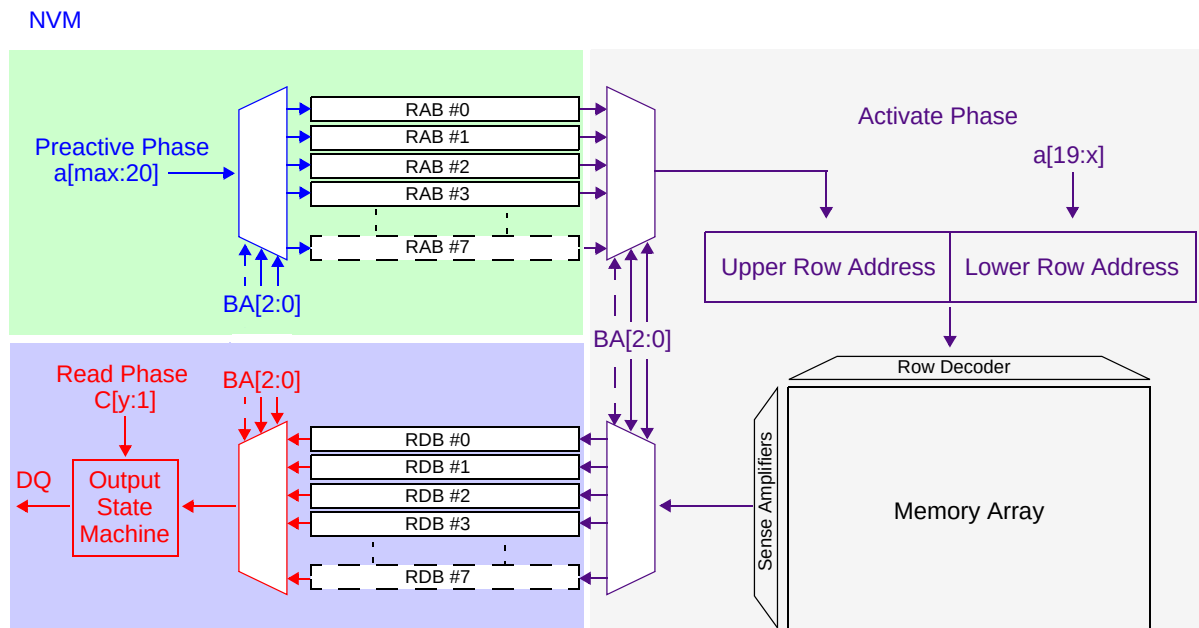


Figure 1 — LPDDR2-N: Three-Phase Address Read

NOTE 1 In the Preactive phase, $a[\text{max}]$ is dependent on the density of the NVM device.

NOTE 2 In the Activate phase, the lower order row address bit $a[x]$ is dependent on the size of the Row Data Buffer (RDB).

NOTE 3 In the Read phase, column address bit $C[y]$ is dependent on the size of the Row Data Buffer (RDB) and the data bus width.

NOTE 4 An {RAB, RDB} pair selected by $BA[2:0]$ is referred to as a Row Buffer (RB).

NOTE 5 The least significant column address C_0 is implied to be zero and is not transmitted on the CA bus.

NOTE 6 An {RAB, RDB} pair can be associated with any portion of the memory array.

2.5.1 Three-Phase Addressing (cont'd)

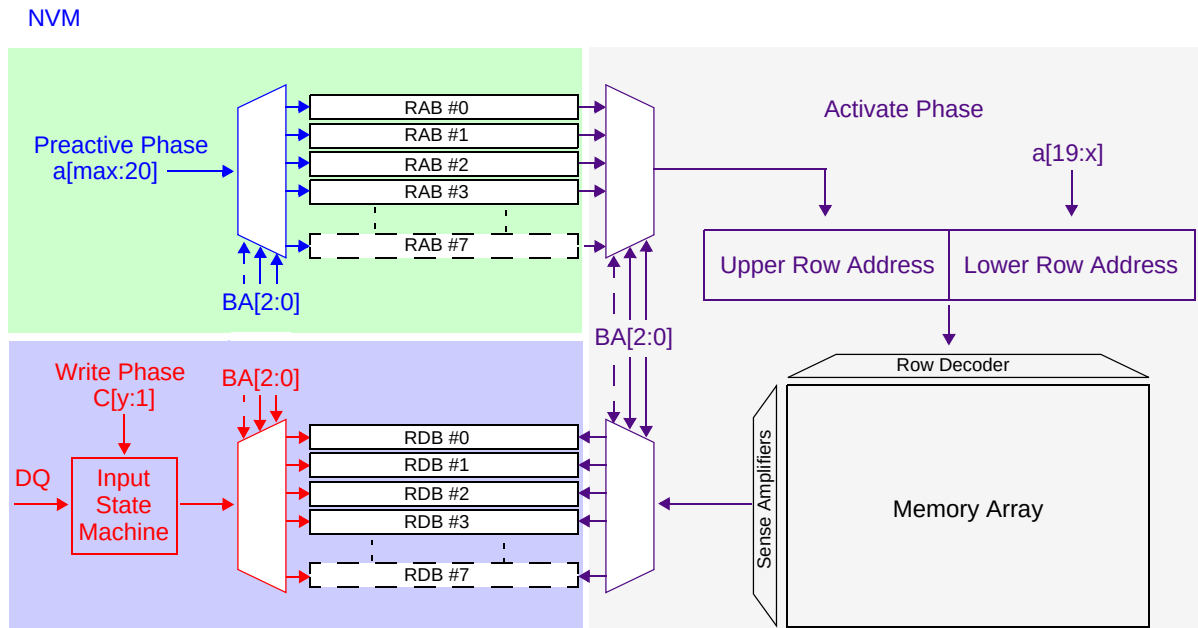


Figure 2 — LPDDR2-N: Three-Phase Address Write

- NOTE 1 In the Preactive phase, $a[\text{max}]$ is dependent on the density of the NVM device.
- NOTE 2 In the Activate phase, the lower order row address bit $a[x]$ is dependent on the size of the Row Data Buffer (RDB).
- NOTE 3 In the Write phase, column address bit $C[y]$ is dependent on the size of the Row Data Buffer (RDB) and the data bus width.
- NOTE 4 An {RAB, RDB} pair selected by $BA[2:0]$ is referred to as a Row Buffer (RB).
- NOTE 5 The least significant column address $C0$ is implied to be zero and is not transmitted on the CA bus.

Table 4 — 64 Mb Addressing

Configuration	8 Mb x 8	4 Mb x 16	2 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREACTIVE)	a22-a20	a22-a20	a22-a20
Lower Row Address (ACTIVE) ^{*1}	a19-A5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 5 — 128 Mb Addressing

Configuration	16 Mb x 8	8 Mb x 16	4 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREACTIVE)	a23-a20	a23-a20	a23-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

2.5.1 Three-Phase Addressing (cont'd)**Table 6 — 256 Mb addressing**

Configuration	32 Mb x 8	16 Mb x 16	8 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a24-a20	a24-a20	a24-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 7 — 512 Mb addressing

Configuration	64 Mb x 8	32 Mb x 16	16 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a25-a20	a25-a20	a25-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 8 — 1 Gb addressing

Configuration	128 Mb x 8	64 Mb x 16	32 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a26-a20	a26-a20	a26-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 9 — 2 Gb addressing

Configuration	256 Mb x 8	128 Mb x 16	64 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a27-a20	a27-a20	a27-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 10 — 4 Gb addressing

Configuration	512 Mb x 8	256 Mb x 16	128 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a28-a20	a28-a20	a28-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

2.5.1 Three-Phase Addressing (cont'd)

Table 11 — 8 Gb addressing

Configuration	1 Gb x 8	512 Mb x 16	256 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a29-a20	a29-a20	a29-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 12 — 16 Gb addressing

Configuration	2 Gb x 8	1 Gb x 16	512 Mb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a30-a20	a30-a20	a30-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Table 13 — 32 Gb addressing

Configuration	4 Gb x 8	2 Gb x 16	1 Gb x 32
# of Row Buffers ^{*2,3}	4	4	4
Upper Row Address (PREAMBLE)	a31-a20	a31-a20	a31-a20
Lower Row Address (ACTIVE) ^{*1}	a19-a5	a19-a5	a19-a5
Column Address (READ/WRITE) ^{*1,4}	a4-a1 (C4-C1)	a4-a2 (C3-C1)	a4-a3 (C2-C1)
RDB size ^{*1}	32 Bytes	32 Bytes	32 Bytes

Notes for Tables 4-13

NOTE 1 All tables above show examples using minimum 32 Byte RDB Size, see [Table 14](#) for other RDB sizes.

NOTE 2 The number of Row Buffers can be 4 or 8. A controller may use a smaller number of Row Buffers provided that the appropriate most significant BA addresses are driven to “0”.

NOTE 3 One Row Buffer consists of a pair of one Row Address Buffer (RAB) and one Row Data Buffer (RDB), selected by Buffer Address, BA0-BA2 (CA7r-CA9r).

NOTE 4 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 5 Row and Column Address values on the CA bus that are not used are “don’t care.”

2.5.1 Three-Phase Addressing (cont'd)

Table 14 — Addressing Dependent on RDB Size

RDB Size	Configuration	x8	x16	x32
32 Byte	Lower Row Address	a19-a5	a19-a5	a19-a5
	Column Address	a4-a1(C4-C1)	a4-a2(C3-C1)	a4-a3(C2-C1)
64 Byte	Lower Row Address	a19-a6	a19-a6	a19-a6
	Column Address	a5-a1(C5-C1)	a5-a2(C4-C1)	a5-a3(C3-C1)
128 Byte	Lower Row Address	a19-a7	a19-a7	a19-a7
	Column Address	a6-a1(C6-C1)	a6-a2(C5-C1)	a6-a3(C4-C1)
256 Byte	Lower Row Address	a19-a8	a19-a8	a19-a8
	Column Address	a7-a1(C7-C1)	a7-a2(C6-C1)	a7-a3(C5-C1)
512 Byte	Lower Row Address	a19-a9	a19-a9	a19-a9
	Column Address	a8-a1(C8-C1)	a8-a2(C7-C1)	a8-a3(C6-C1)
1 KB	Lower Row Address	a19-a10	a19-a10	a19-a10
	Column Address	a9-a1(C9-C1)	a9-a2(C8-C1)	a9-a3(C7-C1)
2 KB	Lower Row Address	a19-a11	a19-a11	a19-a11
	Column Address	a10-a1(C10-C1)	a10-a2(C9-C1)	a10-a3(C8-C1)
4 KB	Lower Row Address	a19-a12	a19-a12	a19-a12
	Column Address	a11-a1(C11-C1)	a11-a2(C10-C1)	a11-a3(C9-C1)

NOTE 1 The least significant column address C0 is implied to be zero and is not transmitted on the CA bus.

NOTE 2 Row and Column Address values on the CA bus that are not used are “don’t care.”

3 Functional description

LPDDR2-S is a high-speed SDRAM device internally configured as a 4 or 8-Bank memory.

LPDDR2-N is a high-speed Non-Volatile Memory device, internally configured to have 4 or 8 Row Buffers.

These devices contain the following number of bits:

64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits
2 Gb has 2,147,483,648 bits
4 Gb has 4,294,967,296 bits
6 Gb has 6,442,450,944 bits
8 Gb has 8,589,934,592 bits

The following densities apply to LPDDR2-NVM devices only:

16 Gb has 17,179,869,184 bits
32 Gb has 34,359,738,368 bits

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S2 also uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S2 effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal SDRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

LPDDR2-S4 and LPDDR2-N also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 and LPDDR2-N effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM/NVM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-SX devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

For LPDDR2-N devices, accesses begin with the registration of an Preactive command, followed by an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Preactive and Activate commands are used to select the row and the Row Buffer to be accessed. The address bits registered coincident with the Read or Write command are used to select the Row Buffer and the starting column location for the burst access.

For LPDDR2-NVM devices, operations other than “array reads” are performed by accessing an overlay window that is mapped over the array space of the memory. The Overlay Window Base Address (OWBA) is programmed using the Mode Registers. The overlay window is enabled and disabled by using the Mode Register. When the overlay window is disabled, all array accesses map to the memory array. When the overlay window is enabled, reads and writes to Overlay Window within the array memory space access the Overlay Window.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 Simplified LPDDR2 Bus Interface State Diagram

The simplified LPDDR2 bus interface state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see [clause 5](#).

3.1 Simplified LPDDR2 Bus Interface State Diagram (cont'd)

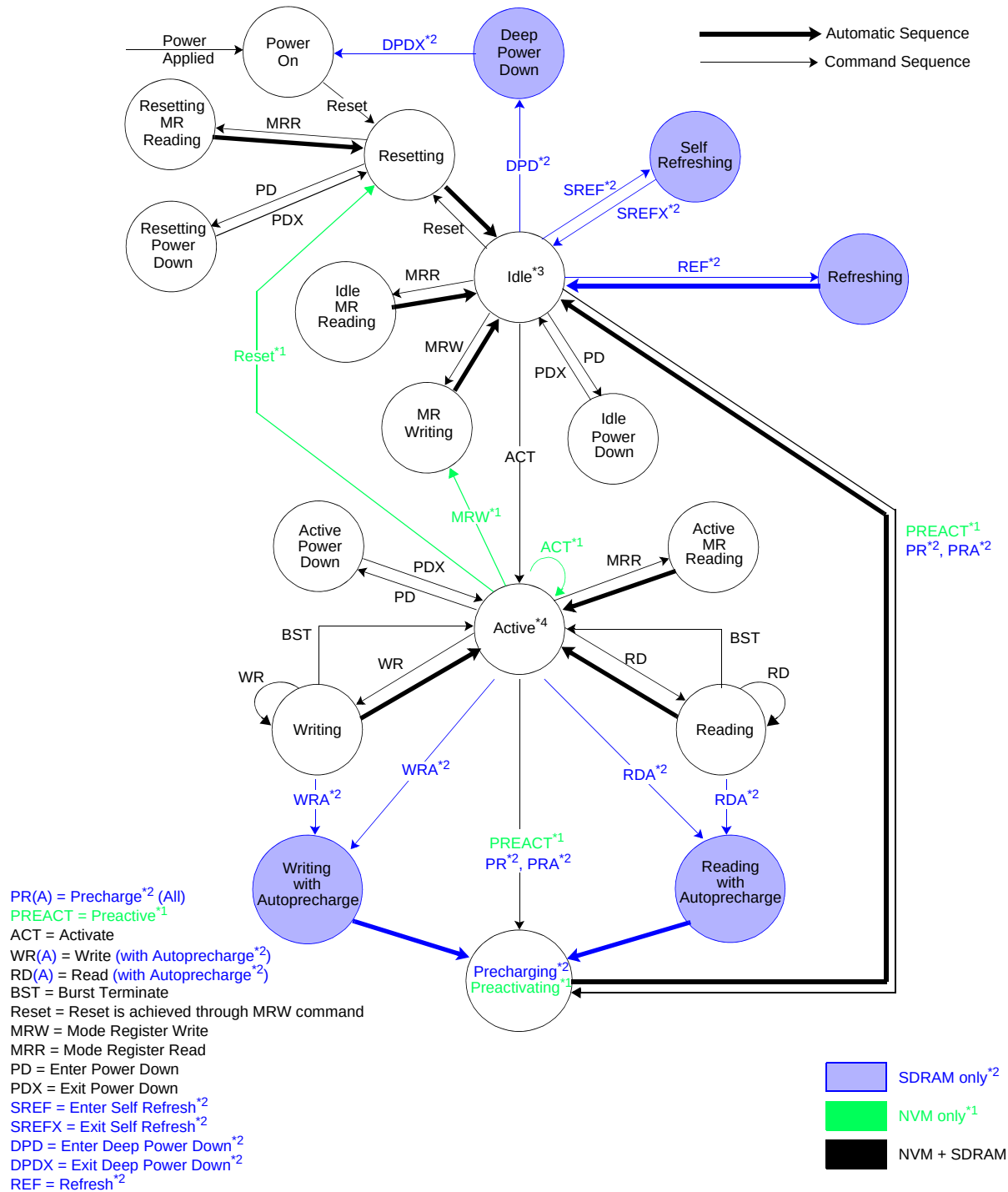


Figure 3 — LPDDR2: Simplified Bus Interface State Diagram

NOTE 1 These transitions apply for LPDDR2-N devices only.

NOTE 2 These transitions apply for LPDDR2-SX devices only.

NOTE 3 For LPDDR2-SDRAM in the Idle state, all banks are precharged.

NOTE 4 For LPDDR2-NVM in the Active state, one or more Row Buffers have been activated.

NOTE 5 Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Bank/Row Buffer are not captured in full detail.

NOTE 6 Resetting duration is variable. Poll DAI status bit to detect state transition to Idle.

NOTE 7 Reset command sets all Row Address Buffers to 0x0000.

3.2 Simplified LPDDR2-SX State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see [clause 5](#).

3.2 Simplified LPDDR2-SX State Diagram (cont'd)

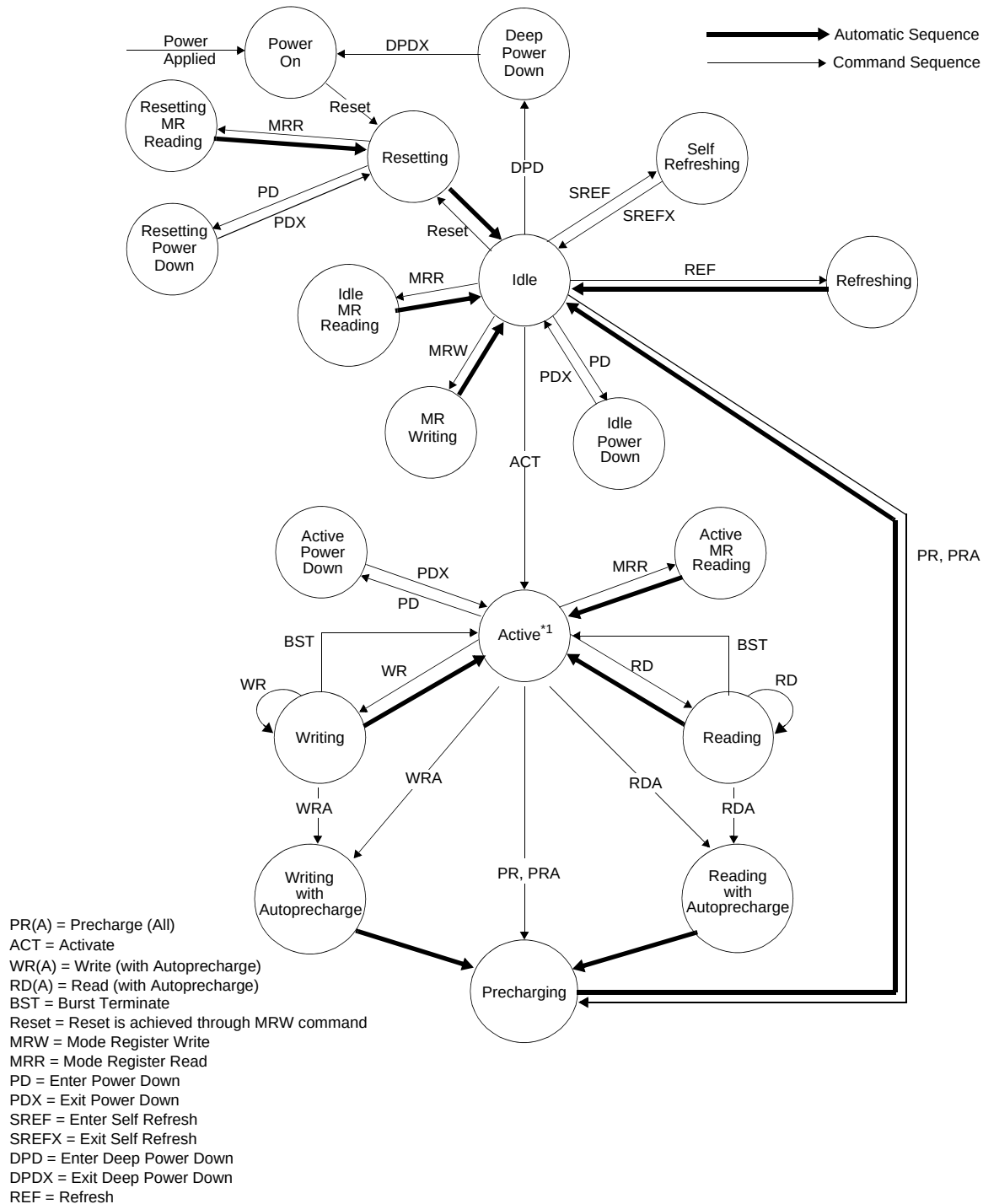


Figure 4 — LPDDR2-S: Simplified Bus Interface State Diagram

NOTE 1 For LPDDR2-SDRAM in the Idle state, all banks are precharged.

3.3 Simplified LPDDR2-N Simplified Bus State Diagram

LPDDR2-NVM simplified bus interface state diagram provides a simplified illustration of allowed bus interface state transitions and the related commands to control them. For a more detailed definition of the device bus interface, the information provided by the state diagram should be integrated with the truth tables and timing specification.

For the command definition see clause 5

LPDDR2-NVM has two types of states: stable states, which are entered and exited with a command, and transitory states, which are entered with a command and exited automatically.

LPDDR2-NVM stable states are: Power-on, Idle, Active, Resetting Power Down, Idle Power Down, and Active Power Down.

LPDDR2-NVM transitory states are: Resetting, Resetting MR Reading, Idle MR Reading, MR Writing, Active MR Reading, Reading, Writing and Preactivating.

LPDDR2-NVM state diagram is shown in Figure 5, where each state transition, due to a command, is represented with a numbered arc.

Follows the description of all the allowed commands for any given state. The arc number of each transition is included in the description in parenthesis.

3.3.1 Power On and Resetting states

- (1) After power up, the device goes in the Power On state.
- (2) The Reset command is the only command allowed in this state, and when issued, it brings all Row Buffers (RB) into the Resetting state after t_{INIT4} .
- (3) Mode Register Read (MRR) command can be issued from the Resetting state. MRR allows retrieving useful information such as: memory type, memory characteristics, or the Resetting status through the DAI bit. The device enters in Resetting Mode Register Reading state when MRR command is registered, and goes back automatically to Resetting state after t_{MRR} .
- (4) Enter Power Down command brings all Row Buffers into the Resetting Power Down state. For the complete description of Power Down entry, see 5.14.
- (5) Exit Power Down command brings all Row Buffers from the Resetting Power Down state back to the Resetting state after t_{XP} . For the complete description of Power Down exit, see 5.14.

The duration of Resetting, t_{INIT5} , is device specific and it is not defined in this document. The memory controller shall poll DAI bit to determine the completion of the device initialization. Upon completion of device initialization, all Row Buffers are in the Idle state and all RABs have a default value of 0x0000.

3.3.2 Idle state

From the Idle state, the following commands are allowed: Reset, Mode Register Write, Mode Register Read, Preactive, Activate and Enter Power Down.

- (6) Reset command brings all Row Buffers into the Resetting state after t_{INIT4} .
- (7) Mode Register Write command brings all Row Buffers to the MR Writing state. All Row Buffers return to the Idle state after t_{MRW} .
- (8) Mode Register Read command brings the Row Buffer to the Idle MR Reading state. The Row Buffer goes automatically back to the Idle state after t_{MRR} .
- (9) Preactive command brings the Row Buffer to the Preactivating state. The Row Buffer goes automatically back to the Idle state after t_{RP} .

3.3.2 Idle state (cont'd)

(10) Activate command brings the Row Buffer from the Idle state to the Row Activating state, which is not explicitly shown in the state diagram. The Row Buffer goes automatically from the Row Activating state to the Active state after t_{RCD} .

(11) Enter Power Down command brings the Row Buffer into the Idle Power Down state. For the complete description of power down entry see [5.14](#).

(12) Exit Power Down command brings the Row Buffer from the Idle Power Down state back to the Idle state after t_{XP} . For the complete description of power down exit see [5.14](#).

3.3.3 Active state

From the Active state, the following commands are allowed: Reset, Mode Register Write, Mode Register Read, Preactive, Activate, Read, Write and Enter Power Down.

(13) Reset command brings all Row Buffers into the Resetting state after t_{INIT4} .

(14) Mode Register Write command brings all Row Buffers to the MR Writing state. All Row Buffers return to the Idle state after t_{MRW} .

(15) Mode Register Read command brings the Row Buffer to the Active MR Reading state. The Row Buffer goes automatically back to the Active state after t_{MRR} .

(16) Preactive command brings the Row Buffer to the Preactivating state. The Row Buffer goes automatically to the Idle state after t_{RP} .

(17) Activate command brings the Row Buffer from the Active state to the Row Activating state, which is not explicitly shown in the state diagram. The Row Buffer goes automatically back to the Active state after t_{RCD} .

(18) Read command moves the Row Buffer to the Reading state. The Row Buffer goes automatically back to the Row Active state after BL/2 clock cycles, or after a Burst Terminate command. See [5.4](#) for timing restrictions to apply between the Read command and a following Read, Write, Mode Register Write, Mode Register Read, Preactive, Activate or Enter Power Down commands that might occur. If a new Read command is issued within BL/2 clock cycles, the Row Buffer remains in the Reading state.

(19) Write command moves the Row Buffer to the Writing state. The Row Buffer goes automatically back to the Row Active state after BL/2 clock cycles, or after a Burst Terminate command. See [5.5](#) for timing restrictions to apply between the Write command and the following Write, Read, Mode Register Write, Mode Register Read, Preactive, Activate or Enter Power Down commands that might occur. If a new Write command is issued within BL/2 clock cycles, the Row buffer remains in the Writing state.

(20) Enter Power Down command brings the Row Buffer into the Active Power Down state. For the complete description of power down entry see [5.14](#).

(21) Exit Power Down command brings the Row Buffer from the Active Power Down state back to the Row Active state after t_{XP} . For the complete description of power down exit see [5.14](#).

3.3.3 Active state (cont'd)

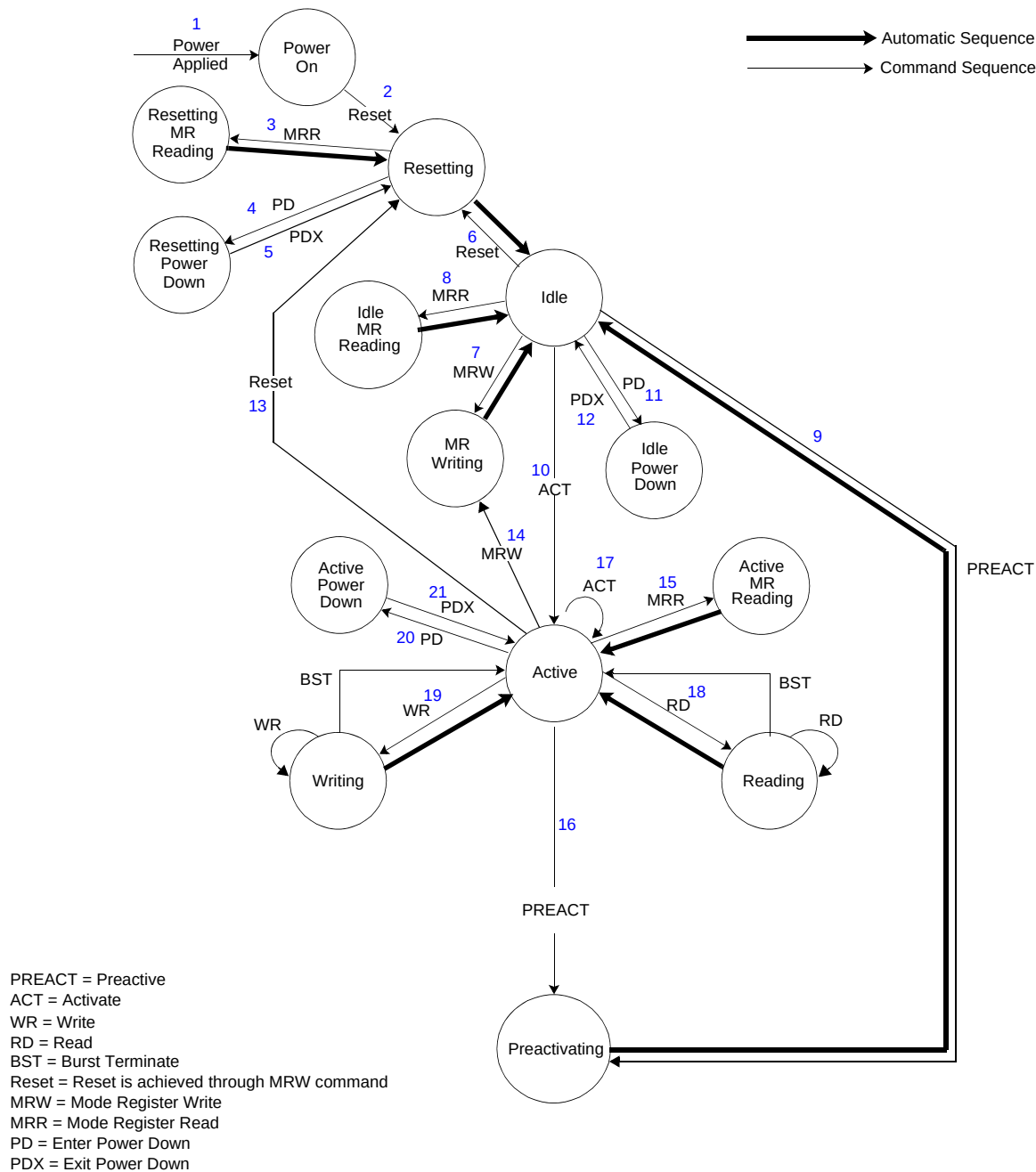


Figure 5 — LPDDR2-N: Simplified Bus Interface State Diagram

NOTE 1 For LPDDR2-NVM in the Active state, one or more Row Buffers have been activated.

NOTE 2 Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Row Buffer are not captured in full detail.

NOTE 3 Resetting duration is variable. Poll DAI status bit to detect state transition to Idle.

NOTE 4 Reset command sets all Row Address Buffers to 0x0000.

3.4 Power-up, Initialization, and Power-Off

LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

3.4.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

1. Power Ramp

While applying power (after T_a), CKE shall be held at a logic low level ($= < 0.2 \times VDDCA$), all other inputs shall be between VIL_{min} and VIH_{max} . The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (T_b) CKE must be held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between $VSSQ$ and $VDDQ$ during voltage ramp to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between $VSSCA$ and $VDDCA$ during voltage ramp to avoid latch-up.

The following conditions apply:

T_a is the point where *any* power supply first reaches 300 mV.

After T_a is reached, $VDD1$ must be greater than $VDD2 - 200$ mV.

After T_a is reached, $VDD1$ and $VDD2$ must be greater than $VDDCA - 200$ mV.

After T_a is reached, $VDD1$ and $VDD2$ must be greater than $VDDQ - 200$ mV.

After T_a is reached, $VREF$ must always be less than all other supply voltages.

The voltage difference between any of VSS , $VSSQ$, and $VSSCA$ pins may not exceed 100 mV.

The above conditions apply between T_a and power-off (controlled or uncontrolled).

T_b is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

For supply and reference voltage operating conditions, see Table 69, Table 70, and Table 71.

Power ramp duration t_{INIT0} ($T_b - T_a$) must be no greater than 20 ms.

NOTE $VDD2$ is not present in some systems. Rules related to $VDD2$ in those cases do not apply.

2. CKE and clock:

Beginning at T_b , CKE must remain low for at least $t_{INIT1} = 100$ ns, after which it may be asserted high. Clock must be stable at least $t_{INIT2} = 5 \times t_{CK}$ prior to the first low to high transition of CKE (T_c). CKE, CS_n and CA inputs must observe setup and hold time (t_{IS} , t_{IH}) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCk}) may have relaxed timings (e.g. t_{DQSCkb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least $t_{INIT3} = 200$ us. (T_d).

3. Reset command:

After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (T_d). The memory controller may optionally issue a Precharge-All command (for LPDDR2-SX) or Preactive (for LPDDR2-N) prior to the MRW Reset command. For LPDDR2-N devices, the subsequent MRW Reset command will set each Row Address Buffers (RAB) to 0x0000 overwriting the value stored by the previous preactive command. Wait for at least t_{INIT4} keeping CKE asserted and issuing NOP commands.

3.4.1 Power Ramp and Device Initialization (cont'd)

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After t_{INIT4} is satisfied (**Te**) only MRR commands and power-down entry/exit commands are allowed.

Therefore, after **Te**, CKE may go low in accordance to Power-Down entry and exit specification (see 5.14).

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of t_{INIT5} before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR0, “DAI”) is set to zero “DAI complete” by the memory device, the device is in idle state (**Tf**). The state of the DAI status bit can be determined by an MRR command to MR0.

All SDRAM devices will set the DAI-bit no later than t_{INIT5} (10 us) after the Reset command. The memory controller shall wait a minimum of t_{INIT5} or until the DAI-bit is set before proceeding.

For NVM devices, repetitive polling of the DAI-Bit is required to determine when this bit has internally been set to zero “DAI complete” by the memory device. A Value for t_{INIT5} value is not defined for NVMs in this document because it is device dependent. The only way to determine when Device Auto-Initialization is complete is to poll DAI. To obtain the shortest boot up time and ensure compatibility with any future NVM device it is recommended to not rely on any predetermined t_{INIT5} value.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

5. ZQ Calibration:

After t_{INIT5} (**Tf**), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). For LPDDR2 devices which do not support the ZQ Calibration command, this command shall be ignored. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after t_{ZQINIT} .

6. Normal Operation:

After t_{ZQINIT} (**Tg**), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

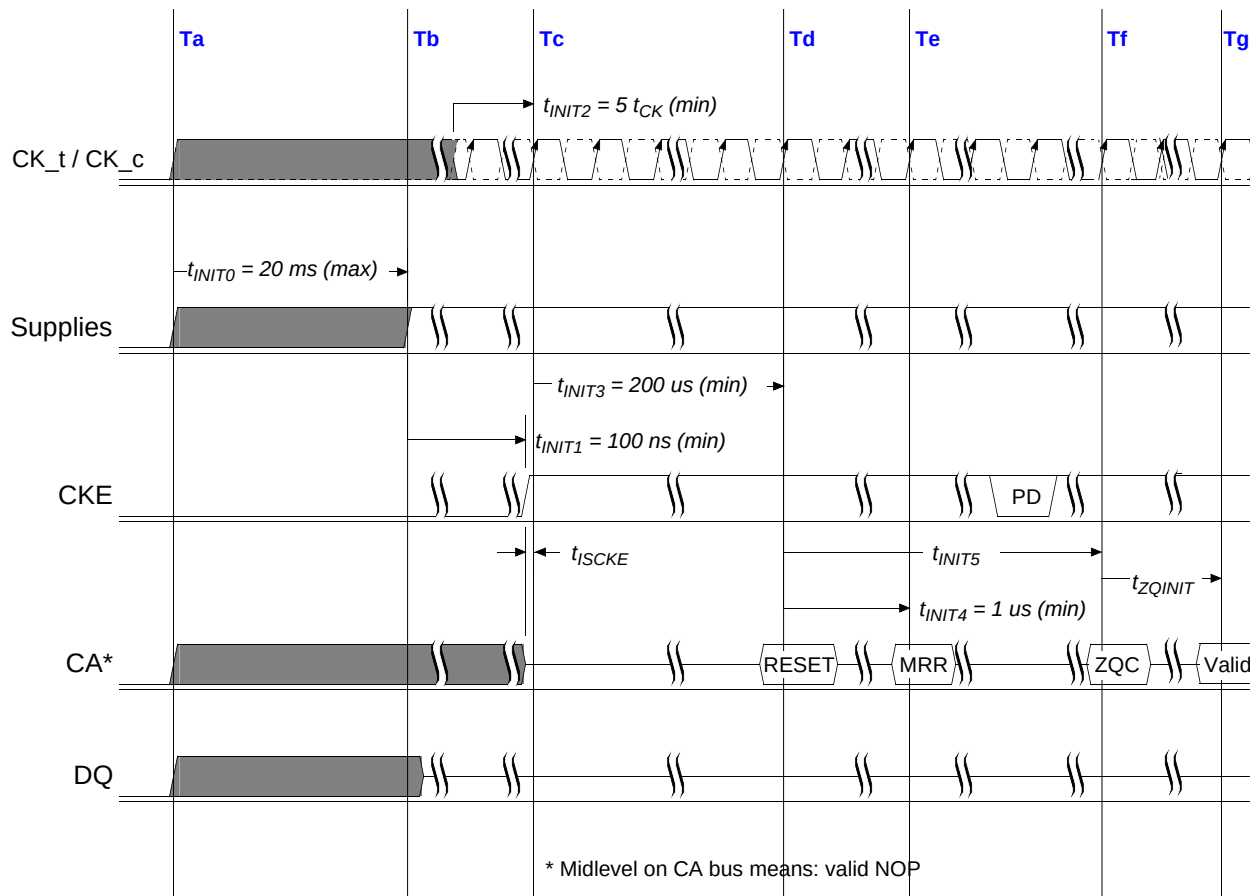
To support simple boot from the NVM, some Mode Registers are reset to default values during Device Auto-Initialization. See the Mode Register section of this specification for default values.

The LPDDR2 device will now be in IDLE state and ready for any valid command.

After **Tg**, the clock frequency may be changed according to the clock frequency change procedure described in 5.16.

3.4.1 Power Ramp and Device Initialization (cont'd)**Table 15 — Timing Parameters for initialization**

Symbol	Value		Unit	Comment
	min	max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	100		ns	Minimum CKE low time after completion of power ramp
t_{INIT2}	5		tCK	Minimum stable clock before first CKE high
t_{INIT3}	200		μs	Minimum Idle time after first CKE assertion
t_{INIT4}	1		μs	Minimum Idle time after Reset command
t_{INIT5}		S: 10	μs	Maximum duration of Device Auto-Initialization
		N: vendor	μs	
t_{ZQINIT}	1		μs	ZQ Initial Calibration for LPDDR2-S4 and LPDDR2-N devices
t_{CKb}	18	100	ns	Clock cycle time during boot

**Figure 6 — Power Ramp and Initialization Sequence****3.4.2 Initialization after Reset (without Power ramp)**

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

3.4.3 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

While removing power, CKE shall be held at a logic low level ($\leq 0.2 \times VDDCA$), all other inputs shall be between VIL_{min} and VIH_{max} . The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

For LPDDR2-N devices, all embedded operations must be finished or aborted and the device must be in the ready state (Status Register, bit 7 = "1") prior to Power-off.

DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during power off sequence to avoid latch-up.

T_x is the point where any power supply decreases under its minimum value specified in the DC operating condition table, see 7.1.

T_z is the point where *all* power supplies are below 300 mV. After T_z, the device is powered off.

The time between T_x and T_z (t_{POFF}) shall be less than 2s.

The following conditions apply:

Between T_x and T_z, VDD1 must be greater than VDD2 - 200 mV.

Between T_x and T_z, VDD1 and VDD2 must be greater than VDDCA - 200 mV.

Between T_x and T_z, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

Between T_x and T_z, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

For supply and reference voltage operating conditions, see Table 69, Table 70, and Table 71.

NOTE VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

Table 16 — Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t _{POFF}	-	2	s	Maximum Power-Off ramp time

3.4.4 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition. Unless specified otherwise, these steps are mandatory and apply to S2, S4 and N devices.

T_x is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

T_z is the point where all power supply first reaches 300 mV. After T_z, the device is powered off.

The time between T_x and T_z (t_{POFF}) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between T_x and T_z.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

3.5 Mode Register Definition

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM

Table 17 shows the 16 common mode registers for LPDDR2 SDRAM and NVM. **Table 18** shows only LPDDR2 SDRAM mode registers and **Table 19** shows only LPDDR2 NVM mode registers. Additionally **Table 20** shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 17 — Mode Register Assignment in LPDDR2 SDRAM/NVM(Common part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link	
0	00 _H	Device Info.	R	(RFU)			RZQI (optional)		DNVI	DI	DAI	go to MR0	
1	01 _H	Device Feature 1	W	nWR (for AP)			WC	BT	BL			go to MR1	
2	02 _H	Device Feature 2	W	(RFU)				RL & WL				go to MR2	
3	03 _H	I/O Config-1	W	(RFU)				DS				go to MR3	
4	04 _H	SDRAM Refr. R.	R	TUF	(RFU)				Refresh Rate				go to MR4
		NVM Temp. Alert	R	TUF	(RFU)				NVM Temp. Alert				
5	05 _H	Basic Config-1	R	LPDDR2 Manufacturer ID								go to MR5	
6	06 _H	Basic Config-2	R	Revision ID1								go to MR6	
7	07 _H	Basic Config-3	R	Revision ID2								go to MR7	
8	08 _H	Basic Config-4	R	I/O width		Density				Type			go to MR8
9	09 _H	Test Mode	W	Vendor-Specific Test Mode								go to MR9	
10	0A _H	IO Calibration	W	Calibration Code								go to MR10	
11:15	0B _H ~0F _H	(reserved)		(RFU)								go to MR11	

Table 18 — Mode Register Assignment in LPDDR2 SDRAM/NVM (SDRAM part)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
16	10 _H	PASR_Bank (S4)	W	Bank Mask								go to MR16
		PASR_Bank (S2)		(RFU)						PASR		
17	11 _H	PASR_Seg	W	Segment Mask (S4 SDRAM only)								go to MR17
18-19	12 _H -13 _H	(Reserved)		(RFU)								go to MR18

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 19 — Mode Register Assignment in LPDDR2 SDRAM/NVM (NVM part)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
20	14 _H	NVM Geometry	R	(RFU)		tRCD De-Rating		RB Number	RDB size			go to MR20
21	15 _H	NVM tRCD	R	tRCD Value (2nd order)				tRCD Value (1st order)				go to MR21
22-23	16 _H -17 _H	(Reserved)		(RFU)								go to MR22
24	18 _H	Overlay Window Enable	R/W	(RFU)						OWD	OWE	go to MR24
25	19 _H	OW Base-Addr 1	R/W	OW base-addr 31 (a19 ~ a13)							0	go to MR25
26	1A _H	OW Base-Addr 2	R/W	OW base-addr 2 (a27 ~ a20)								
27	1B _H	OW Base-Addr 3	R/W	(RFU)				OW base-addr 3 (a31 ~ a28)				
28	1C _H	(Reserved)		(RFU)								go to MR28
29	1D _H	DNV Long Delay	R	tDNV Value (2nd order)				tDNV Value (1st order)				go to MR29
30-31	1E _H -1F _H	(Reserved)		(RFU)								go to MR30

Table 20 — Mode Register Assignment in LPDDR2 SDRAM/NVM
(DQ Calibration and Reset Command)

MR#	MA <7:0>	Function	access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
32	20 _H	DQ Calibration Pattern A	R	See “DQ Calibration” on page 131								go to MR32
33:39	21 _H -27 _H	(Do Not Use)										go to MR33
40	28 _H	DQ Calibration Pattern B	R	See “DQ Calibration” on page 131								go to MR40
41:47	29 _H -2F _H	(Do Not Use)										go to MR41
48:62	30 _H -3E _H	(Reserved)		(RFU)								go to MR48
63	3F _H	Reset	W	X								go to MR63
64:126	40 _H -7E _H	(Reserved)		(RFU)								go to MR64
127	7F _H	(Do Not Use)										go to MR127
128:190	80 _H -BE _H	(Reserved for Vendor Use)		(RFU)								go to MR128
191	BF _H	(Do Not Use)										go to MR191
192:254	C0 _H -FE _H	(Reserved for Vendor Use)		(RFU)								go to MR192
255	FF _H	(Do Not Use)										go to MR255

The following notes apply to Tables 17-20:

NOTE 1 RFU bits shall be set to ‘0’ during Mode Register writes.

NOTE 2 RFU bits shall be read as ‘0’ during Mode Register reads.

NOTE 3 All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.

NOTE 4 All Mode Registers that are specified as RFU shall not be written.

NOTE 5 See Vendor Device Datasheets for details on Vendor Specific Mode Registers.

NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR0 Device Information (MA<7:0> = 00_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI (optional)		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0_B : DAI complete 1_B : DAI still in progress	
DI (Device Information)	Read-only	OP1	0_B : S2 or S4 SDRAM 1_B : NVM	
DNVI (Data Not Valid Information)	Read-only	OP2	0_B : DNV not supported 1_B : DNV supported	1,2
RZQI (Built in Self Test for RZQ Information)	Read-only	OP4:OP3	00_B : RZQ self test not supported 01_B : ZQ-pin may connect to VDDCA or float 10_B : ZQ-pin may short to GND 11_B : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)	3

NOTE 1 LPDDR2 SDRAM will not implement DNV functionality.

NOTE 2 If DNV functionality is not implemented, the device shall not drive the DM/DNV signals.

NOTE 3 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

NOTE 4 If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 5 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per NOTE 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

NOTE 6 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240-ohm +/-1%).

MR1_Device Feature 1 (MA<7:0> = 01_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)				WC	BT	BL	
BL	Write-only	OP<2:0>	010_B : BL4 (default) 011_B : BL8 100_B : BL16 All others : reserved				
BT	Write-only	OP<3>	0_B : Sequential (default) 1_B : Interleaved (allowed for SDRAM only)				1
WC	Write-only	OP<4>	0_B : Wrap (default) 1_B : No wrap (allowed for SDRAM BL4 only)				
nWR	Write-only	OP<7:5>	001_B : nWR=3 (default) 010_B : nWR=4 011_B : nWR=5 100_B : nWR=6 101_B : nWR=7 110_B : nWR=8 All others : reserved				2

NOTE 1 BL 16, interleaved is not an official combination to be supported.

NOTE 2 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

NOTE 3 BL16 is not supported by LPDDR2-NVM with Row Data Buffer size equal to 32-Byte and Data Bus Width equal to 32-bit.

NOTE 4 OP7:OP5 are reserved for LPDDR2-NVM.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 21 — Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence																
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
X	X	0 _B	0 _B	wrap	any	4	0	1	2	3													
X	X	1 _B	0 _B				2	3	0	1													
X	X	X	0 _B	nw	any		y	y+1	y+2	y+3													
X	0 _B	0 _B	0 _B	wrap	seq	8	0	1	2	3	4	5	6	7									
X	0 _B	1 _B	0 _B				2	3	4	5	6	7	0	1									
X	1 _B	0 _B	0 _B				4	5	6	7	0	1	2	3									
X	1 _B	1 _B	0 _B				6	7	0	1	2	3	4	5									
X	0 _B	0 _B	0 _B		int		0	1	2	3	4	5	6	7									
X	0 _B	1 _B	0 _B				2	3	0	1	6	7	4	5									
X	1 _B	0 _B	0 _B				4	5	6	7	0	1	2	3									
X	1 _B	1 _B	0 _B				6	7	4	5	2	3	0	1									
X	X	X	0 _B	nw	any	illegal (not allowed)																	
0 _B	0 _B	0 _B	0 _B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0 _B	0 _B	1 _B	0 _B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	
0 _B	1 _B	0 _B	0 _B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	
0 _B	1 _B	1 _B	0 _B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	
1 _B	0 _B	0 _B	0 _B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	
1 _B	0 _B	1 _B	0 _B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	
1 _B	1 _B	0 _B	0 _B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	
1 _B	1 _B	1 _B	0 _B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	
X	X	X	0 _B		int	illegal (not allowed)																	
X	X	X	0 _B	nw	any	illegal (not allowed)																	

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in [Table 22](#) for the respective density and bus width combinations.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

Table 22 — LPDDR2-SX Non Wrap Restrictions

	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/6Gb/8Gb
Not across full page boundary				
x8	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001	FFE, FFF, 000, 001
x16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
x32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
Not across sub page boundary				
x8	07E, 07F, 080, 081	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401	7FE, 7FF, 800, 801
	17E, 17F, 180, 181	2FE, 2FF, 300, 301	5FE, 5FF, 600, 601	BFE, BFF, C00, C01
x16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
x32	None	None	None	None

NOTE 1 Non-wrap BL=4 data-orders shown above are prohibited.

MR2 Device Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	0001_B : RL = 3 / WL = 1 (default) 0010_B : RL = 4 / WL = 2 0011_B : RL = 5 / WL = 2 0100_B : RL = 6 / WL = 3 0101_B : RL = 7 / WL = 4 0110_B : RL = 8 / WL = 4 All others : reserved
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MR3 I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	0000_B : reserved 0001_B : 34.3-ohm typical 0010_B : 40-ohm typical (default) 0011_B : 48-ohm typical 0100_B : 60-ohm typical 0101_B : reserved for 68.6-ohm typical 0110_B : 80-ohm typical 0111_B : 120-ohm typical (optional) All others : reserved
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3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR4 Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF			(RFU)				SDRAM Refresh Rate
TUF			(RFU)				NVM Temperature Alert

SDRAM Refresh Rate	Read-only	OP<2:0>	000_B : SDRAM Low temperature operating limit exceeded 001_B : $4 \times t_{REFI}$, $4 \times t_{REFIpb}$, $4 \times t_{REFW}$ 010_B : $2 \times t_{REFI}$, $2 \times t_{REFIpb}$, $2 \times t_{REFW}$ 011_B : $1 \times t_{REFI}$, $1 \times t_{REFIpb}$, $1 \times t_{REFW}$ ($\leq 85^{\circ}\text{C}$) 100_B : Reserved 101_B : $0.25 \times t_{REFI}$, $0.25 \times t_{REFIpb}$, $0.25 \times t_{REFW}$, do not de-rate SDRAM AC timing 110_B : $0.25 \times t_{REFI}$, $0.25 \times t_{REFIpb}$, $0.25 \times t_{REFW}$, de-rate SDRAM AC timing 111_B : SDRAM High temperature operating limit exceeded
NVM Temperature Alert	Read-only	OP<2:0>	000_B : NVM Low temperature operating limit exceeded 001_B : Reserved 010_B : Reserved 011_B : Temperature Alert not active, do not de-rate NVM AC timing ($\leq 85^{\circ}\text{C}$) 100_B : Temperature Alert not active, de-rate NVM AC timing 101_B : Temperature Alert active, do not de-rate NVM AC timing 110_B : Temperature Alert active, de-rate NVM AC timings 111_B : NVM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	0_B : OP<2:0> value has not changed since last read of MR4. 1_B : OP<2:0> value has changed since last read of MR4.

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.

NOTE 2 OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85°C.

NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.

NOTE 5 LPDDR2 might not operate properly when OP[2:0] = 000_B or 111_B.

NOTE 6 For specified operating temperature range and maximum operating temperature refer to [Table 72](#).

NOTE 7 LPDDR2-SX devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in [Table 103](#). Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 8 LPDDR2-NVM devices shall be de-rated by adding the value found at location OP5:OP4 in MR20 to the following core timing parameters: tRCD, tRC, tRAS, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in [Table 103](#). Prevailing clock frequency spec and related setup and hold timings remain unchanged.

NOTE 9 See [5.12.1](#) for information on the recommended frequency of reading MR4.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR5 Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							
LPDDR2 Manufacturer ID	Read-only	OP<7:0>	0000 0000B : Reserved				
			0000 0001B : Samsung				
			0000 0010B : Qimonda				
			0000 0011B : Elpida				
			0000 0100B : Etron				
			0000 0101B : Nanya				
			0000 0110B : Hynix				
			0000 0111B : Mosel				
			0000 1000B : Winbond				
			0000 1001B : ESMT				
			0000 1010B : Reserved				
			0000 1011B : Spansion				
			0000 1100B : SST				
			0000 1101B : ZMOS				
			0000 1110B : Intel				
			1111 1110B : Numonyx				
			1111 1111B : Micron				
			All Others : Reserved				

MR6 Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							
Revision ID1	Read-only	OP<7:0>	00000000 _B : A-version				

NOTE 1 MR6 is Vendor Specific.

MR7 Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							
Revision ID2	Read-only	OP<7:0>	00000000 _B : A-version				

NOTE 1 MR7 is Vendor Specific.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR8 Basic Configuration 4 (MA<7:0> = 08B_H):

OP7		OP6		OP5		OP4		OP3		OP2		OP1		OP0	
I/O width				Density								Type			
Type	Read-only	OP<1:0>		00_B : S4 SDRAM 01_B : S2 SDRAM 10_B : N NVM 11_B : Reserved											
Density	Read-only	OP<5:2>		0000_B : 64Mb 0001_B : 128Mb 0010_B : 256Mb 0011_B : 512Mb 0100_B : 1Gb 0101_B : 2Gb 0110_B : 4Gb 1110_B : 6Gb 0111_B : 8Gb 1000_B : 16Gb 1001_B : 32Gb all others : reserved											
I/O width	Read-only	OP<7:6>		00_B : x32 01_B : x16 10_B : x8 11_B : not used											

MR9 Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10 Calibration (MA<7:0> = 0A_H):

								OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code															
Calibration Code	Write-only	OP<7:0>	0xFF: Calibration command after initialization												
			0xAB: Long calibration												
			0x56: Short calibration												
			0xC3: ZQ Reset												
			others: Reserved												

NOTE 1 Host processor shall not write MR10 with “Reserved” values

NOTE 2 LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.

NOTE 3 See AC timing table for the calibration latency.

NOTE 4 If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see 5.13.4) or default calibration (through the ZQreset command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

NOTE 5 LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.

NOTE 6 Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate R_{ZQ} pin connection.

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)**MR11:15 (Reserved) (MA<7:0> = 0B_H-0F_H):****MR16_PASR_Bank Mask (MA<7:0> = 010_H): S2 and S4 SDRAM only**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S2 SDRAM	(RFU)						PASR	
S4 SDRAM	Bank Mask (4-bank or 8-bank)							

S2 SDRAM:

PASR Map	Write-only	OP<1:0>	00_B : Full array (default) 01_B : 1/2 array - BA1=0 for 4-banks, BA2=0 for 8-banks 10_B : 1/4 array - BA1=BA0=0 for 4-banks, BA2=BA1=0 for 8-banks 11_B : 1/8 array - Not used for 4-banks, BA2=BA1=BA0=0 for 8-banks	
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S4 SDRAM:

Bank <7:0> Mask	Write-only	OP<7:0>	0_B : refresh enable to the bank (=unmasked, default) 1_B : refresh blocked (=masked)	1
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1. For 4-bank S4 SDRAM, only OP<3:0> are used.

OP	Bank Mask	4-Bank S4 SDRAM	8-Bank S4 SDRAM
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

MR17_PASR_Segment Mask (MA<7:0> = 011_H): 1Gb ~ 8Gb S4 SDRAM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							
Segment <7:0> Mask	Write-only	OP<7:0>	0_B : refresh enable to the segment (=unmasked, default) 1_B : refresh blocked (=masked)				

			1Gb	2Gb,4Gb,6Gb	8Gb
Segment	OP	Segment Mask	R12:10	R13:11	R14:12
0	0	XXXXXXXX1	000_B		
1	1	XXXXXX1X	001_B		
2	2	XXXXX1XX	010_B		
3	3	XXXX1XXX	011_B		
4	4	XXX1XXXX	100_B		
5	5	XX1XXXXX	101_B		
6	6	X1XXXXXX	110_B		
7	7	1XXXXXXX	111_B		

NOTE This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment

MR18-19_Reserved (MA<7:0> = 012_H - 013_H):

MR20_NVM Geometry (MA<7:0> = 014_H): NVM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)		tRCD De-Rating		RB Number	RDB size		

RDB Size	Read-only	OP<2:0>	000_B : 32B 001_B : 64B 010_B : 128B 011_B : 256B 100_B : 512B 101_B : 1024B 110_B : 2048B 111_B : 4096B
RB Number	Read-only	OP<3>	0_B : 4 Row Buffers 1_B : 8 Row Buffers
tRCD De-rating (t _{NVMDERATING})	Read-only	OP<5:4>	00_B : 0 ns 01_B : 1.875 ns 10_B : 3.75 ns 11_B : 7.5 ns

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)**MR21 NVM tRCD (MA<7:0> = 15_H): NVM only**

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
t _{RCD} Value (2nd order)				t _{RCD} Value (1st order)			

t _{RCD} Value (1st order = value ns)	Read-only	OP<3:0>	0000 _B : 0ns	0001 _B : 1ns	
			0010 _B : 2ns	0011 _B : 3ns	
			0100 _B : 4ns	0101 _B : 5ns	
			0110 _B : 6ns	0111 _B : 7ns	
			1000 _B : 8ns	1001 _B : 9ns	
			1010 _B : 10ns	1011 _B : 11ns	
			1100 _B : 12ns	1101 _B : 13ns	
			1110 _B : 14ns	1111 _B : 15ns	
t _{RCD} Value (2nd order = valuex16 ns)	Read-only	OP<7:4>	0000 _B : 0ns	0001 _B : 16ns	
			0010 _B : 32ns	0011 _B : 48ns	
			0100 _B : 64ns	0101 _B : 80ns	
			0110 _B : 96ns	0111 _B : 112ns	
			1000 _B : 128ns	1001 _B : 144ns	
			1010 _B : 160ns	1011 _B : 176ns	
			1100 _B : 192ns	1101 _B : 208ns	
			1110 _B : 224ns	1111 _B : 240ns	

NOTE 1 t_{RCD} value is obtained adding 1st order value to the 2nd order value

MR22:23 (Reserved) (MA<7:0> = 16_H:17_H):