JEDEC STANDARD

Low Power Double Data Rate 3 (LPDDR3)

JESD209-3C

(Revision of JESD209-3B, August 2013)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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LOW POWER DOUBLE DATA RATE 3 SDRAM (LPDDR3)

From JEDEC Board Ballot JCB-15-12, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memory.)

1 Scope

This document defines the LPDDR3 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant 1 Gb through 32 Gb for x16 and x32 SDRAM devices. This standard was created using aspects of the following documents: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR2 (JESD209-2). Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR3 standard.

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2 Package ballout & Pin Definition

2.1 POP FBGA Ball-outs

2.1.1 216-ball 12 mm x 12 mm, 0.4 mm Pitch Dual-Channel POP FBGA (top view) Using Variation VCCCDB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSS	VDD2	DQ30_a	DQ29_a	VSS	DQ26_a	DQ25_a	VSS	DQS3_c_a	VSS	DQ14_a	DQ13_a	VSS	VDD1	VDD2	DQ11_a	DQ10_a	DQ9_a	DQS1_t_a	DM_1_a	VDDQ	DQS0_t_a	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS	DNU
B	VSS	NC	DQ31_a	VDDQ	DQ28_a	DQ27_a	VDDQ	DQ24_a	VDDQ	DQS3_t_a	DM3_a	DQ15_a	VDDQ	VSS	Vref(DQ)_a	VDD2	DQ12_a	VDDQ	DQ8_a	DQS1_c_a	VSS	DM_0_a	DQS0_c_a	VSS	VDDQ	DQ5_a	DQ2_a	NC	VSS
C	VDD1	DQ16_b																										VDD1	VDD2
D	DQ17_b	VDDQ																										DQ1_a	VDDQ
E	DQ18_b	DQ19_b																										VSS	DQ0_a
F	VSS	DQ20_b																										DM2_a	VDDQ
G	DQ21_b	VDDQ																										DQS2_t_a	DQS2_c_a
H	DQ22_b	DQ23_b																										VSS	DQ23_a
J	VSS	VDDQ																										VDDQ	DQ22_a
K	DQS2_c_b	DQS2_t_b																										DQ20_a	DQ21_a
L	DM2_b	DQ0_b																										DQ19_a	VSS
M	DQ1_b	VSS																										VDDQ	DQ18_a
N	DQ2_b	VDD1																										DQ16_a	DQ17_a
P	VSS	VSS																										VDD2	VDD1
R	VDD1	Vref(DQ)_b																										VSS	CA0_b
T	VDD2	VDD2																										VDDCA	CA1_b
U	VDDQ	DQ3_b																										Vref(CA)_b	CA2_b
V	DQ4_b	VSS																										VSS	CA3_b
W	DQ6_b	DQ5_b																										CA4_b	CS1_n_b
Y	VDDQ	DQ7_b																										CS0_n_b	CKE1_b
AA	DQS0_t_b	DQS0_c_b																										VSS	CKE0_b
AB	DM0_b	VSS																										CK_t_b	CK_c_b
AC	VDDQ	DM1_b																										VDDCA	CA5_b
AD	DQS1_c_b	DQS1_t_b																										CA7_b	CA6_b
AE	DQ8_b	VSS																										CA8_b	VDDCA
AF	DQ9_b	VDDQ																										VSS	CA9_b
AG	DQ10_b	DQ11_b																										VDD2	ZQ_b
AH	VSS	VDD1	VDD2	DQ13_b	VSS	DQ15_b	DM3_b	DQS3_t_b	VDDQ	DQ26_b	DQ27_b	VDDQ	DQ30_b	VSS	VDD2	Vref(CA)_a	CA9_a	VSS	CA7_a	CA6_a	CK_c_a	VDDCA	CKE0_a	CS0_n_a	CA3_a	CA2_a	CA1_a	VDD1	VSS
AJ	DNU	VSS	DQ12_b	VDDQ	DQ14_b	VDDQ	VSS	DQS3_c_b	DQ24_b	DQ25_b	VSS	DQ28_b	DQ29_b	DQ31_b	VDD1	VSS	ZQ_a	CA8_a	VDDCA	CA5_a	CK_t_a	VSS	CKE1_a	CS1_n_a	CA4_a	VDDCA	CA0_a	VSS	DNU

- Channel b
- Channel a
- Power
- Ground
- Do Not Use
- ZQ
- Clock
- NC

NOTE 1 12x12 mm, 0.4mm pitch, 29 rows

NOTE 2 216 Ball Count

NOTE 3 Top View, A1 in Top Left Corner

NOTE 4 See JESD21-C, 3.12.2

NOTE 5 ODT pin is NOT supported. ODT die pads are connected to V_{SS} inside the package.

NOTE 6 ZQ_a (ZQ_b) is connected to rank 0 DRAM and rank 1 DRAM (if second rank is present) of channel a (channel b).

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2.1.2 216-ball 12 mm x 12 mm, 0.4 mm Pitch Single Channel A POP FBGA (top view) Using Variation VCCCDB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSS	VDD2	DQ30	DQ29	VSS	DQ26	DQ25	VSS	DQS3_c	VSS	DQ14	DQ13	VSS	VDD1	VDD2	DQ11	DQ10	DQ9	DQS1_t	DM_1	VDDQ	DQS0_t	DQ7	DQ6	DQ4	DQ3	VSS	DNU
B	VSS	NC	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	VDDQ	DQS3_t	DM3	DQ15	VDDQ	VSS	Vref(DQ)	VDD2	DQ12	VDDQ	DQ8	DQS1_c	VSS	DM_0	DQS0_c	VSS	VDDQ	DQ5	DQ2	NC	VSS
C	VDD1	NC																										VDD1	VDD2
D	NC	VDDQ																										DQ1	VDDQ
E	NC	NC																										VSS	DQ0
F	VSS	NC																										DM2	VDDQ
G	NC	VDDQ																										DQS2_t	DQS2_c
H	NC	NC																										VSS	DQ23
J	VSS	VDDQ																										VDDQ	DQ22
K	NC	NC																										DQ20	DQ21
L	NC	NC																										DQ19	VSS
M	NC	VSS																										VDDQ	DQ18
N	NC	VDD1																										DQ16	DQ17
P	VSS	VSS																										VDD2	VDD1
R	VDD1	NC																										VSS	NC
T	VDD2	VDD2																										VDDCA	NC
U	VDDQ	NC																										NC	NC
V	NC	VSS																										VSS	NC
W	NC	NC																										NC	NC
Y	VDDQ	NC																										NC	NC
AA	NC	NC																										VSS	NC
AB	NC	VSS																										NC	NC
AC	VDDQ	NC																										VDDCA	NC
AD	NC	NC																										NC	NC
AE	NC	VSS																										NC	VDDCA
AF	NC	VDDQ																										VSS	NC
AG	NC	NC																										VDD2	ZQ1
AH	VSS	VDD1	VDD2	NC	VSS	NC	NC	NC	VDDQ	NC	NC	VDDQ	NC	VSS	VDD2	Vref(CA)	CA9	VSS	CA7	CA6	CK_c	VDDCA	CKE0	CS0_n	CA3	CA2	CA1	VDD1	VSS
AJ	DNU	VSS	NC	VDDQ	NC	VDDQ	VSS	NC	NC	NC	VSS	NC	NC	NC	VDD1	VSS	ZQ0	CA8	VDDCA	CA5	CK_t	VSS	CKE1	CS1_n	CA4	VDDCA	CA0	VSS	DNU

Channel
Power
Ground
Do Not Use
ZQ
Clock
NC

NOTE 1 12x12 mm, 0.4 mm pitch, 29 rows
NOTE 2 216 Ball Count
NOTE 3 Top View, A1 in Top Left Corner
NOTE 4 See JESD21-C, 3.12.2 (MO-273, Issue: C, Item: 11-841, Variation: VCCCDB)
NOTE 5 ODT pin is NOT supported. ODT die pads are connected to V_{SS} inside the package
NOTE 6 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is NC
NOTE 7 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if present).
NOTE 8 Consult manufacturer for guidance concerning Single Channel A and Single Channel B ballout support availability.

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2.1.3 216-ball 12 mm x 12 mm, 0.4 mm Pitch Single Channel B POP FBGA (top view) Using Variation VCCCDB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSS	VDD2	NC	NC	VSS	NC	NC	VSS	NC	VSS	NC	NC	VSS	VDD1	VDD2	NC	NC	NC	NC	NC	VDDQ	NC	NC	NC	NC	NC	VSS	DNU
B	VSS	NC	NC	VDDQ	NC	NC	VDDQ	NC	VDDQ	NC	NC	NC	VDDQ	VSS	NC	VDD2	NC	VDDQ	NC	NC	VSS	NC	NC	VSS	VDDQ	NC	NC	NC	VSS
C	VDD1	DQ16																										VDD1	VDD2
D	DQ17	VDDQ																										NC	VDDQ
E	DQ18	DQ19																										VSS	NC
F	VSS	DQ20																										NC	VDDQ
G	DQ21	VDDQ																										NC	NC
H	DQ22	DQ23																										VSS	NC
J	VSS	VDDQ																										VDDQ	NC
K	DQS2_c	DQS2_t																										NC	NC
L	DM2	DQ0																										NC	VSS
M	DQ1	VSS																										VDDQ	NC
N	DQ2	VDD1																										NC	NC
P	VSS	VSS																										VDD2	VDD1
R	VDD1	Vref(DQ)																										VSS	CA0
T	VDD2	VDD2																										VDDCA	CA1
U	VDDQ	DQ3																										Vref(CA)	CA2
V	DQ4	VSS																										VSS	CA3
W	DQ6	DQ5																										CA4	CS1_n
Y	VDDQ	DQ7																										CS0_n	CKE1
AA	DQS0_t	DQS0_c																										VSS	CKE0
AB	DM0	VSS																										CK_t	CK_c
AC	VDDQ	DM1																										VDDCA	CA5
AD	DQS1_c	DQS1_t																										CA7	CA6
AE	DQ8	VSS																										CA8	VDDCA
AF	DQ9	VDDQ																										VSS	CA9
AG	DQ10	DQ11																										VDD2	ZQ0
AH	VSS	VDD1	VDD2	DQ13	VSS	DQ15	DM3	DQS3_t	VDDQ	DQ26	DQ27	VDDQ	DQ30	VSS	VDD2	NC	NC	VSS	NC	NC	NC	VDDCA	NC	NC	NC	NC	NC	VDD1	VSS
AJ	DNU	VSS	DQ12	VDDQ	DQ14	VDDQ	VSS	DQS3_c	DQ24	DQ25	VSS	DQ28	DQ29	DQ31	VDD1	VSS	ZQ1	NC	VDDCA	NC	NC	VSS	NC	NC	NC	VDDCA	NC	VSS	DNU

	Channel
	Power
	Ground
	Do Not Use
	ZQ
	Clock
	NC

NOTE 1 12x12 mm, 0.4 mm pitch, 29 rows

NOTE 2 216 Ball Count

NOTE 3 Top View, A1 in Top Left Corner

NOTE 4 See JESD21-C, 3.12.2 (MO-273, Issue: C, Item: 11-841, Variation: VCCCDB)

NOTE 5 ODT pin is NOT supported. ODT die pads are connected to V_{SS} inside the package.

NOTE 6 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is NC

NOTE 7 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if present).

NOTE 8 Consult manufacturer for guidance concerning Single Channel A and Single Channel B ballout support availability.

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2.1.4 256-ball 14 mm x 14 mm, 0.4 mm Pitch Dual-Channel POP FBGA (top view) Using Variation VEECDB for MO-273

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	DNU	DNU	VDD2	DQ30_a	DQ28_a	DQ27_a	VDDQ	DQ24_a	DQS3_t_a	VDDQ	VDD2	DQ15_a	VDDQ	DQ12_a	DQ11_a	VDDQ	DQ8_a	DQS1_t_a	VDDQ	VDD2	ODT_a	Vref(DQ)_a	VDDQ	DQS0_c_a	DQ7_a	VDDQ	DQ4_a	DQ3_a	VDDQ	DQ0_a	VDDQ	VDD2	DNU	DNU	A
B	DNU	VSS	VDD1	DQ31_a	DQ29_a	VSS	DQ26_a	DQ25_a	VSS	DQS3_c_a	DM3_a	VSS	DQ14_a	DQ13_a	VSS	DQ10_a	DQ9_a	VSS	DQS1_c_a	DM1_a	VSS	DM0_a	DQS0_t_a	VSS	DQ6_a	DQ5_a	VSS	DQ2_a	DQ1_a	VSS	DM2_a	VDD1	VSS	DNU	B
C	VDD2	VDD1																														DQS2_c_a	VDDQ	C
D	DQ17_b	DQ16_b																														VSS	DQS2_t_a	D
E	DQ19_b	DQ18_b																														DQ22_a	DQ23_a	E
F	DQ20_b	VSS																														DQ21_a	VDDQ	F
G	VDDQ	DQ21_b																														VSS	DQ20_a	G
H	DQ23_b	DQ22_b																														DQ18_a	DQ19_a	H
J	DQS2_t_b	VSS																														DQ16_a	DQ17_a	J
K	VDDQ	DQS2_c_b																														VSS	VDDQ	K
L	VDD2	DM2_b																														VDD1	VDD2	L
M	DQ0_b	VSS																														VSS	VSS	M
N	VDDQ	DQ1_b																														CA0_b	VDDCA	N
P	DQ3_b	DQ2_b																														CA2_b	CA1_b	P
R	DQ4_b	VSS																														VSS	VDD2	R
T	VDDQ	DQ5_b																														CA4_b	CA3_b	T
U	DQ7_b	DQ6_b																														CS1_n_b	CS0_n_b	U
V	DQS0_c_b	VSS																														CKE1_b	CKE0_b	V
W	VDDQ	DQS0_t_b																														VSS	VDDCA	W
Y	Vref(DQ)_b	DM0_b																														CK_c_b	CK_t_b	Y
AA	ODT_b	VSS																														Vref(CA)_b	VDD2	AA
AB	VDD2	DM1_b																														VSS	VDDCA	AB
AC	VDDQ	DQS1_c_b																														CA6_b	CA5_b	AC
AD	DQS1_t_b	VSS																														VSS	CA7_b	AD
AE	DQ8_b	DQ9_b																														CA8_b	VDDCA	AE
AF	VDDQ	DQ10_b																														ZQ0_b	CA9_b	AF
AG	DQ11_b	VSS																														RFU	ZQ1_b	AG
AH	DQ12_b	DQ13_b																														VDD1	VDD2	AH
AJ	VDDQ	DQ14_b																														VSS	VSS	AJ
AK	DQ15_b	VSS																														DNU	DNU	AK
AL	VDDQ	DM3_b																														DNU	DNU	AL
AM	VDD2	VDD1																														DNU	DNU	AM
AN	DNU	VSS	DQS3_c_b	VSS	DQ25_b	DQ26_b	VSS	DQ29_b	DQ31_b	VSS	VDD1	RFU	ZQ0_a	CA8_a	VSS	CA6_a	VSS	Vref(CA)_a	CK_c_a	VSS	CKE1_a	CS1_n_a	CA4_a	VSS	CA2_a	CA0_a	VSS	VDD1	VSS	DNU	DNU	DNU	DNU	DNU	AN
AP	DNU	DNU	VDDQ	DQS3_t_b	DQ24_b	VDDQ	DQ27_b	DQ28_b	DQ30_b	VDDQ	VDD2	ZQ1_a	CA9_a	VDDCA	CA7_a	CA5_a	VDDCA	VDD2	CK_t_a	VDDCA	CKE0_a	CS0_n_a	CA3_a	VDD2	CA1_a	VDDCA	VSS	VDD2	VSS	DNU	DNU	DNU	DNU	DNU	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

NOTE 1 14 mm x 14 mm, 0.4 mm pitch, 34 rows x 34 columns
NOTE 2 256 ball count
NOTE 3 Top View, A1 in Top Left Corner
NOTE 4 ODT_A (ODT_B) will be connected to rank 0 of channel A (channel B). The ODT inputs to rank 1 (if 2nd rank is present) will be connected to V_{SS} in the package.
NOTE 5 For channel A (channel B) using x32 DRAM
-ZQ0_A (ZQ0_B) is connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).
-ZQ1_A (ZQ1_B) is NC.
NOTE 6 For Channel A (channel B) using x16 DRAM
-ZQ0_A (ZQ0_B) is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).
-ZQ1_A (ZQ1_B) is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).

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2.1.5 256-ball 14 mm x 14 mm, 0.4 mm Pitch Single Channel-A POP FBGA (top view) Using Variation VEECDB for MO-273

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	DNU	VDD2	DQ30	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	VDD2	DQ15	VDDQ	DQ12	DQ11	VDDQ	DQ8	DQS1_t	VDDQ	VDD2	ODT	Vref(DQ)	VDDQ	DQS0_c	DQ7	VDDQ	DQ4	DQ3	VDDQ	DQ0	VDDQ	VDD2	DNU	DNU	A
B	DNU	VDD1	DQ31	DQ29	VSS	DQ26	DQ25	VSS	DQS3_c	DM3	VSS	DQ14	DQ13	VSS	DQ10	DQ9	VSS	DQS1_c	DM1	VSS	DM0	DQS0_t	VSS	DQ6	DQ5	VSS	DQ2	DQ1	VSS	DM2	VDD1	VSS	DNU	B
C	VDD2	VDD1																														DQS2_c	VDDQ	C
D	NC	NC																														VSS	DQS2_t	D
E	NC	NC																														DQ22	DQ23	E
F	NC	VSS																														DQ21	VDDQ	F
G	VDDQ	NC																														VSS	DQ20	G
H	NC	NC																														DQ18	DQ19	H
J	NC	VSS																														DQ16	DQ17	J
K	VDDQ	NC																														VSS	VDDQ	K
L	VDD2	NC																														VDD1	VDD2	L
M	NC	VSS																														VSS	VSS	M
N	VDDQ	NC																														NC	VDDCA	N
P	NC	NC																														NC	NC	P
R	NC	VSS																														VSS	VDD2	R
T	VDDQ	NC																														NC	NC	T
U	NC	NC																														NC	NC	U
V	NC	VSS																														NC	NC	V
W	VDDQ	NC																														VSS	VDDCA	W
Y	NC	NC																														NC	NC	Y
AA	NC	VSS																														NC	VDD2	AA
AB	VDD2	NC																														VSS	VDDCA	AB
AC	VDDQ	NC																														NC	NC	AC
AD	NC	VSS																														VSS	NC	AD
AE	NC	NC																														NC	VDDCA	AE
AF	VDDQ	NC																														NC	NC	AF
AG	NC	VSS																														NC	NC	AG
AH	NC	NC																														VDD1	VDD2	AH
AJ	VDDQ	NC																														VSS	VSS	AJ
AK	NC	VSS																														DNU	DNU	AK
AL	VDDQ	NC																														DNU	DNU	AL
AM	VDD2	VDD1																														DNU	DNU	AM
AN	DNU	VSS	NC	VSS	NC	NC	VSS	NC	NC	VSS	VDD1	RFU	ZQ0	CA8	VSS	CA6	VSS	Vref(CA)	CK_c	VSS	CKE1	CS1_n	CA4	VSS	CA2	CA0	VSS	VDD1	VSS	DNU	DNU	DNU	DNU	DNU	AN
AP	DNU	DNU	VDDQ	NC	NC	VDDQ	NC	NC	NC	VDDQ	VDD2	ZQ1	CA9	VDDCA	CA7	CA5	VDDCA	VDD2	CK_t	VDDCA	CKE0	CS0_n	CA3	VDD2	CA1	VDDCA	VSS	VDD2	VSS	DNU	DNU	DNU	DNU	DNU	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

NOTE 1 14 mm x 14 mm, 0.4mm pitch, 34 rows x 34 columns
NOTE 2 256 ball count
NOTE 3 Top View, A1 in Top Left Corner
NOTE 4 ODT will be connected to rank 0. The ODT inputs to rank 1 (if 2nd rank is present) will be connected to V_{SS} in the package.
NOTE 5 Using x32 DRAM
-ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).
-ZQ1 is NC.
NOTE 6 Using x16 DRAM
-ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).
-ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).

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2.1.6 168-ball 12 mm x 12 mm, 0.5 mm pitch single channel x32 PoP with optional e•MMC using Variation VCCBCB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	DNU	DNU	CMD	CLK	DAT6	VCCm	DAT4	DAT2	VCCQm	DAT0	VDD1	VSS	DQ30	DQ29	VSS	DQ26	DQ25	VSS	DQS3_c	VDD1	VSS	DNU	DNU	A
B	DNU	DNU	VDD1	DAT7	VSSm	DAT5	DAT3	VSSm	DAT1	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	DM3	VDD2	DNU	DNU	B
C	VSS	VDD2																				DQ15	VSS	C
D	DNU	DNU																				VDDQ	DQ14	D
E	VSF1	VSF2																				DQ12	DQ13	E
F	VDDImm	VSSm				VCCm	3	(3V or 1.8V depending on technology)		VSSmm	5											DQ11	VSS	F
G	VSF3	VSF4				VCCQm	2	(includes VDDI)						x32 LPDDR3 DQs								VDDQ	DQ10	G
H	VSF5	VSF6				VDD2	8			VSS	24			LPDDR3 CMD/Address								DQ8	DQ9	H
J	VCCm	VSSm				VDD1	7							LPDDR3 ZQ								DQS1_t	VSS	J
K	VSF7	VSF8				VDDCA	3							eMMC ADQ/CTRL								VDDQ	DQS1_c	K
L	RST_n	VSF9				VDDQ	12							eMMC VSF								VDD2	DM1	L
M	DNU	VSS				VREF	2							Power								VREF (DQ)	VSS	M
N	DNU	VDD1												Ground								VDD1	DM0	N
P	ZQ0	VREF (CA)																				DQS0_c	VSS	P
R	VSS	VDD2				DNU	29															VDDQ	DQS0_t	R
T	CA9	CA8																				DQ6	DQ7	T
U	CA7	VDDCA																				DQ5	VSS	U
V	VSS	CA6																				VDDQ	DQ4	V
W	CA5	VDDCA																				DQ2	DQ3	W
Y	CK_c	CK_t																				DQ1	VSS	Y
AA	VSS	VDD2																				VDDQ	DQ0	AA
AB	DNU	DNU	CS0_n	CS1_n	VDD1	CA1	VSS	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_t	VDDQ	DM2	VDD2	DNU	DNU	AB
AC	DNU	DNU	CKE0	CKE1	VSS	CA0	CA2	VDDCA	VSSm	VCCm	ZQ1	VSS	DQ17	DQ19	VSS	DQ21	DQ23	VSS	DQS2_c	VDD1	VSS	DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

NOTE 1 body 12mm x 12 mm, 0.5 mm pitch, 23 rows
NOTE 2 168 Ball Count
NOTE 3 Top View, A1 in Top Left Corner
NOTE 4 See JESD21-C, 3.12.2 (MO-273)
NOTE 5 ODT pin is NOT supported. ODT die pads are connected to VSS inside the package
NOTE 6 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is NC

NOTE 7 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if present).

NOTE 8 For DRAM-only configurations, VSSm balls may be either NC or connected to VSS
NOTE 9 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

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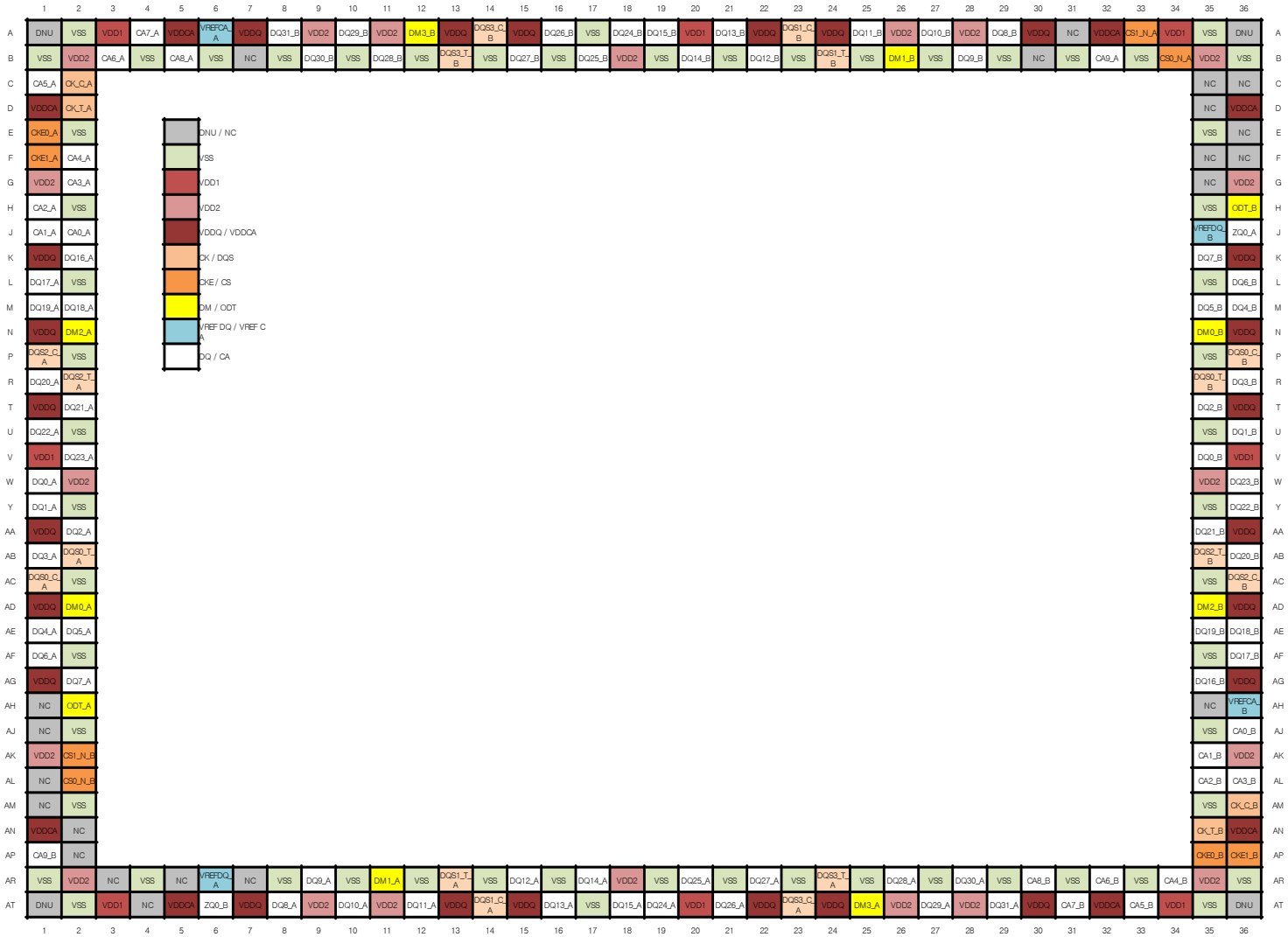
2.1.7 272-ball 15 mm x 15 mm, 0.4 mm pitch, Dual-Channel POP FBGA (top view) Using Variation VFFCDB for MO-273



NOTE 1 15 mm x 15 mm, 0.4 mm ball pitch
NOTE 2 272 ball count, 36 rows
NOTE 3 Top View, A1 in top left corner
NOTE 4 ODT_A and ODT_B will be connected to rank 0. The ODT inputs to rank 1 (if 2nd rank is present) will be connected to VSS in the package.
NOTE 5 Using x32 DRAM, ZQ0_A and ZQ0_B balls are connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present).

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2.1.8 136-ball 10 mm x 10 mm, 0.50 mm pitch POP (e•MMC5.0 + LPDDR3) FBGA (top view), Using Variation xAABCB for MO-273C

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	DNU	VSSm	DS	CLK	DAT7	VCCQ	DAT4	DAT3	VCCQ	DAT0	VSS	VDDQ	DQ29	DQ28	VSS	DQ26	DQ24	VSS	DNU
B	VSS	VCC	VDDI	VSSm	DAT6	DAT5	VSSm	VCC	DAT2	DAT1	VSSm	DQ31	DQ30	VDDQ	DQ27	DQ25	VDDQ	VDD1	VSS
C	ZQ	CMD																DQS3_t	DQS3_c
D	CA9	RST_n																VDD2	DM3
E	CA8	VDDCA																DQ15	VSS
F	VSS	CA7																VDDQ	DQ14
G	CA6	VDD2																DQ12	DQ13
H	CA5	VDD1																DQ11	VSS
J	VSS	Vref(CA)																VDDQ	DQ10
K	CK_t	CK_c																DQ9	DQ8
L	VSS	VDD2																VDDQ	VSS
M	CKE1	VSS																DQS1_t	DQS1_c
N	CKE0	CS1_n																VSS	DM1
P	CA4	CS0_n																VDD1	VDD2
R	VDDCA	CA3																Vref(DQ)	VSS
T	CA2	VSS																VDDQ	DM0
U	CA1	CA0																DQS0_t	DQS0_c
V	VSS	VDD1	VDD2	DQ17	DQ18	VSS	DQ21	DQ22	VSS	DQS2_t	VDDQ	DQ0	VDDQ	DQ3	DQ4	VSS	DQ7	VDDQ	VSS
W	DNU	VSS	VSS	DQ16	VDDQ	DQ19	DQ20	VDDQ	DQ23	DQS2_c	DM2	VSS	DQ1	DQ2	VDD2	DQ6	DQ5	VSS	DNU

NOTE 1 10 mm x 10 mm, 0.5 mm pitch
NOTE 2 136 ball count, 19rows x 19 columns
NOTE 3 Top View, A1 in Top Left Corner
NOTE 4 ODT pin is NOT supported, ODT die pads are connected to VSS inside the package.
NOTE 5 ZQ is connected to rank0 and rank1 DRAM (if present)
NOTE 6 For DRAM-only configurations, VSSm balls may be either NC or connected to VSS.

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2.2 FBGA Package Ball-outs

2.2.1 253-Ball 0.5 mm Pitch Discrete Dual-Channel FBGA (top view) Using Variation EA for MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	NC	VSS	VSS	VSS	VSS	VDDCA	VDD2	VSS	VDDCA	Vref(CA)_a	VDD2	VSS	VDDQ	VSS	VDD1	VDD1	NC	A
B	VSS	VDD1	VSS	VSS	CA0_a	CA3_a	CS1_n_a	CK_t_a	VDDCA	CA7_a	ZQ0_a	VDDQ	DQ28_b	DQ29_b	DQ30_b	DQ31_b	VDD2	B
C	VSS	VSS	VDD2	VSS	CA1_a	CA4_a	CKE0_a	CK_c_a	CA5_a	CA8_a	ZQ1_a	VDDQ	DQ24_b	DQ25_b	DQ26_b	DQ27_b	VDD2	C
D	VSS	VSS	VSS	VSS	CA2_a	CS0_n_a	CKE1_a	RFU	CA6_a	CA9_a	RFU	VSS	DQ15_b	DM3_b	DQS3_c_b	DQS3_t_b	VSS	D
E	VDDCA	ZQ0_b	ZQ1_b	RFU	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DQ11_b	DQ12_b	DQ13_b	DQ14_b	VDDQ	E
F	VSS	CA7_b	CA8_b	CA9_b	VSS								DM1_b	DQ8_b	DQ9_b	DQ10_b	VSS	F
G	VSS	VDDCA	CA5_b	CA6_b	VSS							VDDQ	DQS1_c_b	DQS1_t_b	VSS	VSS	VDDQ	G
H	VDD2	CK_c_b	CK_t_b	RFU	VSS							VSS	ODT_b	DM0_b	VSS	VDD2	Vref(DQ)_b	H
J	Vref(CA)_b	CS1_n_b	CKE0_b	CKE1_b	VSS							RFU	DQS0_c_b	DQS0_t_b	DQ6_b	DQ7_b	VSS	J
K	VDDCA	CA3_b	CA4_b	CS0_n_b	VSS							VDDQ	DQ2_b	DQ3_b	DQ4_b	DQ5_b	VDDQ	K
L	VDD2	CA0_b	CA1_b	CA2_b	VSS							VSS	DQ23_b	DM2_b	DQ0_b	DQ1_b	VDDQ	L
M	VSS	VDDQ	VDDQ	VSS	VSS	VSS	VDDQ	VSS	RFU	VDDQ	VSS	VDDQ	DQ21_b	DQ22_b	DQS2_c_b	DQS2_t_b	VSS	M
N	VDDQ	DQ19_a	DQ23_a	DQ0_a	DQ4_a	DM0_a	DQS0_c_a	ODT_a	DQS1_c_a	DQ13_a	DQ24_a	DQ25_a	VSS	DQ18_b	DQ19_b	DQ20_b	VSS	N
P	VSS	DQ18_a	DQ22_a	DM2_a	DQ3_a	DQ7_a	DQS0_t_a	DM1_a	DQS1_t_a	DQ12_a	DM3_a	DQ26_a	DQ29_a	VSS	DQ16_b	DQ17_b	VDDQ	P
R	VDD1	DQ17_a	DQ21_a	DQS2_c_a	DQ2_a	DQ6_a	VSS	VSS	DQ9_a	DQ11_a	DQ15_a	DQS3_c_a	DQ28_a	DQ31_a	VDD2	VSS	VSS	R
T	VDD1	DQ16_a	DQ20_a	DQS2_t_a	DQ1_a	DQ5_a	VSS	VDD2	DQ8_a	DQ10_a	DQ14_a	DQS3_t_a	DQ27_a	DQ30_a	VSS	VDD1	VSS	T
U	NC	VDD2	VDD2	VSS	VDDQ	VSS	VDDQ	Vref(DQ)_a	VSS	VDDQ	VDDQ	VSS	VSS	VDDQ	VSS	VSS	NC	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

NOTE 1 ODT_A (ODT_B) will be connected to rank 0 of channel A (channel B). The ODT inputs to rank 1 (if 2nd rank is present) will be connected to V_{SS} in the package.

NOTE 2 For channel A (channel B) using x32 DRAM

- ZQ0_A (ZQ0_B) is connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).
- ZQ1_A (ZQ1_B) is NC.

NOTE 3 For Channel A (channel B) using x16 DRAM

- ZQ0_A (ZQ0_B) is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).
- ZQ1_A (ZQ1_B) is connected to Byte 2-3 of rank 0 DRAM

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2.2.2 178-Ball Discrete Single-Channel FBGA (top view) Using Variation AA for MO-311

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	VSS	ZQ0	ZQ1	VSS	VSS		DQ31 NC	DQ30 NC	DQ29 NC	DQ28 NC	VSS	DNU	B
C		CA9	VSS	NC	VSS	VSS		DQ27 NC	DQ26 NC	DQ25 NC	DQ24 NC	VDDQ		C
D		CA8	VSS	VDD2	VDD2	VDD2		DM3 NC	DQ15	DQS3_t NC	DQS3_c NC	VSS		D
E		CA7	CA6	VSS	VSS	VSS		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	VSS	VSS	VSS		DQ11	DQ10	DQ9	DQ8	VSS		F
G		VDDCA	VSS	VSS	VDD2	VSS		DM1	VSS	DQS1_t	DQS1_c	VDDQ		G
H		VSS	VDDCA	Vref(CA)	VDD2	VDD2		VDDQ	VDDQ	VSS	VDDQ	VDD2		H
J		CK_c	CK_t	VSS	VDD2	VDD2		ODT	VDDQ	VDDQ	Vref(DQ)	VSS		J
K		VSS	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	VSS	VDDQ	VDD2		K
L		VDDCA	CS0_n	CS1_n	VDD2	VSS		DM0	VSS	DQS0_t	DQS0_c	VDDQ		L
M		VDDCA	CA4	VSS	VSS	VSS		DQ4	DQ5	DQ6	DQ7	VSS		M
N		CA2	CA3	VSS	VSS	VSS		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	VSS	VDD2	VDD2	VDD2		DM2	DQ0	DQS2_t NC	DQS2_c NC	VSS		P
R		CA0	NC	VSS	VSS	VSS		DQ20 NC	DQ21 NC	DQ22 NC	DQ23 NC	VDDQ		R
T	DNU	VSS	VSS	VSS	VSS	VSS		DQ16 NC	DQ17 NC	DQ18 NC	DQ19 NC	VSS	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTE 1 When using the x16 configuration DQ16 through DQ31 become NC as indicated by the second row of signal names for those signals in the ball-out diagram.

NOTE 2 0.8 mm pitch (X-axis), 0.65mm pitch (Y-axis), x16/x32, 17 rows

NOTE 3 Top View, A1 in Top Left Corner

NOTE 4 See JESD21-C, 3.12.1

NOTE 5 ODT will be connected to rank 0. The ODT input to rank 1 (if 2nd rank is present) will be connected to V_{SS} in the package.

NOTE 6 For Channel using x32 DRAM

- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is NC

NOTE 7 For Channel using x16 DRAM

- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if present).

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2.2.3 346-ball 0.5 mm Pitch Dual-Channel Multi-Chip Package (MCP) FBGA (top view) Using Variation AP for MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A				NC			NC				NC				NC			NC			
B																					
C	NC		DNU	DNU	CLEn VSF1m	VCCn VCCQm	R/B0n DATA5m	VCCn VCCQm	R/B1n CLKm	VCCn VCCQm	CEB1n RSTm	VCCn VCCQm	CEB0n VSF2m	VCCn VCCQm	REBn VCCm	VCCn VCCm	VSSn VSSm	DNU	DNU		NC
D			DNU	NCn VCCQm	WEBn NCm	VSSn VSSQm	IO6n DAT1m	VSSn VSSQm	IO4n DAT2m	VSSn VSSQm	IO2n VSF3m	VSSn VSSQm	IO0n NCm	VSSn VSSQm	ALEn VCCm	VSSn VSSm	VSSn VSSm	NCn NCm	DNU		
E			VCCn VCCm	NCn VSSQm	VCCn VCCm	NCn VSSQm	IO14n DAT4m	NCn VSSQm	IO12n DAT6m	NCn VSSQm	IO10n NCm	NCn VSSQm	IO8n NCm	NCn VDDIm	WPBn VCCm	NCn VSF4m	NCn NCm	NCn NCm	NCn VSF5m		
F			VCCn VCCm	VSSn VSSm	VCCn VCCm	NCn VSSQm	IO7n DAT0m	NCn VSSQm	IO5n DAT3m	NCn VSSQm	IO3n NCm	NCn VSSQm	IO1n NCm	NCn VSF6m	NCn NCm	NCn NCm	NCn NCm	NCn NCm	NCn NCm		
G			VSSn VSSm	VSSn VSSm		NCn VSF7m	IO15n CMDm			IO13n DAT7m	IO11n NCm	IO9n VSF8m			NCn NCm	NCn NCm		NCn VSF9m	NCn NCm		
H																					
J																					
K																					
L			NC	VSS	VSS	VSS	VSS	VDDCA	VDD2	VSS	VDDCA	Vref(CA)_a	VDD2	VSS	VDDQ	VSS	VDD1	VDD1	NC		
M			VSS	VDD1	VSS	VSS	CA0_a	CA3_a	CS1_n_a	CK_t_a	VDDCA	CA7_a	ZQ0_a	VDDQ	DQ28_b	DQ29_b	DQ30_b	DQ31_b	VDD2		
N			VSS	VSS	VDD2	VSS	CA1_a	CA4_a	CKE0_a	CK_c_a	CA5_a	CA8_a	ZQ1_a	VDDQ	DQ24_b	DQ25_b	DQ26_b	DQ27_b	VDD2		
P			VSS	VSS	VSS	VSS	CA2_a	CS0_n_a	CKE1_a	RFU	CA6_a	CA9_a	RFU	VSS	DQ15_b	DM3_b	DQS3_c_b	DQS3_t_b	VSS		
R			VDDCA	ZQ0_b	ZQ1_b	RFU	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DQ11_b	DQ12_b	DQ13_b	DQ14_b	VDDQ		
T			VSS	CA7_b	CA8_b	CA9_b	VSS							VSS	DM1_b	DQ8_b	DQ9_b	DQ10_b	VSS		
U			VSS	VDDCA	CA5_b	CA6_b	VSS							VDDQ	DQS1_c_b	DQS1_t_b	VSS	VSS	VDDQ		
V			VDD2	CK_c_b	CK_t_b	RFU	VSS							VSS	ODT_b	DM0_b	VSS	VDD2	Vref(DQ)_b		
W			Vref(CA)_b	CS1_n_b	CKE0_b	CKE1_b	VSS							RFU	DQS0_c_b	DQS0_t_b	DQ6_b	DQ7_b	VSS		
Y			VDDCA	CA3_b	CA4_b	CS0_n_b	VSS							VDDQ	DQ2_b	DQ3_b	DQ4_b	DQ5_b	VDDQ		
AA			VDD2	CA0_b	CA1_b	CA2_b	VSS							VSS	DQ23_b	DM2_b	DQ0_b	DQ1_b	VDDQ		
AB			VSS	VDDQ	VDDQ	VSS	VSS	VSS	VDDQ	VSS	RFU	VDDQ	VSS	VDDQ	DQ21_b	DQ22_b	DQS2_c_b	DQS2_t_b	VSS		
AC			VDDQ	DQ19_a	DQ23_a	DQ0_a	DQ4_a	DM0_a	DQS0_c_a	ODT_a	DQS1_c_a	DQ13_a	DQ24_a	DQ25_a	VSS	DQ18_b	DQ19_b	DQ20_b	VSS		
AD			VSS	DQ18_a	DQ22_a	DM2_a	DQ3_a	DQ7_a	DQS0_t_a	DM1_a	DQS1_t_a	DQ12_a	DM3_a	DQ26_a	DQ29_a	VSS	DQ16_b	DQ17_b	VDDQ		
AE			VDD1	DQ17_a	DQ21_a	DQS2_c_a	DQ2_a	DQ6_a	VSS	VSS	DQ9_a	DQ11_a	DQ15_a	DQS3_c_a	DQ28_a	DQ31_a	VDD2	VSS	VSS		
AF			VDD1	DQ16_a	DQ20_a	DQS2_t_a	DQ1_a	DQ5_a	VSS	VDD2	DQ8_a	DQ10_a	DQ14_a	DQS3_t_a	DQ27_a	DQ30_a	VSS	VDD1	VSS		
AG	NC		NC	VDD2	VDD2	VSS	VDDQ	VSS	VDDQ	Vref(DQ)_a	VSS	VDDQ	VDDQ	VSS	VSS	VDDQ	VSS	VSS	NC		NC
AH																					
AJ				NC			NC				NC				NC			NC			

NOTE 1 0.5mm ball pitch, 346 ball count

NOTE 2 Target package sizes : 12mm x 16mm and 14mm x 18mm

NOTE 3 Target package, size depends on Flash density.

NOTE 4 Top view, A1 in top left corner

NOTE 5 ODT_A (ODT_B) will be connected to rank 0 of channel A (channel B). The ODT inputs to rank 1 (if 2nd rank is present) will be connected to V_{SS} in the package.

NOTE 6 For channel A (channel B) using x32 DRAM

- ZQ0_A (ZQ0_B) is connected to rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).
- ZQ1_A (ZQ1_B) is NC.

NOTE 7 For Channel A (channel B) using x16 DRAM

- ZQ0_A (ZQ0_B) is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).
- ZQ1_A (ZQ1_B) is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if 2nd rank is present) of channel A (channel B).

NOTE 8 For flash ball-out, “n” ball assignments are used for NAND flash, and “m” ball assignments for e-MMC.

NOTE 9 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessability and may be used for general purpose vendor specific operations.

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2.2.4 221-ball 0.5 mm Pitch Multi-Chip Package LPDDR3 x32+eMMC/NAND MCP (top view) Using Variation EB for MO276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DNU	VSF1	VSSm	VCCQ	DAT6	CMD	~~RFU~~DS	VSSm	DAT0	DAT5	VDDI	VSSm	VSF2	DNU
B	VSF3	VSSm	VCC	DAT7	DAT3	VCCQ	VSSm	CLK	VCCQ	DAT1	VSSm	VCC	VCC	VSF4
C		RST_n	VSSm	VCC	VSSm	DAT2	VCCQ	VSSm	DAT4	VSSm	VCCQ	VSSm	VSSm	
D		VSF5	VSF6	VSF7	VSF8	VSF9	VSSm	VCC						
E														
F		VSS	VDD1	VDD1	VDD2			VDD2	VDD1	DQ29	DQ30	DQ31	VSS	
G		ZQ_0	ZQ_1	VSS	VDD1			VSS	VDDQ	DQ26	VSS	DQ27	DQ28	
H		CA9	VSS	VSS	VSS			VDDQ	DQS3_t	VSS	DQ24	VDDQ	DQ25	
J		CA8	CA7	VSS	VDD2			VSS	DQS3_c	DM3	VDDQ	DQ15	VSS	
K		VDDCA	CA6	VSS	VDD2			VSS	VSS	VDDQ	DQ13	VDDQ	DQ14	
L		VDD2	CA5	VSS	VDD2			VDDQ	VDDQ	VSS	DQ12	VSS	DQ11	
M		V_{REF}(CA)	VSS	VSS	VDD2			VSS	DQS1_t	VDDQ	DQ10	VDDQ	DQ9	
N		VDDCA	CK_c	VSS	VDD2			VSS	DQS1_c	DM1	VDDQ	DQ8	VSS	
P		VSS	CK_t	VSS	VDD2			VDD2	VSS	ODT	VDD2	VSS	V_{REF}(DQ)	
R		CKE1	VSS	VSS	VDD2			VSS	DQS0_c	DM0	VDDQ	DQ7	VSS	
T		CKE0	CS1_n	VSS	VDD2			VSS	DQS0_t	VDDQ	DQ5	VDDQ	DQ6	
U		VDDCA	CS0_n	VSS	VDD2			VDDQ	VDDQ	VSS	DQ3	VSS	DQ4	
V		VDDCA	CA4	VSS	VDD2			VSS	VSS	VDDQ	DQ1	VDDQ	DQ2	
W		CA2	CA3	VSS	VDD2			VSS	DQS2_c	DM2	VDDQ	DQ0	VSS	
Y		CA0	CA1	VSS	VSS			VDDQ	DQS2_t	VSS	DQ23	VDDQ	DQ22	
AA	DNU	VSS	VDD1	VSS	VDD1			VSS	VDDQ	DQ21	VSS	DQ20	DQ19	DNU
AB	DNU	DNU	VDD1	VDD1	VDD2			VDD2	VDD1	DQ18	DQ17	DQ16	DNU	DNU

NOTE 1 0.5mm ball pitch, 221 ball count
NOTE 2 Target package sizes : 11.5mm x 13mm and TBDmm x TBDmm
NOTE 3 Target package, size depends on Flash density.
NOTE 4 Top view, A1 in top left corner
NOTE 5 ODT will be connected to rank 0. The ODT input to rank 1 (if 2nd rank is present) will be connected to VSS in the package.
NOTE 6 For Channel using x32 DRAM
- ZQ0 is connected to rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is NC

NOTE 7 For Channel using x16 DRAM
- ZQ0 is connected to Byte 0-1 of rank 0 DRAM and rank 1 DRAM (if present).
- ZQ1 is connected to Byte 2-3 of rank 0 DRAM and rank 1 DRAM (if present).

NOTE 8 The flash ball-out is based on eMMC.
NOTE 9 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

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2.3 LPDDR3 Pad Sequence

Table 1 — LPDDR3 Pad Sequence

CA Pad Seq	DQ Pad Sequence	
	x32	x16
VDD2	VDD2	VDD2
VSS	VSS	VSS
VSS	VSS *1	VSS *1
VDD1	VDD1	VDD1
VDD2	VDDQ	
VSS	VSSQ	
	DQ31	
	DQ30	
	VDDQ	
	DQ29	
	DQ28	
	VSSQ	
	DQ27	
	DQ26	
	VDDQ	
	DQ25	
	DQ24	
	VSSQ	
	DQS3_t	
	DQS3_c	
	VDDQ	
	DM3	
	VSSQ	VSSQ
	DQ15	DQ15
	DQ14	DQ14
	VDDQ	VDDQ
	DQ13	DQ13
	DQ12	DQ12
	VSSQ	VSSQ
	DQ11	DQ11
	DQ10	DQ10
	VDDQ	VDDQ
ZQ	DQ9	DQ9
CA9	DQ8	DQ8
CA8	VSSQ	VSSQ
VSSCA	DQS1_t	DQS1_t
VDDCA	DQS1_c	DQS1_c
CA7	VDDQ	VDDQ
CA6	DM1	DM1
CA5	VSSQ	VSSQ
	VDDQ	VDDQ
VDD2	VDD2	VDD2
Vref(CA)	ODT	ODT
VSS	VSS	VSS
VDDCA	Vref(DQ)	Vref(DQ)
CK_c		
CK_t		
VSSCA	VSS	VSS
CKE	VDD2	VDD2
CS_N		
CA4	VDDQ	VDDQ
CA3	VSSQ	VSSQ
CA2	DM0	DM0
VDDCA	VDDQ	VDDQ
VSSCA	DQS0_c	DQS0_c
CA1	DQS0_t	DQS0_t
CA0	VSSQ	VSSQ
	DQ7	DQ7
	DQ6	DQ6
	VDDQ	VDDQ
	DQ5	DQ5
	DQ4	DQ4
	VSSQ	VSSQ
	DQ3	DQ3
	DQ2	DQ2
	VDDQ	VDDQ
	DQ1	DQ1
	DQ0	DQ0
	VSSQ	VSSQ
	DM2	
	VDDQ	
	DQS2_c	
	DQS2_t	
	VSSQ	
	DQ23	
	DQ22	
	VDDQ	
	DQ21	
	DQ20	
	VSSQ	
	DQ19	
	DQ18	
	VDDQ	
	DQ17	
	DQ16	
	VSSQ	
VSS	VDDQ	
VDD2		
VDD1	VDD1	VDD1
VSS	VSS *1	VSS *1
VSS	VSS	VSS
VDD2	VDD2	VDD2

NOTE 1 Pads with (*1) are optional.

NOTE 2 Applications are recommended to follow bit/byte assignments. Bit or byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 3 CA pads and DQ pads shall be separated on opposite sides of die from top of silicon view.

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2.4 LPDDDR3 Pad Definition and Description

Table 2 — Pad Definition and Description

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth Table for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	**Data Inputs/Output:** Bi-directional data bus
DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0 - DM3 (x32)	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
ODT	Input	**On-Die Termination**: This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
V_{DD1}	Supply	**Core Power Supply 1:** Core power supply
V_{DD2}	Supply	**Core Power Supply 2:** Core power supply
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for data input/output buffers.
$V_{REF(CA)}$	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for Input Receivers**
V_{SSQ}	Supply	**I/O Ground:** Ground for data input/output buffers
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

NOTE 1 Data includes DQ and DM.

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3 LPDDR3 Functional Description

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory.

These devices contain the following number of bits:

1 Gb has 1,073,741,824 bits
2 Gb has 2,147,483,648 bits
4 Gb has 4,294,967,296 bits
6 Gb has 6,442,450,944 bits
8 Gb has 8,589,934,592 bits
16 Gb has 17,179,869,184 bits
32 Gb has 34,359,738,368 bits

LPDDR3 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8*n*-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 LPDDR3 SDRAM Addressing

Table 3 — LPDDR3 SDRAM Addressing

Items		1Gb	2Gb	4Gb	6Gb	8Gb	12Gb	16Gb	32Gb
Number of Banks		8	8	8	8	8	8	8	TBD
Bank Addresses		BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	TBD
t_{REFI}(us)[2]		7.8	3.9	3.9	3.9	3.9	3.9	3.9	TBD
x16	Row Addresses	R0-R12	R0-R13	R0-R13	R0-R14[4]	R0-R14	R0-R14[4]	R0-R14	TBD
	Column Addresses[1]	C0-C9	C0-C9	C0-C10	C0-C10	C0-C10	C0-C11	C0-C11	TBD
x32	Row Addresses	R0-R12	R0-R13	R0-R13	R0-R14[4]	R0-R14	R0-R14[4]	R0-R14	TBD
	Column Addresses[1]	C0-C8	C0-C8	C0-C9	C0-C9	C0-C9	C0-C10	C0-C10	TBD

NOTE 1 The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

NOTE 2 t_{REFI} value for all bank refresh is for *T*c = -25~85 °C, *T*c means Operating Case Temperature. Depending on MR4 settings a refresh multiplier RM applies to the actually required refresh interval t_{REFIM} = RM x t_{REFI}

NOTE 3 Row and Column Address values on the CA bus that are not used are “don’t care.”

NOTE 4 No memory present at addresses with R13=R14=HIGH. ACT command with R13=R14=HIGH is ignored (NOP). Write to R13=R14=HIGH is ignored (NOP).

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3.2 Simplified LPDDR3 State Diagram

LPDDR3-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see Clause 4, LPDDR3 Command Definitions and Timing Diagrams.

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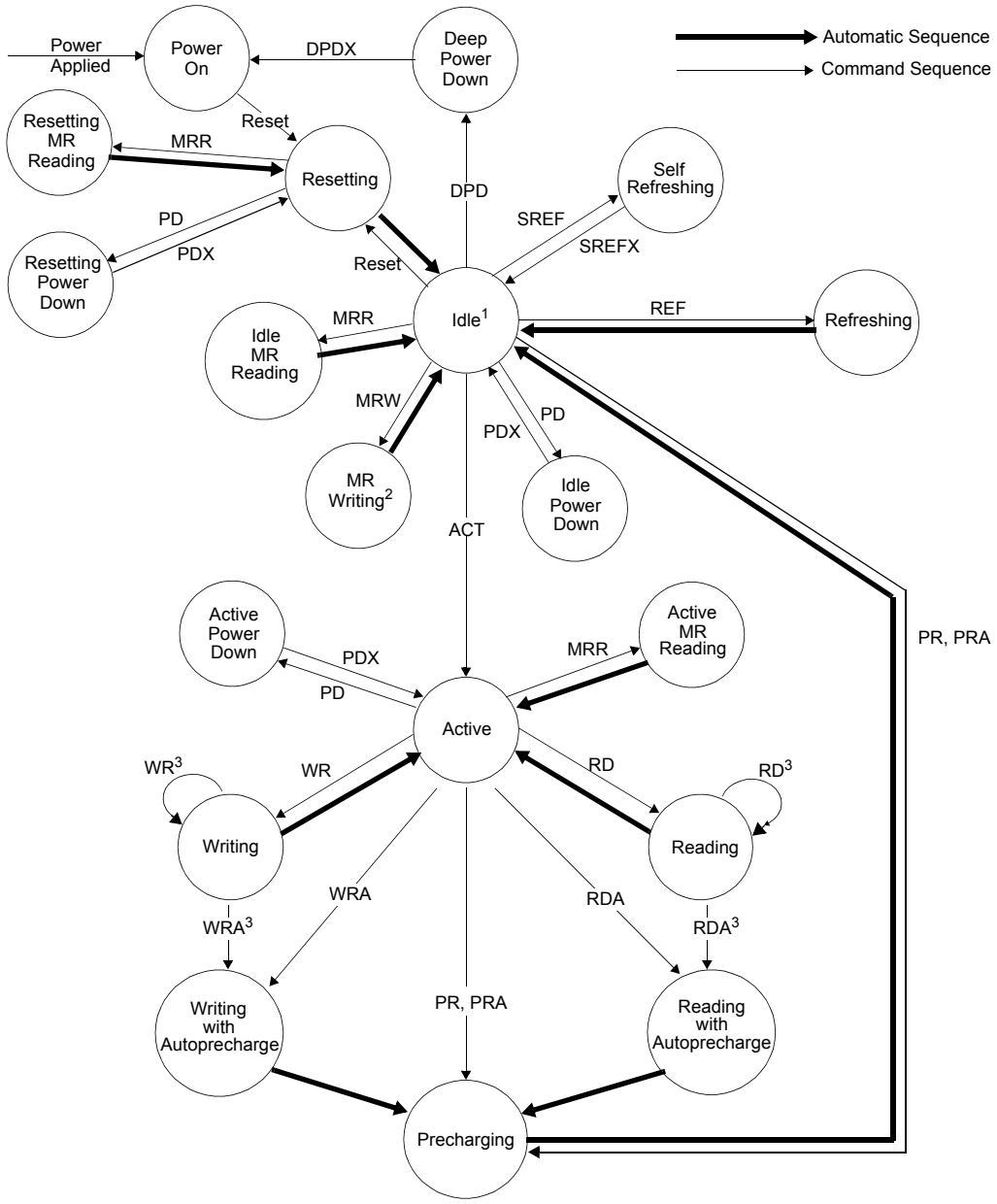
3.2 Simplified LPDDR3 State Diagram (cont'd)



ACT = Activate
PR(A) = Precharge (All)
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
MRW = Mode Register Write
MRR = Mode Register Read
Reset = Reset is achieved through MRW command

PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
REF = Refresh

Figure 1 — LPDDR3: Simplified Bus Interface State Diagram

NOTE 1 In the Idle state, all banks are precharged.
NOTE 2 In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state. In these cases an additional MRW command is required to exit either operating mode and return to the Idle state. See sections "CA Training" or "Write Leveling".
NOTE 3 Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.
NOTE 4 Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not captured in full detail.

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3.3 Power-up, Initialization, and Power-off

3.3.1 Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp: While applying power (after Ta), CKE must be held LOW (≤ 0.2 × V_{DDCA}) and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Table 4.

Table 4 — Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200 mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200 mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200 mV
	V_{Ref} must always be less than all other supply voltages

NOTE 1 Ta is the point when any power supply first reaches 300 mV.
NOTE 2 Noted conditions apply between Ta and power-off (controlled or uncontrolled).
NOTE 3 Tb is the point at which all supply and reference voltages are within their defined operating ranges.
NOTE 4 Power ramp duration t_{INIT0} (Tb - Ta) must not exceed 20 ms.
NOTE 5 The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100 mV.

Beginning at Tb, CKE must remain LOW for at least t_{INIT1}, after which CKE can be asserted HIGH. The clock must be stable at least t_{INIT2} prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS_n, and CA inputs must observe setup and hold requirements (t_{IS}, t_{IH}) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).

If any MRR commands are issued, the clock period must be within the range defined for t_{CKb}. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, t_{DQSCK}) could have relaxed timings (such as t_{DQSCKb}) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least t_{INIT3} (Td). The ODT input signal may be in undefined state until t_{IS} before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of t_{ZQINIT}.

2. RESET Command: After t_{INIT3} is satisfied, the MRW RESET command must be issued (Td).

An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least t_{INIT4} while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during time t_{INIT4}.

3. MRRs and Device Auto Initialization (DAI) Polling: After t_{INIT4} is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. CA Training may only begin after time Tf. User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after t_{INIT5}(max) has expired (whether or not DAI bit has been read by MRR command).As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than t_{INIT5} after the RESET command. The controller must wait at least t_{INIT5}(max) or until the DAI bit is set before proceeding.

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3.3.1 Voltage Ramp and Device Initialization (cont'd)

4. ZQ Calibration: If CA Training is *not* required, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. See "Mode Register Write - CA Training Mode" on page 66 for the CA Training command. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (Tf'), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10).

This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after t_{ZQINIT}.

5. Normal Operation: After t_{ZQINIT} (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the LPDDR3 specification.

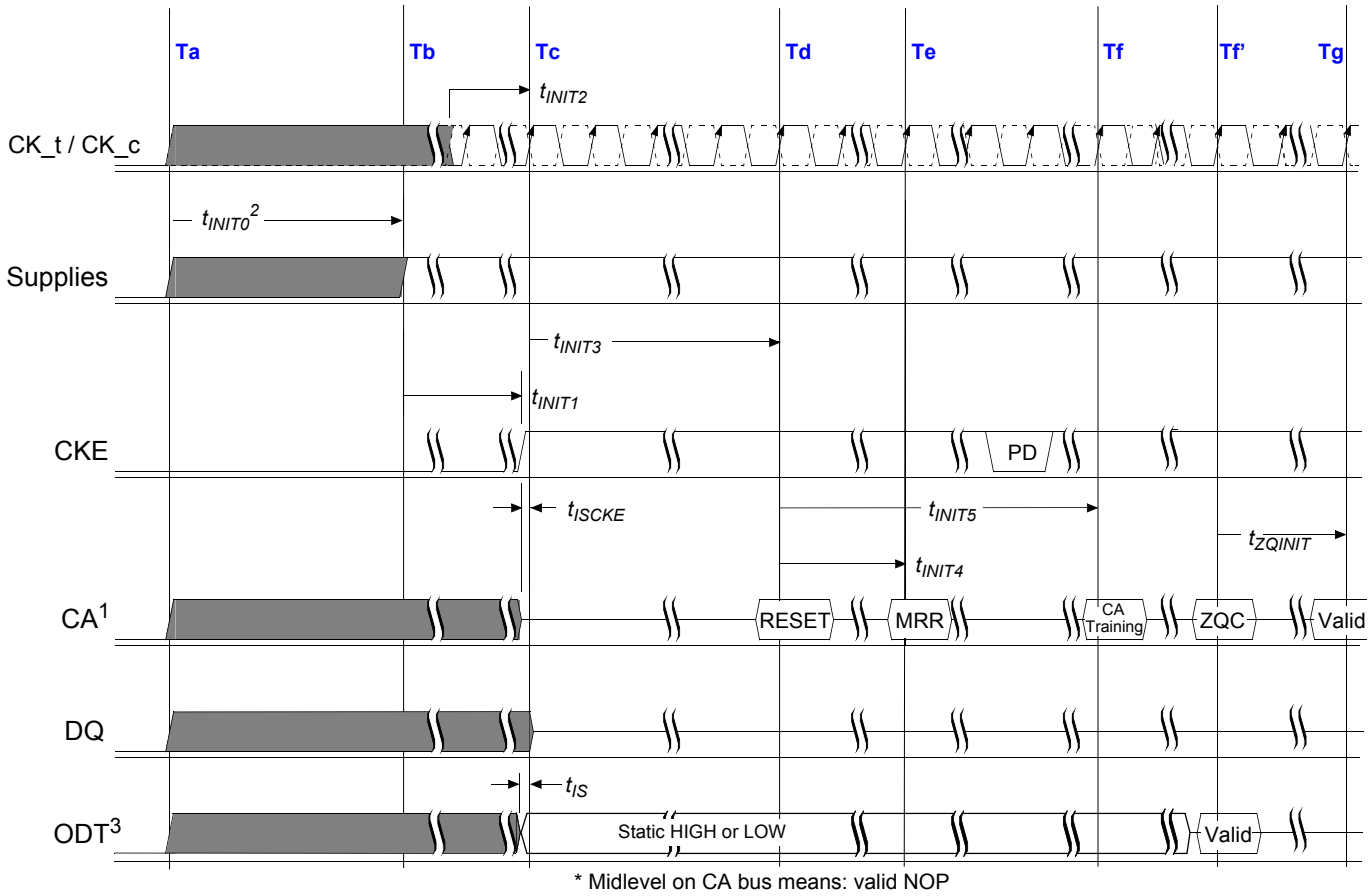

Figure 2 — Voltage Ramp and Initialization Sequence

NOTE 1 High-Z on the CA bus indicates NOP.

NOTE 2 For t_{INIT} values, see Table 5.

NOTE 3 After RESET command (time Te), R_{TT} is disabled until ODT function is enabled by MRW to MR11 following Tg.

NOTE 4 CA Training is optional.

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3.3 Power-up, Initialization, and Power-off (cont'd)

Table 5 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	–	20	ms	Maximum voltage-ramp time
t_{INIT1}	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
t_{INIT2}	5	–	^{t}CK	Minimum stable clock before first CKE HIGH
t_{INIT3}	200	–	µs	Minimum idle time after first CKE assertion
t_{INIT4}	1	–	µs	Minimum idle time after RESET command
t_{INIT5} 1)	–	10	µs	Maximum duration of device auto initialization
t_{ZQINIT}	1	–	µs	ZQ initial calibration
t_{CKb}	18	100	ns	Clock cycle time during boot

NOTE 1 If DAI bit is not read via MRR, SDRAM will be in idle state after tINIT5(max) has expired.

3.3.1.1 Initialization After RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

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3.3.2 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤ 0.2 × V_{DDCA}); all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between V_{SSCA} and V_{DDCA} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see Table 1).

Table 6 — Power Supply Conditions

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}—200mV
Tx and Tz	V_{DD1} must be greater than V_{DDCA}—200mV
Tx and Tz	V_{DD1} must be greater than V_{DDQ}—200mV
Tx and Tz	V_{REF} must always be less than all other supply voltages

The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

3.3.2.1 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

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3.3 Power-up, Initialization, and Power-off (cont'd)

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 7 — Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

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3.4 Mode Register Definition

3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM

Table 8 shows the mode registers for LPDDR3 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 8 — Mode Register Assignment in LPDDR3 SDRAM

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00_H	Device Info.	R	RL3	WL (Set B)	(RFU)	RZQI (optional)		(RFU)		DAI	go to MR0
1	01_H	Device Feature 1	W	*n*WR (for AP)			(RFU)		BL			go to MR1
2	02_H	Device Feature 2	W	WR Lev	WL Select	(RFU)	*n*WRE	RL & WL				go to MR2
3	03_H	I/O Config-1	W	(RFU)				DS				go to MR3
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			go to MR4
5	05_H	Basic Config-1	R	LPDDR3 Manufacturer ID								go to MR5
6	06_H	Basic Config-2	R	Revision ID1								go to MR6
7	07_H	Basic Config-3	R	Revision ID2								go to MR7
8	08_H	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09_H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	$0A_H$	IO Calibration	W	Calibration Code								go to MR10
11	$0B_H$	ODT Feature		(RFU)					PD CTL	DQ ODT		go to MR11
12:15	$0C_H$~$0F_H$	(reserved)		(RFU)								go to MR12
16	10_H	PASR_Bank	W	PASR Bank Mask								go to MR16
17	11_H	PASR_Seg	W	PASR Segment Mask								go to MR17
18-31	12_H-$1F_H$	(Reserved)		(RFU)								go to MR18
32	20_H	DQ Calibration Pattern A	R	See "DQ Calibration" on page 61								go to MR32
33:39	21_H~27_H	(Do Not Use)										go to MR33
40	28_H	DQ Calibration Pattern B	R	See "DQ Calibration" on page 61								go to MR40
41	29_H	CA Training 1	W	See "Mode Register Write - CA Training Mode" on page 66								go to MR41
42	$2A_H$	CA Training 2	W	See "Mode Register Write - CA Training Mode" on page 66								go to MR42
43:47	$2B_H$~$2F_H$	(Do Not Use)										go to MR43
48	30_H	CA Training 3	W	See "Mode Register Write - CA Training Mode" on page 66								go to MR48
49:62	31_H~$3E_H$	(Reserved)		(RFU)								go to MR49
63	$3F_H$	Reset	W	X								go to MR63
64:255	40_H~FF_H	(Reserved)		(RFU)								go to MR64

NOTE 1 RFU bits shall be set to '0' during mode register writes.
NOTE 2 RFU bits shall be read as '0' during mode register reads.
NOTE 3 All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
NOTE 4 All mode registers that are specified as RFU shall not be written.
NOTE 5 See vendor device datasheets for details on vendor-specific mode registers.
NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR0_Device Information (MA<7:0> = 00_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI (optional)		**(RFU)**		**DAI**

DAI (Device Auto-Initialization Status)	Read-only	OP<0>	**0_B:** DAI complete **1_B:** DAI still in progress	
RZQI (Built in Self Test for RZQ Information)	Read-only	OP<4:3>	**00_B:** RZQ self test not supported **01_B:** ZQ-pin may connect to V_{DDCA} or float **10_B:** ZQ-pin may short to GND **11_B:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{DDCA} or float nor short to GND)	1-4
WL (Set B) Support	Read-only	OP<6>	**0_B**: DRAM does not support WL (Set B) **1_B**: DRAM supports WL (SetB)	WL (Set B) Option Support
RL3 Option Support	Read-only	OP<7>	**0_B**: DRAM does not support RL=3, nWR=3, WL=1 **1_B**: DRAM supports RL=3, nWR=3, WL=1 for frequencies ≤ 166	RL3 Option Support

NOTE 1 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.

NOTE 2 If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR3 device will default to factory trim settings for R_{ON}, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

NOTE 4 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-Ω ±1%).

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR1_Device Feature 1 (MA<7:0> = 01_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
*n*WR (for AP)			(RFU)		BL		

BL	**Write-only**	**OP<2:0>**	**011_B:** BL8 (default) All others: reserved	
***n*WR**	**Write-only**	**OP<7:5>**	If *n*WRE (MR2 OP<4>) = 0: **001_B**: *n*WR=3 (optional) **100_B**: *n*WR=6 **110_B**: *n*WR=8 **111_B**: *n*WR=9 If *n*WRE (MR2 OP<4>) = 1: **000_B**: *n*WR=10 (default) **001_B**: *n*WR=11 **010_B**: *n*WR=12 **100_B**: *n*WR=14 **110_B**: *n*WR=16 All others: reserved	**1**

NOTE 1 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table 9 — Burst Sequence

C2	C1	C0	BL	Burst Cycle Number and Burst Address Sequence							
				1	2	3	4	5	6	7	8
0_B	0_B	0_B	8	0	1	2	3	4	5	6	7
0_B	1_B	0_B		2	3	4	5	6	7	0	1
1_B	0_B	0_B		4	5	6	7	0	1	2	3
1_B	1_B	0_B		6	7	0	1	2	3	4	5

1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2 - C0.

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR2_Device Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	*n*WRE	RL & WL			

RL & WL	Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) **0001_B**: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) **0100_B**: RL = 6 / WL = 3 (≤ 400 MHz) **0110_B**: RL = 8 / WL = 4 (≤ 533 MHz) **0111_B**: RL = 9 / WL = 5 (≤ 600 MHz) **1000_B**: RL = 10 / WL = 6 (≤ 667 MHz, default) **1001_B**: RL = 11 / WL = 6 (≤ 733 MHz) **1010_B**: RL = 12 / WL = 6 (≤ 800 MHz) **1100_B**: RL = 14 / WL = 8 (≤ 933 MHz) **1110_B**: RL = 16 / WL = 8 (≤ 1066 MHz) All others: reserved If OP<6> =1 (WL Set B, optional[2]) **0001_B**: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) **0100_B**: RL = 6 / WL = 3 (≤ 400 MHz) **0110_B**: RL = 8 / WL = 4 (≤ 533 MHz) **0111_B**: RL = 9 / WL = 5 (≤ 600 MHz) **1000_B**: RL = 10 / WL = 8 (≤ 667 MHz, default) **1001_B**: RL = 11 / WL = 9 (≤ 733 MHz) **1010_B**: RL = 12 / WL = 9 (≤ 800 MHz) **1100_B**: RL = 14 / WL = 11 (≤ 933 MHz) **1110_B**: RL = 16 / WL = 13 (≤ 1066 MHz) All others: reserved	
*n*WRE	Write-only	OP<4>	**0_B:** enable *n*WR programming ≤ 9 **1_B:** enable *n*WR programming > 9 (default)	
WL Select	Write-only	OP<6>	**0_B:** Select WL Set A (default) **1_B:** Select WL Set B (optional[2])	
WR Leveling	Write-only	OP<7>	**0_B:** disabled (default) **1_B:** enabled	

NOTE 1 See MR0, OP<7>
NOTE 2 See MR0, OP<6>

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0001_B:** 34.3Ω typical pull-down/pull-up **0010_B:** 40Ω typical pull-down/pull-up (default) **0011_B:** 48Ω typical pull-down/pull-up **0100_B:** reserved for 60Ω typical pull-down/pull-up **0110_B:** reserved for 80Ω typical pull-down/pull-up **1001_B:** 34.3Ω typical pull-down, 40Ω typical pull-up **1010_B:** 40Ω typical pull-down, 48Ω typical pull-up **1011_B:** 34.3Ω typical pull-down, 48Ω typical pull-up **All others:** reserved	

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate, Refresh Multiplier (RM)	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** RM = 4; t_{REFIM} = 4 x t_{REFI}, $t_{REFIMpb}$ = 4 x t_{REFIpb}, t_{REFWM} = 4 x t_{REFW}**010_B:** RM = 2; t_{REFIM} = 2 x t_{REFI}, $t_{REFIMpb}$ = 2 x t_{REFIpb}, t_{REFWM} = 2 x t_{REFW} **011_B:** RM = 1; t_{REFIM} = t_{REFI}, $t_{REFIMpb}$ = t_{REFIpb}, t_{REFWM} = t_{REFW}(<=85°C) **100_B:** RM = 0.5; t_{REFIM} = 0.5 x t_{REFI}, $t_{REFIMpb}$ = 0.5 x t_{REFIpb}, t_{REFWM} = 0.5 x t_{REFW}, do not de-rate SDRAM AC timing **101_B:** RM = 0.25; t_{REFIM} = 0.25 x t_{REFI}, $t_{REFIMpb}$ = 0.25 x t_{REFIpb}, t_{REFWM} = 0.25 x t_{REFW}, do not de-rate SDRAM AC timing **110_B:** RM = 0.25; t_{REFIM} = 0.25 x t_{REFI}, $t_{REFIMpb}$ = 0.25 x t_{REFIpb}, t_{REFWM} = 0.25 x t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.

NOTE 2 OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85°C.

NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.

NOTE 5 SDRAM might not operate properly when OP[2:0] = 000_B or 111_B.

NOTE 6 For specified operating temperature range and maximum operating temperature refer to Table 31 on page 88.

NOTE 7 LPDDR3 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: t_{RCD}, t_{RC}, t_{RAS}, t_{RP}, and t_{RRD}. t_{DQSCK} shall be de-rated according to the t_{DQSCK} de-rating in Table 64 on page 123. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 8 See "Temperature Sensor" on page 59 for information on the recommended frequency of reading MR4.

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR3 Manufacturer ID							

LPDDR3 Manufacturer ID	Read-only	OP<7:0>	See JESD-TBD LPDDR3 Manufacturer ID encodings	

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**00000000_B:** A-version	

NOTE 1 MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**00000000_B:** A-version	

NOTE 1 MR7 is vendor specific.

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR8_Basic Configuration 4 (MA<7:0> = $08B_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**11_B:** S8 SDRAM **all others:** Reserved	
Density	Read-only	OP<5:2>	**0100_B:** 1Gb **0101_B:** 2Gb **0110_B:** 4Gb **1110_B:** 6Gb **0111_B:** 8Gb **1101_B:** 12Gb **1000_B:** 16Gb **1001_B:** 32Gb **all others:** reserved	
I/O width	Read-only	OP<7:6>	**00_B:** x32 **01_B:** x16 **all others:** reserved	

MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
vendor-specific test mode							

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved

NOTE 1 Host processor shall not write MR10 with "Reserved" values

NOTE 2 LPDDR3 devices shall ignore calibration command when a "Reserved" value is written into MR10.

NOTE 3 See AC timing table for the calibration latency.

NOTE 4 If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command" on page 64) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

NOTE 5 LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.

NOTE 6 Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR11_ODT Control (MA<7:0> = $0B_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					PD CTL	DQ ODT	

DQ ODT	Write-only	OP<1:0>	**00_B:** Disable (Default) **01_B:** $R_{ZQ}/4$ (see Note 1) **10_B:** $R_{ZQ}/2$ **11_B:** $R_{ZQ}/1$	
PD Control	Write-only	OP<2>	**0_B:** ODT disabled by DRAM during power down (default) **1_B:** ODT enabled by DRAM during power down	

NOTE 1 $R_{ZQ}/4$ shall be supported for LPDDR3-1866 and LPDDR3-2133 devices. $R_{ZQ}/4$ support is optional for LPDDR3-1333 and LPDDR3-1600 devices. Consult manufacturer specifications for $R_{ZQ}/4$ support for LPDDR3-1333 and LPDDR3-1600.

MR12:15_(Reserved) (MA<7:0> = $0C_H$-$0F_H$):

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

Bank <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the bank (= unmasked, default) **1_B:** refresh blocked (= masked)	1

OP	Bank Mask	8-Bank SDRAM
0	XXXXXXX1	**Bank 0**
1	XXXXXX1X	**Bank 1**
2	XXXXX1XX	**Bank 2**
3	XXXX1XXX	**Bank 3**
4	XXX1XXXX	**Bank 4**
5	XX1XXXXX	**Bank 5**
6	X1XXXXXX	**Bank 6**
7	1XXXXXXX	**Bank 7**

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR17_PASR_Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the segment (=unmasked, default) **1_B:** refresh blocked (=masked)	

Segment	OP	Segment Mask	1Gb	2Gb	4Gb	6Gb[2]	8Gb	12Gb[2]	16Gb	32Gb
			R12:10	R13:11	R13:11	R14:12	R14:12	R14:12	R14:12	TBD
0	0	XXXXXXX1	**000_B**							
1	1	XXXXXX1X	**001_B**							
2	2	XXXXX1XX	**010_B**							
3	3	XXXX1XXX	**011_B**							
4	4	XXX1XXXX	**100_B**							
5	5	XX1XXXXX	**101_B**							
6	6	X1XXXXXX	**110_B**							
7	7	1XXXXXXX	**111_B**							

NOTE 1 This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

NOTE 2 No memory present at addresses with R13=R14=HIGH. Segment masks 6 and 7 are ignored.

MR18-31_Reserved (MA<7:0> = 012_H - $01F_H$):

MR32_DQ Calibration Pattern A (MA<7:0> = 20_H):

Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on page 61.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0> = 28_H):

Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on page 61.

MR41_CA Training_1 (MA<7:0> = 29_H):

Writes to MR41 enables CA Training. See Mode Register Write - CA Training Mode on page 66

MR42_CA Training_2 (MA<7:0> = $2A_H$):

Writes to MR42 exits CA Training. See Mode Register Write - CA Training Mode on page 66.

MR43:47_(Do Not Use) (MA<7:0> = $2B_H$-$2F_H$):

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3.4.1 Mode Register Assignment and Definition in LPDDR3 SDRAM (cont'd)

MR48_CA_Training_3 (MA<7:0> = 30_H):

Writes to MR48 enables CA Training. See Mode Register Write - CA Training Mode on page 66.

MR49:62_(Reserved) (MA<7:0>=31_H-$3E_H$:

MR63_Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X or 0xFC[1]							

NOTE 1 For additonal information on MRW RESET see "Mode Register Write" on page 62.

MR64:255_(Reserved) (MA<7:0> = 40_H-FF_H):

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4 LPDDR3 Command Definitions and Timing Diagrams

4.1 Activate Command

The ACTIVATE command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 to BA2 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at t_{RCD} after the ACTIVATE command is issued. After a bank has been activated it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between ACTIVATE commands to different banks is t_{RRD} (see Figure 1).

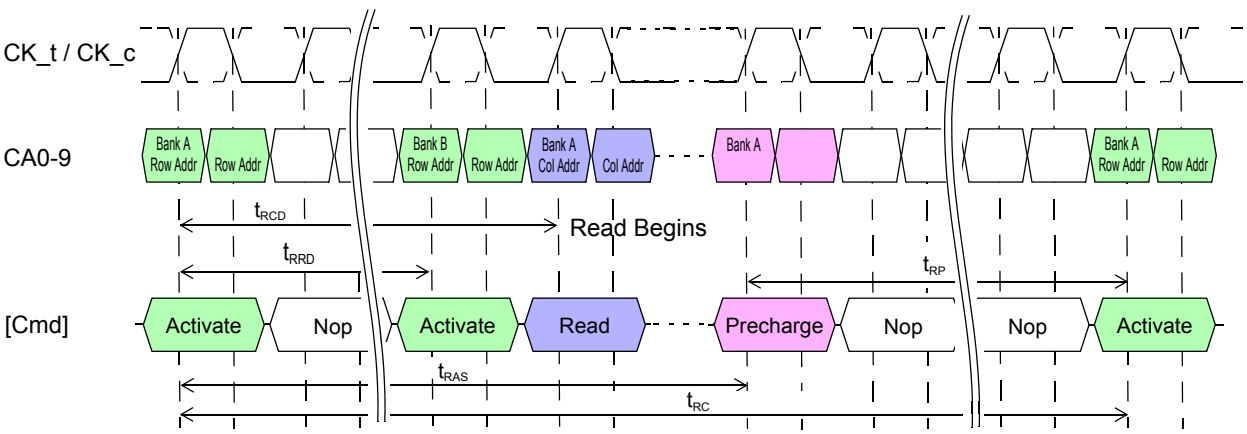

Figure 3 — ACTIVATE Command

3. A PRECHARGE-all command uses t_{RPab} timing, while a single-bank PRECHARGE command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE.

4.1.1 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR3 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

The 8-Bank Device Sequential Bank Activation Restriction: No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling t_{FAW} window. The number of clocks in a t_{FAW} period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting to clocks is done by dividing t_{FAW}[ns] by t_{CK}[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(t_{FAW}/t_{CK}) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock $n + 1$ and $n + 9$. REFpb also counts as bank activation for purposes of t_{FAW}. If the clock frequency is changed during the t_{FAW} period, the rolling t_{FAW} window may be calculated in clock cycles by adding up the time spent in each clock period. The t_{FAW} requirement is met when the previous n clock cycles exceeds the t_{FAW} time.

The 8-Bank Device Precharge-All Allowance: t_{RP} for a PRECHRGE ALL command must equal t_{RPab}, which is greater than t_{RPpb}.

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4.1 Activate Command (cont'd)

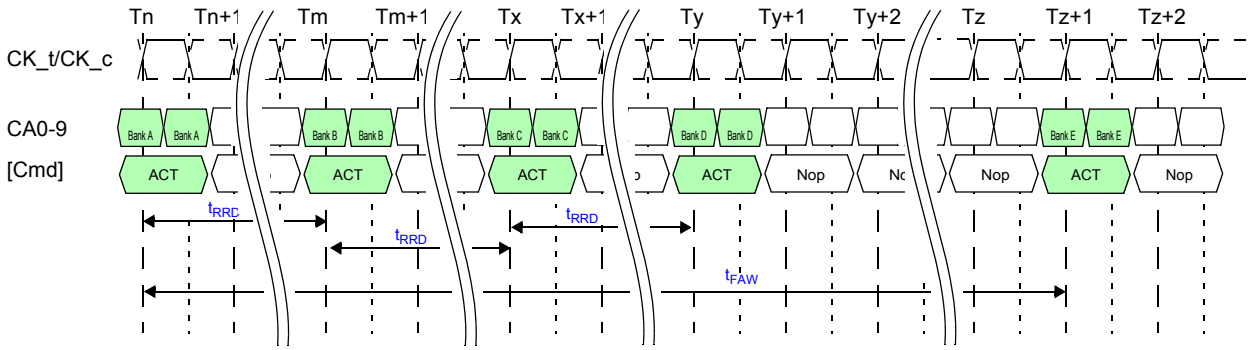
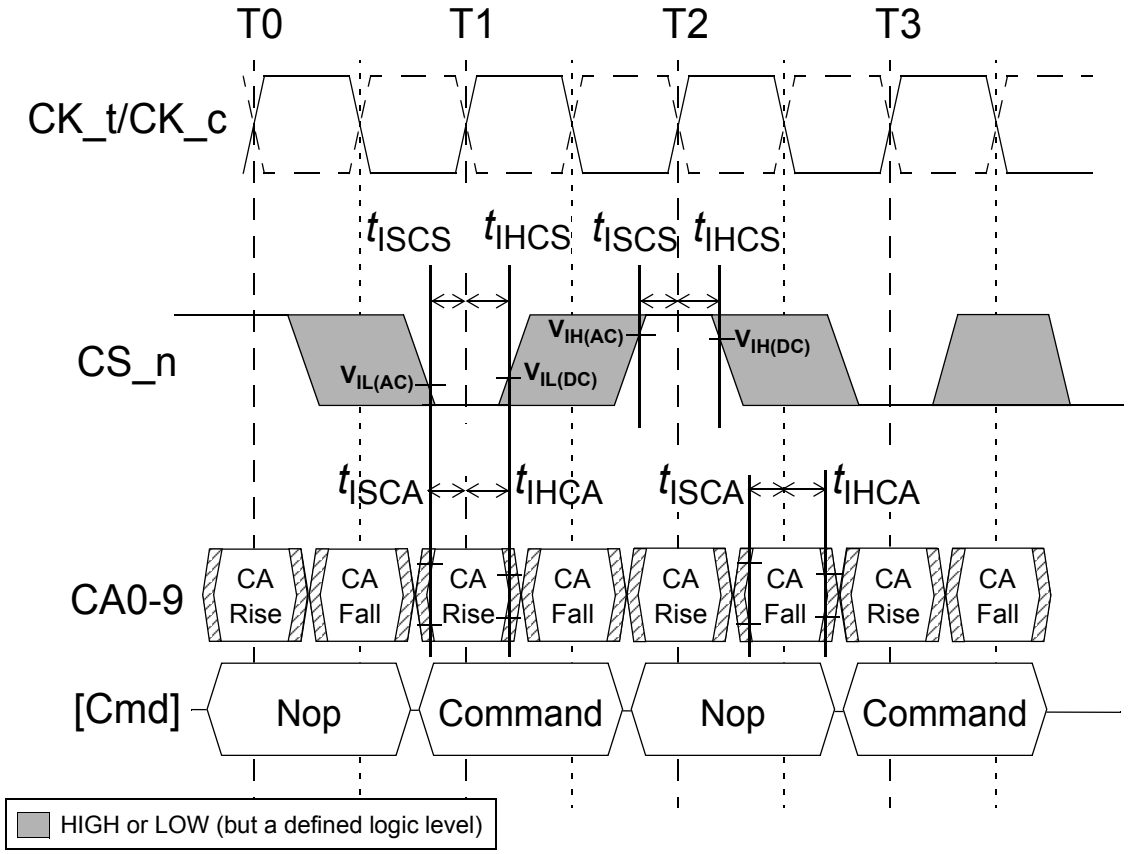


Figure 4 — LPDDR3 t_{FAW} Timing

4.2 LPDDR3 Command Input Signal Timing Definition



NOTE Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 5 — LPDDR3: Command Input Setup and Hold Timing

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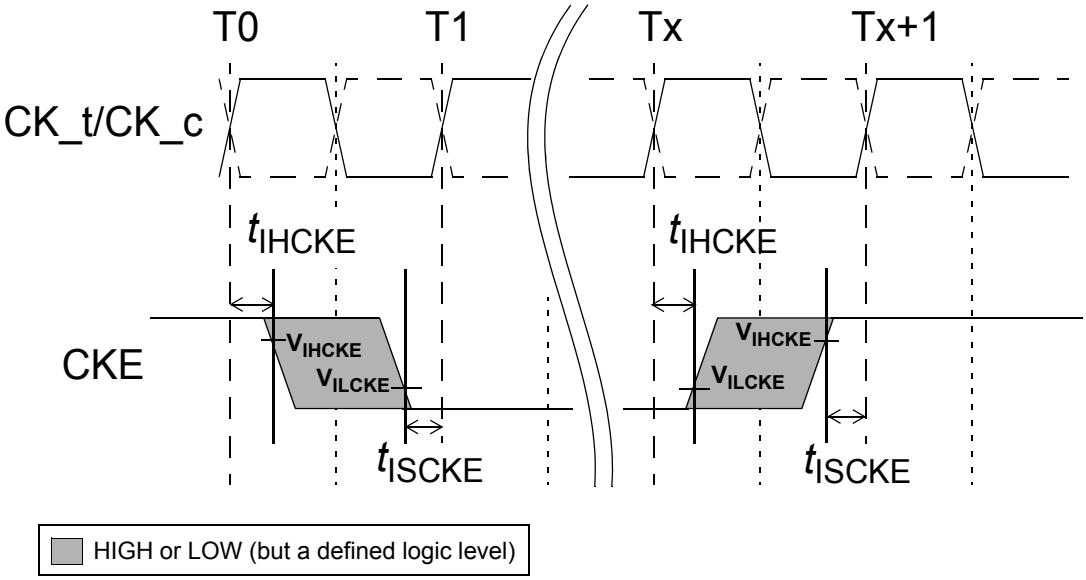
4.2.1 LPDDR3 CKE Input Setup and Hold Timing



NOTE 1: After CKE is registered LOW, CKE signal level shall be maintained below V_{ILCKE} for t_{CKE} specification (LOW pulse width).
NOTE 2: After CKE is registered HIGH, CKE signal level shall be maintained above V_{IHCKE} for t_{CKE} specification (HIGH pulse width).

Figure 6 — LPDDR3: Command Input Setup and Hold Timing

4.3 Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR3 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles. Burst interrupts are not allowed.

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4.4 Burst Read Operation

The burst READ command is initiated with CS_n LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs CA5r–CA6r and CA1f–CA9f determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid data is available RL × t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW ^{t}RPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

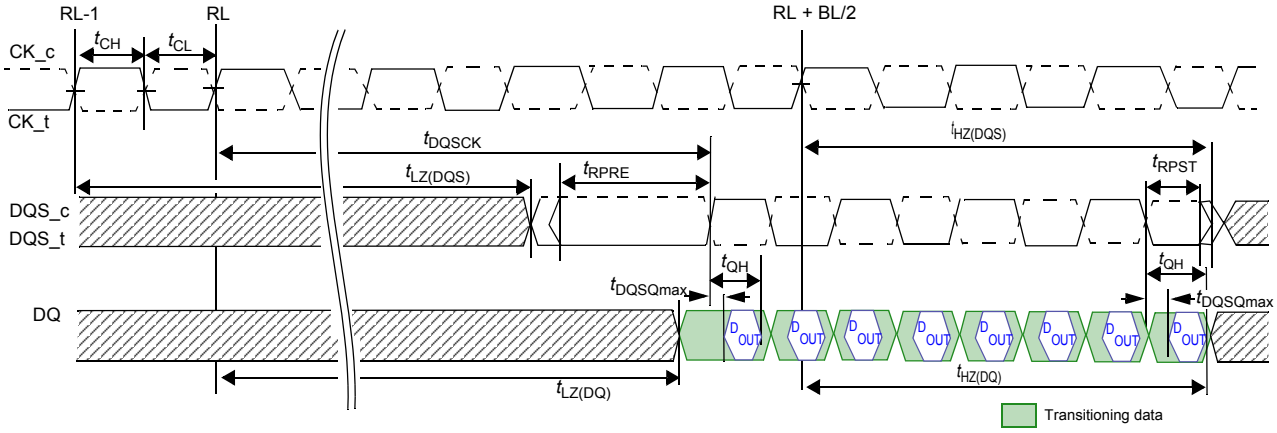

Figure 7 — Read Output Timing

NOTE 1 t_{DQSCK} can span multiple clock periods.

NOTE 2 An effective burst length of 8 is shown.

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4.4 Burst Read Operation (cont'd)

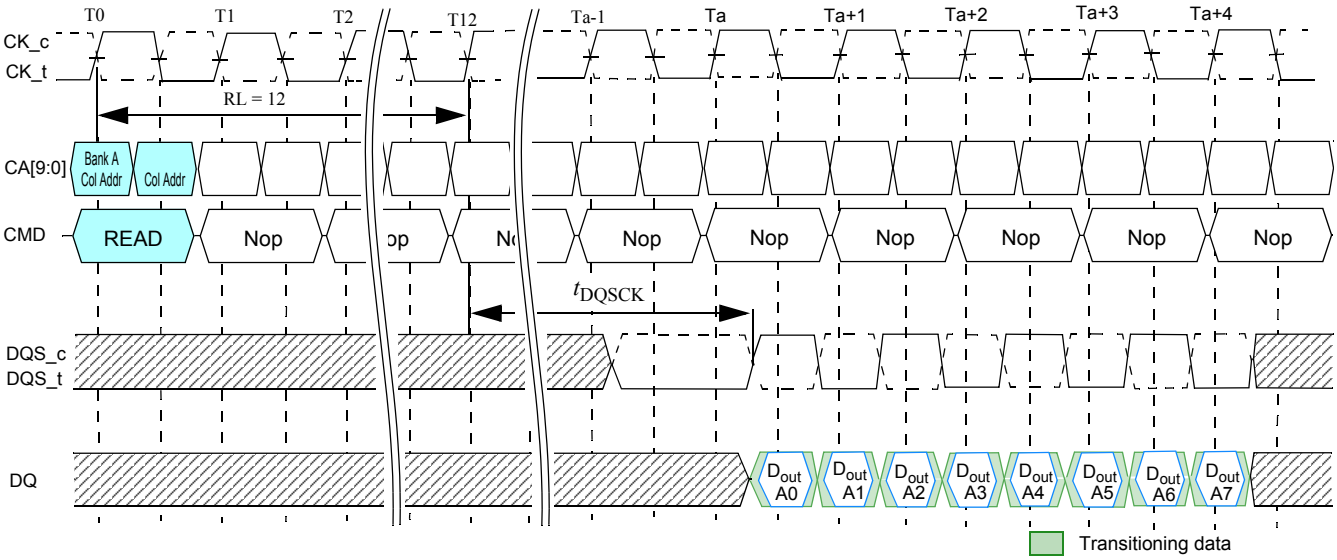

Figure 8 — Burst Read: RL = 12, BL = 8, $t_{DQSCK} > t_{CK}$

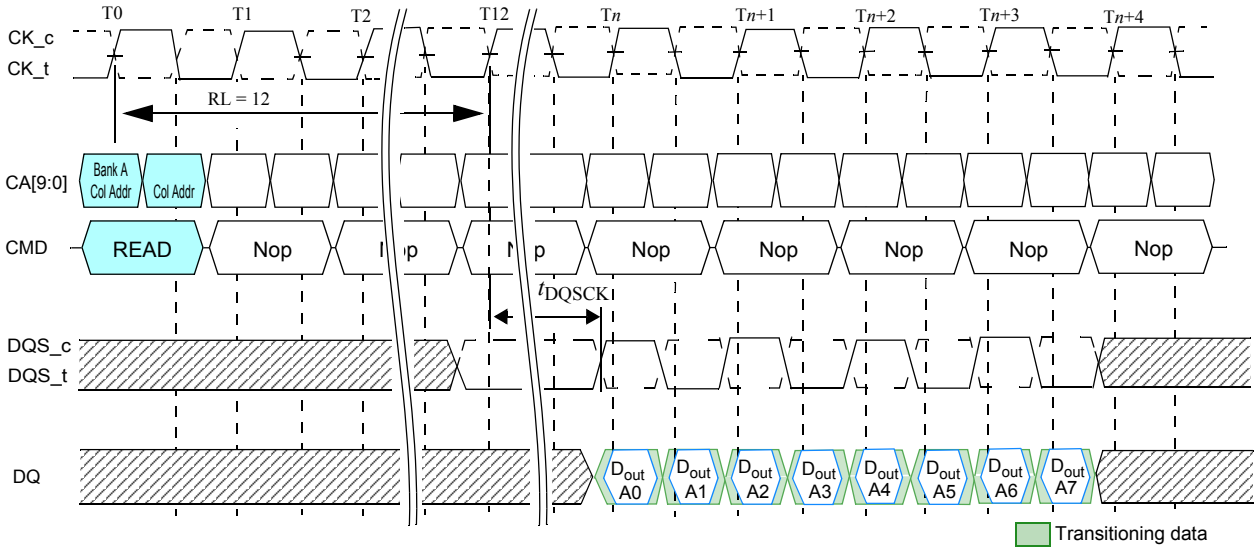

Figure 9 — Burst Read: RL = 12, BL = 8, $t_{DQSCK} < t_{CK}$

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4.4 Burst Read Operation (cont'd)

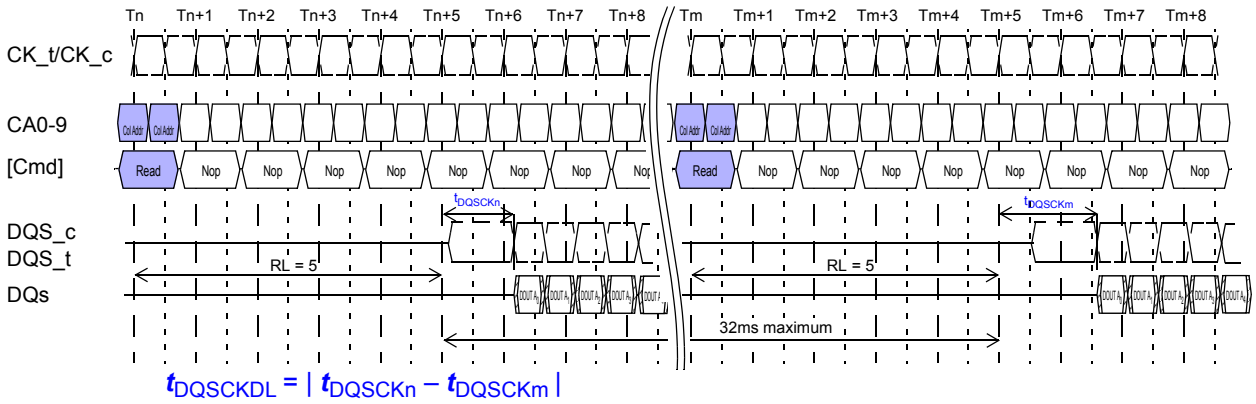

Figure 10 — LPDDR3: $t_{DQSCKDL}$ timing

NOTE 1 $t_{DQSCKDLmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair within any 32ms rolling window.

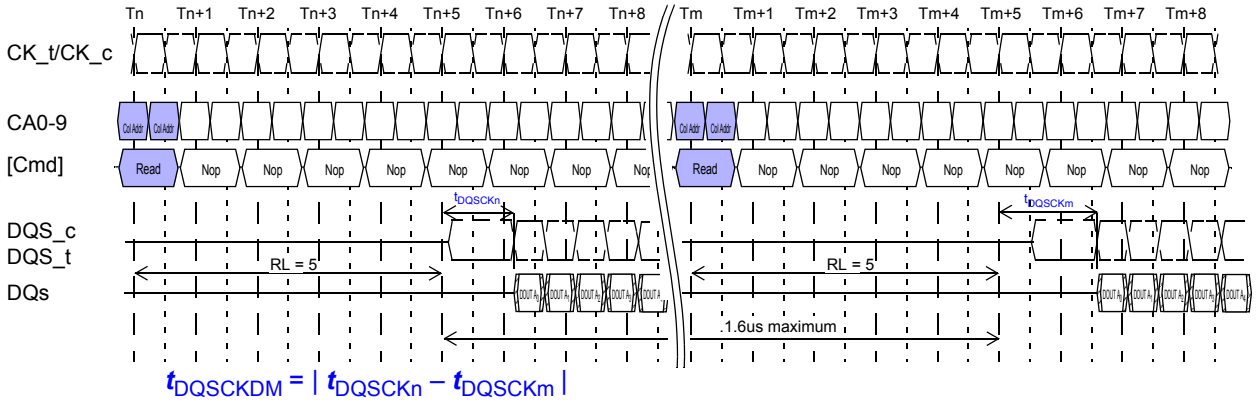

Figure 11 — LPDDR3: $t_{DQSCKDM}$ timing

NOTE 1 $t_{DQSCKDMmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair within any 1.6us rolling window.

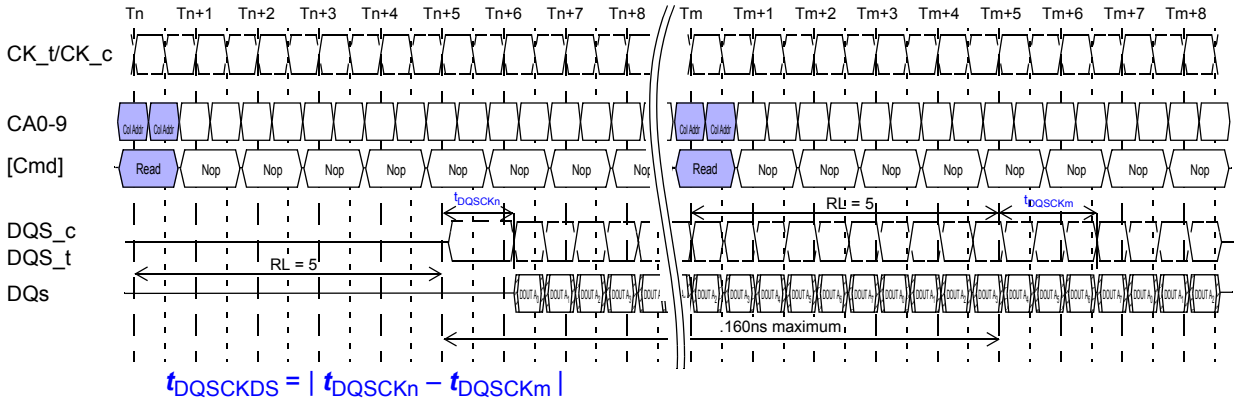

Figure 12 — LPDDR3: $t_{DQSCKDS}$ timing

NOTE 1 $t_{DQSCKDSmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair for reads within a consecutive burst within any 160ns rolling window.

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