JEDEC STANDARD

Addendum No. 1 to JESD209-4 - Low Power Double Data Rate 4X (LPDDR4X)

JESD209-4-1

JANUARY 2017

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2017
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

Addendum No. 1 to JESD209-4 - LOW POWER DOUBLE DATA RATE 4X (LPDDR4X)

Contents

1 Scope 1
2 Package ballout and Pin Definition 2
2.1 Pad Order 2
2.2 Single Channel Pad Order 3
2.3 LPDDR4X packages 4
2.3.1 LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch) – Using MO-317A 4
2.3.2 144 ball ePoP MCP One-Channel FBGA (top view) using MO-323A 5
2.3.3 200-ball x32 Discrete Package, 0.80 mm x 0.65 mm using MO-311 6
2.3.4 432-ball x64 HDI Discrete Package, 0.50 mm x 0.50 mm (MO-313) 7
2.3.5 254 ball *e*•MMC MCP Two-Channel FBGA (top view) using MO-276 10
2.3.6 254 ball UFS MCP Two-Channel FBGA (top view) using MO-276 11
2.3.7 254 ball *e*•MMC MCP One Channel FBGA (top view) using MO-276 10
2.4 Pad Definition and Description 13
2.5 Mode Register Definition 14
3 Command Definitions and Timing Diagrams 23
3.1 Pull Up/Pull Down Driver Characteristics and Calibration 23
3.2 ODT Mode Register and ODT Characteristics 23
3.3 On Die Termination for DQ, DQS and DMI 25
3.4 Output Driver and Termination Register Temperature and Voltage Sensitivity 27
4 AC and DC Operating Conditions 28
4.1 Recommended DC Operating Conditions for low voltage 28
4.2 Single Ended Output Slew Rate 28
4.3 Differential Output Slew Rate 29
5 V_{REF} Specifications 30
5.1 CA Internal V_{REF} Specifications 30
5.2 DQ Internal V_{REF} Specifications 30
6 Power-up, Initialization and Power-off Procedure 30
7 ODT Mode Register and ODT State Table 33
8 Core Timing 34

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

Contents (cont'd)

Tables

Table 1 Pad Definition and Description 13
Table 2 Mode Register Assignment in LPDDR4 SDRAM 14
Table 3 V_{REF} Settings for Range[0] and Range[1] 18
Table 4 V_{REF} Settings for Range[0] and Range[1] 20
Table 5 LPDDR4X Byte Mode Device (MR11 OP[6:4] ≠ 000B Case) 22
Table 6 Pull-down Driver Characteristics, with ZQ Calibration 23
Table 7 Terminated Pull-Up Characteristics, with ZQ Calibration 23
Table 8 Terminated Valid Calibration Points 23
Table 9 ODT DC Electrical Characteristics, assuming RZQ = 240 Ω +/-1% over the entire operating temperature range after a proper ZQ calibration. 24
Table 10 ODT DC Electrical Characteristics, assuming RZQ = 240 Ω +/-1% over the entire operating temperature range after a proper ZQ calibration. 26
Table 11 Output Driver and Termination Register Sensitivity Definition 27
Table 12 Output Driver and Termination Register Temperature and Voltage Sensitivity 27
Table 13 Recommended DC Operating Conditions 28
Table 14 Output Slew Rate (single-ended) for 0.6 V V_{DDQ} 28
Table 15 Differential Output Slew Rate for 0.6 V V_{DDQ} 29
Table 16 CA Internal V_{REF} Specifications 30
Table 17 DQ Internal V_{REF} Specifications 29
Table 18 MRS defaults settings 30
Table 19 Command Bus ODT State 33
Table 20 Core Timing 34

Figures

Figure 1 On Die Termination for CA 23
Figure 2 On Die Termination 25
Figure 3 Single Ended Output Slew Rate Definition 28
Figure 4 Differential Output Slew Rate Definition 29

Documents
Document Sharing Hub
Full document details: JEDEC JESD209-4-1 2017

Addendum No. 1 to JESD209-4 - LOW POWER DOUBLE DATA RATE 4X (LPDDR4X)

(From JEDEC Board Ballot JCB-16-49, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This document defines the LPDDR4 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit per channel SDRAM device with either one or two channels. LPDDR4 dual channel device density ranges from 4 Gb through 32 Gb and single channel density ranges from 2 Gb through 16 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) and LPDDR3 (JESD209-3).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR4 standard.

This addendum defines LPDDR4X specifications that supersede the LPDDR4 Standard (JESD209-4) to enable low V_{DDQ} operation of LPDDR4X devices to reduce power consumption.

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

2 Package Ballout and Pin Definition

2.1 Pad Order

Ch. A Top					
1	VDD2	41	VDD2	101	VDD2
2	VSS	42	CKE_A	102	VSS
3	VDD1	43	CS_A	103	VDD1
4	VDD2	44	VSS	104	VDD2
5	VSS	45	CA1_A	105	VSS
6	VSSQ	46	CA0_A	106	VSSQ
7	DQ8_A	47	VDD2	107	DQ8_B
8	VDDQ	48	ODT(ca)_A	108	VDDQ
9	DQ9_A	49	VSS	109	DQ9_B
10	VSSQ	50	VDD1	110	VSSQ
11	DQ10_A	51	VSSQ	111	DQ10_B
12	VDDQ	52	DQ7_A	112	VDDQ
13	DQ11_A	53	VDDQ	113	DQ11_B
14	VSSQ	54	DQ6_A	114	VSSQ
15	DQS1_t_A	55	VSSQ	115	DQS1_t_B
16	DQS1_c_A	56	DQ5_A	116	DQS1_c_B
17	VDDQ	57	VDDQ	117	VDDQ
18	DMI1_A	58	DQ4_A	118	DMI1_B
19	VSSQ	59	VSSQ	119	VSSQ
20	DQ12_A	60	DMI0_A	120	DQ12_B
21	VDDQ	61	VDDQ	121	VDDQ
22	DQ13_A	62	DQS0_c_A	122	DQ13_B
23	VSSQ	63	DQS0_t_A	123	VSSQ
24	DQ14_A	64	VSSQ	124	DQ14_B
25	VDDQ	65	DQ3_A	125	VDDQ
26	DQ15_A	66	VDDQ	126	DQ15_B
27	VSSQ	67	DQ2_A	127	VSSQ
28	ZQ	68	VSSQ	128	RESET_n
29	VDDQ	69	DQ1_A	129	VDDQ
30	VDD2	70	VDDQ	130	VDD2
31	VDD1	71	DQ0_A	131	VDD1
32	VSS	72	VSSQ	132	VSS
33	CA5_A	73	VSS	133	CA5_B
34	CA4_A	74	VDD2	134	CA4_B
35	VDD2	75	VDD1	135	VDD2
36	CA3_A	76	VSS	136	CA3_B
37	CA2_A	77	VDD2	137	CA2_B
38	VSS	Ch. A Bottom		138	VSS
39	CK_c_A			139	CK_c_B
40	CK_t_A			140	CK_t_B
Ch. A Top				Ch. B Top	

Ch. B Top			
141	VDD2		
142	CKE_B		
143	CS_B		
144	VSS		
145	CA1_B		
146	CA0_B		
147	VDD2		
148	ODT(ca)_B		
149	VSS		
150	VDD1		
151	VSSQ		
152	DQ7_B		
153	VDDQ		
154	DQ6_B		
155	VSSQ		
156	DQ5_B		
153	VDDQ		
158	DQ4_B		
159	VSSQ		
160	DMI0_B		
161	VDDQ		
162	DQS0_c_B		
163	DQS0_t_B		
164	VSSQ		
165	DQ3_B		
166	VDDQ		
167	DQ2_B		
168	VSSQ		
169	DQ1_B		
170	VDDQ		
171	DQ0_B		
172	VSSQ		
173	VSS		
174	VDD2		
175	VDD1		
176	VSS		
177	VDD2		
Ch. B Bottom			

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads (“DNU”), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 V_{DDQ} pads ((#12,#21,#57,#66,#112,#121,#157 and #166) may be individually assigned to either V_{DDQ} or V_{DD2}. Please refer to vendor specification.

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

2.2 Single Channel Pad Order

Top			
1	VDD2	40	CK_c
2	VSS	41	CK_t
3	VDD1	42	VDD2
4	VDD2	43	CKE
5	VSS	44	CS
6	VSSQ	45	VSS
7	DQ8	46	CA1
8	VDDQ	47	CA0
9	DQ9	48	VDD2
10	VSSQ	49	ODT(ca)
11	DQ10	50	VSS
12	VDDQ	51	VDD1
13	DQ11	52	VSSQ
14	VSSQ	53	DQ7
15	DQS1_t	54	VDDQ
16	DQS1_c	55	DQ6
17	VDDQ	56	VSSQ
18	DMI1	57	DQ5
19	VSSQ	58	VDDQ
20	DQ12	59	DQ4
21	VDDQ	60	VSSQ
22	DQ13	61	DMI0
23	VSSQ	62	VDDQ
24	DQ14	63	DQS0_c
25	VDDQ	64	DQS0_t
26	DQ15	65	VSSQ
27	VSSQ	66	DQ3
28	ZQ	67	VDDQ
29	VDDQ	68	DQ2
30	VDD2	69	VSSQ
31	RESET_n	70	DQ1
32	VDD1	71	VDDQ
33	VSS	72	DQ0
34	CA5	73	VSSQ
35	CA4	74	VSS
36	VDD2	75	VDD2
37	CA3	76	VDD1
38	CA2	77	VSS
39	VSS	78	VDD2
		Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 V_{DDQ} pads (#12, #21, #57 and #66) may be individually assigned to either V_{DDQ} or V_{DD2}. Please refer to vendor specification.

NOTE 4 A RESET_n pad is added. The RESET_n pad location is vendor specific. See vendor device datasheets for details about RESET_n pad location.

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

2.3 LPDDR4X packages

2.3.1 LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch) – Using MO-317A

LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	NC	VDD2	DQ3_A	VSS	DQ5_A	ODT(ca)_A	CA0_A	CS1_A	CKE1_A	CA2_A	VSS	VSS	DQ13_A	VDD2	VDD1	DQ10_A	ZQ1_A	ZQ1_D	DQ10_C	VDD1	VDD2	DQ13_C	VSS	VSS	CA2_C	CKE1_C	CS1_C	CA0_C	ODT(ca)_C	DQ5_C	VSS	DQ3_C	VDD2	NC	A
B	VSS	DQ2_A	VDDQ	DMI0_A	VDDQ	DQ7_A	VDD2	CS0_A	CKE0_A	VDD2	CA4_A	DQ15_A	VDDQ	DMI1_A	DQ11_A	VSS	ZQ0_A	ZQ0_D	VSS	DQ11_C	DMI1_C	VDDQ	DQ15_C	CA4_C	VDD2	CKE0_C	CS0_C	VDD2	DQ7_C	VDDQ	DMI0_C	VDDQ	DQ2_C	VSS	B
C	DQ0_A	VDDQ	VSS	VSS	DQ4_A	VDDQ	CA1_A	VDD2	VSS	CA3_A	VSS	VDDQ	DQ12_A	VSS	VDDQ	DQ9_A	RESET_n	RFU	DQ9_C	VDDQ	VSS	DQ12_C	VDDQ	VSS	CA3_C	VSS	VDD2	CA1_C	VDDQ	DQ4_C	VSS	VSS	VDDQ	DQ0_C	C
D	VDD1	DQ1_A	DQS0_t_A	DQS0_c_A	VSS	DQ6_A	VSS	CK_t_A	CK_c_A	VSS	CA5_A	DQ14_A	VSS	DQS1_c_A	DQS1_t_A	VDDQ	DQ8_A	DQ8_C	VDDQ	DQS1_t_C	DQS1_c_C	VSS	DQ14_C	CA5_C	VSS	CK_c_C	CK_t_C	VSS	DQ6_C	VSS	DQS0_c_C	DQS0_t_C	DQ1_C	VDD1	D
E	VDD2	VSS																															VSS	VDD2	E
F	VDD2	VDD2																															VDD2	VDD2	F
G	VSS	VSS																															VSS	VSS	G
H	RFU	RFU																															RFU	RFU	H
J	RFU	RFU																															RFU	RFU	J
K	RFU	RFU																															RFU	RFU	K
L	RFU	RFU																															RFU	RFU	L
M	RFU	RFU																															RFU	RFU	M
N	RFU	RFU																															RFU	RFU	N
P	RFU	RFU																															RFU	RFU	P
R	RFU	RFU																															RFU	RFU	R
T	RFU	RFU																															RFU	RFU	T
U	RFU	RFU																															RFU	RFU	U
V	RFU	RFU																															RFU	RFU	V
W	RFU	RFU																															RFU	RFU	W
Y	RFU	RFU																															RFU	RFU	Y
AA	RFU	RFU																															RFU	RFU	AA
AB	RFU	RFU																															RFU	RFU	AB
AC	RFU	RFU																															RFU	RFU	AC
AD	RFU	RFU																															RFU	RFU	AD
AE	RFU	RFU																															RFU	RFU	AE
AF	RFU	RFU																															RFU	RFU	AF
AG	RFU	RFU																															RFU	RFU	AG
AH	VSS	VSS																															VSS	VSS	AH
AJ	VDD2	VDD2																															VDD2	VDD2	AJ
AK	VDD2	VSS																															VSS	VDD2	AK
AL	VDD1	DQ1_B	DQS0_t_B	DQS0_c_B	VSS	DQ6_B	VSS	CK_t_B	CK_c_B	VSS	CA5_B	DQ14_B	VSS	DQS1_c_B	DQS1_t_B	VDDQ	DQ8_B	DQ8_D	VDDQ	DQS1_t_D	DQS1_c_D	VSS	DQ14_D	CA5_D	VSS	CK_c_D	CK_t_D	VSS	DQ6_D	VSS	DQS0_c_D	DQS0_t_D	DQ1_D	VDD1	AL
AM	DQ0_B	VDDQ	VSS	VSS	DQ4_B	VDDQ	CA1_B	VDD2	VSS	CA3_B	VSS	VDDQ	DQ12_B	VSS	VDDQ	DQ9_B	VDD2	VDD2	DQ9_D	VDDQ	VSS	DQ12_D	VDDQ	VSS	CA3_D	VSS	VDD2	CA1_D	VDDQ	DQ4_D	VSS	VSS	VDDQ	DQ0_D	AM
AN	VSS	DQ2_B	VDDQ	DMI0_B	VDDQ	DQ7_B	VDD2	CS0_B	CKE0_B	VDD2	CA4_B	DQ15_B	VDDQ	DMI1_B	DQ11_B	VSS	RFU	RFU	VSS	DQ11_D	DMI1_D	VDDQ	DQ15_D	CA4_D	VDD2	CKE0_D	CS0_D	VDD2	DQ7_D	VDDQ	DMI0_D	VDDQ	DQ2_D	VSS	AN
AP	NC	VDD2	DQ3_B	VSS	DQ5_B	ODT(ca)_B	CA0_B	CS1_B	CKE1_B	CA2_B	VSS	VSS	DQ13_B	VDD2	VDD1	DQ10_B	RFU	RFU	DQ10_D	VDD1	VDD2	DQ13_D	VSS	VSS	CA2_D	CKE1_D	CS1_D	CA0_D	ODT(ca)_D	DQ5_D	VSS	DQ3_D	VDD2	NC	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

NOTE 1 14 mm x 14 mm, 0.4 mm pitch.
NOTE 2 376 ball count, 34 rows.
NOTE 3 Top View, A1 in top left corner.
NOTE 4 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.
NOTE 5 Package Channel a and Channel d shall be assigned to die Channel A of different LPDDR4 die.
NOTE 6 DRAM die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.
NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

Documents
Document Sharing Hub
Full document details: JEDEC JESD209-4-1 2017

2.3.2 144 ball ePoP MCP One-Channel FBGA (top view) using MO-323A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	DNU	VSSm	VSSm	VCCQm	VSSm	VSSm	DAT5m	VCCQm	DAT0m	CLKm	VCCm	DAT6m	VCCQm	DAT7m	VCCQm	VSSm	RSTm	VSSm	DNU
B	VSSm	VSSm	VCCm	VSSm	VDDI	VCCm	DAT1m	DAT4m	VSSm	VCCQm	VSSm	DAT2m	DAT3m	VSSm	DSm	VSSm	CMDm	VCCm	VSSm
C	VSSm	VCCm																VSSm	VSSm
D	VSF1	VSF3																VSF5	VSF8
E	VSF2	VSF4																VSF6	VSF9
F	RESET_n	VSS																VSF7	RFU
G	ZQ1_A	ZQ0_A																RFU	RFU
H	VSS	VSS																VSS	VSS
J	VDD1	VDD1																VDD1	VDD1
K	VDD2	VDD2																VDD2	VDD2
L	VSS	VDDQ								eMCP 144FBGA 19x21								VDDQ	VSS
M	DQ8_A	DQ9_A																DQ1_A	DQ0_A
N	VDD2	DQ10_A																DQ2_A	VDD2
P	DQ11_A	VSS																VSS	DQ3_A
R	DQS1_t_A	DQS1_c_A																DQS0_c_A	DQS0_t_A
T	VSS	VDDQ																VDDQ	VSS
U	DM1_A	VSS																VSS	DM0_A
V	VDD2	VDDQ																VDDQ	VDD2
W	DQ12_A	DQ13_A																DQ5_A	DQ4_A
Y	VSS	VDD2	DQ14_A	VDD1	CA5_A	VSS	CA2_A	VDD2	CK_c_A	VSS	CKE0_A	CS0_A	CA1_A	VDD2	VSS	DQ7_A	DQ6_A	VDD2	VSS
AA	DNU	VSS	VDDQ	DQ15_A	VDD2	CA4_A	CA3_A	VSS	CK_t_A	CKE1_A	CS1_A	VSS	CA0_A	ODT(ca)_A	VDD1	VDDQ	VSS	VSS	DNU

eMMC	VCCm
	VCCQm
	VSSm
DRAM	VDDQ
	VDD1
	VDD2
	VSS

NOTE 1 0.4 mm pitch, 2 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 Body size: 8 mm x 9.5 mm

NOTE 4 ODT(ca)_A balls are wired to ODT(ca)_A pads of Rank 0 DRAM die. ODT(ca) pads for other ranks (if present) are disabled in the package.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to V_{SS} package balls.

NOTE 6 The flash ball-out supports *e*•MMC 5.x

NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

Documents
Document Sharing Hub
Full document details: JEDEC JESD209-4-1 2017

2.3.3 200-ball x32 Discrete Package, 0.80 mm x 0.65 mm using MO-311

0.80mm Pitch

0.65mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODTa	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

NOTE 1 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

NOTE 5 Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

AVA Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017

2.3.4 432-ball x64 HDI Discrete Package, 0.50 mm x 0.50 mm (MO-313)

Documents
Document Sharing Hub

Full document details: JEDEC JESD209-4-1 2017