

JEDEC STANDARD

Addendum No. 1 to JESD209-4 - Low Power Double Data Rate 4X (LPDDR4X)

JESD209-4-1A (Revision of JESD209-4-1, January 2017)

February 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Addendum No. 1 to JESD209-4 - LOW POWER DOUBLE DATA RATE 4X (LPDDR4X)

(From JEDEC Board Ballot JCB-20-65, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories. Item 1831.55A)

1 Scope

This document defines the LPDDR4 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit per channel SDRAM device with either one or two channels. LPDDR4 dual channel device density ranges from 4 Gb through 32 Gb and single channel density ranges from 2 Gb through 16 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) and LPDDR3 (JESD209-3).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR4 standard.

This addendum defines LPDDR4X specifications that supersede the LPDDR4 Standard (JESD209-4) to enable low V_{DDQ} operation of LPDDR4X devices to reduce power consumption.

2 Package Ballout and Pin Definition

2.1 Pad Order

Ch. A Top				Ch. B Top			
1	VDD2	41	VDD2	101	VDD2	141	VDD2
2	VSS	42	CKE_A	102	VSS	142	CKE_B
3	VDD1	43	CS_A	103	VDD1	143	CS_B
4	VDD2	44	VSS	104	VDD2	144	VSS
5	VSS	45	CA1_A	105	VSS	145	CA1_B
6	VSSQ	46	CA0_A	106	VSSQ	146	CA0_B
7	DQ8_A	47	VDD2	107	DQ8_B	147	VDD2
8	VDDQ	48	ODT(ca)_A	108	VDDQ	148	ODT(ca)_B
9	DQ9_A	49	VSS	109	DQ9_B	149	VSS
10	VSSQ	50	VDD1	110	VSSQ	150	VDD1
11	DQ10_A	51	VSSQ	111	DQ10_B	151	VSSQ
12	VDDQ	52	DQ7_A	112	VDDQ	152	DQ7_B
13	DQ11_A	53	VDDQ	113	DQ11_B	153	VDDQ
14	VSSQ	54	DQ6_A	114	VSSQ	154	DQ6_B
15	DQS1_t_A	55	VSSQ	115	DQS1_t_B	155	VSSQ
16	DQS1_c_A	56	DQ5_A	116	DQS1_c_B	156	DQ5_B
17	VDDQ	57	VDDQ	117	VDDQ	153	VDDQ
18	DMI1_A	58	DQ4_A	118	DMI1_B	158	DQ4_B
19	VSSQ	59	VSSQ	119	VSSQ	159	VSSQ
20	DQ12_A	60	DMI0_A	120	DQ12_B	160	DMI0_B
21	VDDQ	61	VDDQ	121	VDDQ	161	VDDQ
22	DQ13_A	62	DQS0_c_A	122	DQ13_B	162	DQS0_c_B
23	VSSQ	63	DQS0_t_A	123	VSSQ	163	DQS0_t_B
24	DQ14_A	64	VSSQ	124	DQ14_B	164	VSSQ
25	VDDQ	65	DQ3_A	125	VDDQ	165	DQ3_B
26	DQ15_A	66	VDDQ	126	DQ15_B	166	VDDQ
27	VSSQ	67	DQ2_A	127	VSSQ	167	DQ2_B
28	ZQ	68	VSSQ	128	RESET_n	168	VSSQ
29	VDDQ	69	DQ1_A	129	VDDQ	169	DQ1_B
30	VDD2	70	VDDQ	130	VDD2	170	VDDQ
31	VDD1	71	DQ0_A	131	VDD1	171	DQ0_B
32	VSS	72	VSSQ	132	VSS	172	VSSQ
33	CA5_A	73	VSS	133	CA5_B	173	VSS
34	CA4_A	74	VDD2	134	CA4_B	174	VDD2
35	VDD2	75	VDD1	135	VDD2	175	VDD1
36	CA3_A	76	VSS	136	CA3_B	176	VSS
37	CA2_A	77	VDD2	137	CA2_B	177	VDD2
38	VSS	Ch. A Bottom		138	VSS	Ch. B Bottom	
39	CK_c_A			139	CK_c_B		
40	CK_t_A			140	CK_t_B		
Ch. A Top				Ch. B Top			

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 VDDQ pads ((#12,#21,#57,#66,#112,#121,#157 and #166) may be individually assigned to either VDDQ or VDD2. Please refer to vendor specification.

2.2 Single Channel Pad Order

Top			
1	VDD2	40	CK_c
2	VSS	41	CK_t
3	VDD1	42	VDD2
4	VDD2	43	CKE
5	VSS	44	CS
6	VSSQ	45	VSS
7	DQ8	46	CA1
8	VDDQ	47	CA0
9	DQ9	48	VDD2
10	VSSQ	49	ODT(ca)
11	DQ10	50	VSS
12	VDDQ	51	VDD1
13	DQ11	52	VSSQ
14	VSSQ	53	DQ7
15	DQS1_t	54	VDDQ
16	DQS1_c	55	DQ6
17	VDDQ	56	VSSQ
18	DMI1	57	DQ5
19	VSSQ	58	VDDQ
20	DQ12	59	DQ4
21	VDDQ	60	VSSQ
22	DQ13	61	DMI0
23	VSSQ	62	VDDQ
24	DQ14	63	DQS0_c
25	VDDQ	64	DQS0_t
26	DQ15	65	VSSQ
27	VSSQ	66	DQ3
28	ZQ	67	VDDQ
29	VDDQ	68	DQ2
30	VDD2	69	VSSQ
31	RESET_n	70	DQ1
32	VDD1	71	VDDQ
33	VSS	72	DQ0
34	CA5	73	VSSQ
35	CA4	74	VSS
36	VDD2	75	VDD2
37	CA3	76	VDD1
38	CA2	77	VSS
39	VSS	78	VDD2
		Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 VDDQ pads (#12, #21, #57 and #66) may be individually assigned to either VDDQ or VDD2. Please refer to vendor specification.

NOTE 4 A RESET_n pad is added. The RESET_n pad location is vendor specific. See vendor device datasheets for details about RESET_n pad location.

2.3 LPDDR4X packages

2.3.1 LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch) – Using MO-317A

LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm pitch)																																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
A	NC	VDD2	DQ3_A	VSS	DQ5_A	ODT(ca)_A	CA0_A	CS1_A	CKE1_A	CA2_A	VSS	VSS	DQ13_A	VDD2	VDD1	DQ10_A	ZQ1_A	ZQ1_D	DQ10_C	VDD1	VDD2	DQ13_C	VSS	VSS	CA2_C	CKE1_C	CS1_C	CA0_C	ODT(ca)_C	DQ5_C	VSS	DQ3_C	VDD2	NC	A
B	VSS	DQ2_A	VDDQ	DM10_A	VDDQ	DQ7_A	VDD2	CS0_A	CKE0_A	VDD2	CA4_A	DQ15_A	VDDQ	DM11_A	DQ11_A	VSS	ZQ0_A	ZQ0_D	VSS	DQ11_C	DM11_C	VDDQ	DQ15_C	CA4_C	VDD2	CKE0_C	CS0_C	VDD2	DQ7_C	VDDQ	DM10_C	VDDQ	DQ2_C	VSS	B
C	DQ0_A	VDDQ	VSS	VSS	DQ4_A	VDDQ	CA1_A	VDD2	VSS	CA3_A	VSS	VDDQ	DQ12_A	VSS	VDDQ	DQ9_A	RESET_n	RFU	DQ9_C	VDDQ	VSS	DQ12_C	VDDQ	VSS	CA3_C	VSS	VDD2	CA1_C	VDDQ	DQ4_C	VSS	VSS	VDDQ	DQ0_C	C
D	VDD1	DQ1_A	DQ00_t_A	DQ00_c_A	VSS	DQ6_A	VSS	CK_t_A	CK_c_A	VSS	CA5_A	DQ14_A	VSS	DGSI_c_A	DQ01_t_A	VDDQ	DQ8_A	DQ8_C	VDDQ	DQS1_t_C	DQS1_c_C	VSS	DQ14_C	CA5_C	VSS	CK_c_C	CK_t_C	VSS	DQ6_C	VSS	DQ00_c_C	DQ00_t_C	DQ1_C	VDD1	D
E	VDD2	VSS																															VSS	VDD2	E
F	VDD2	VDD2																															VDD2	VDD2	F
G	VSS	VSS																															VSS	VSS	G
H	RFU	RFU																															RFU	RFU	H
J	RFU	RFU																															RFU	RFU	J
K	RFU	RFU																															RFU	RFU	K
L	RFU	RFU																															RFU	RFU	L
M	RFU	RFU																															RFU	RFU	M
N	RFU	RFU																															RFU	RFU	N
P	RFU	RFU																															RFU	RFU	P
R	RFU	RFU																															RFU	RFU	R
T	RFU	RFU																															RFU	RFU	T
U	RFU	RFU																															RFU	RFU	U
V	RFU	RFU																															RFU	RFU	V
W	RFU	RFU																															RFU	RFU	W
Y	RFU	RFU																															RFU	RFU	Y
AA	RFU	RFU																															RFU	RFU	AA
AB	RFU	RFU																															RFU	RFU	AB
AC	RFU	RFU																															RFU	RFU	AC
AD	RFU	RFU																															RFU	RFU	AD
AE	RFU	RFU																															RFU	RFU	AE
AF	RFU	RFU																															RFU	RFU	AF
AG	RFU	RFU																															RFU	RFU	AG
AH	VSS	VSS																															VSS	VSS	AH
AJ	VDD2	VDD2																															VDD2	VDD2	AJ
AK	VDD2	VSS																															VSS	VDD2	AK
AL	VDD1	DQ1_B	DQ00_t_B	DQ00_c_B	VSS	DQ6_B	VSS	CK_t_B	CK_c_B	VSS	CA5_B	DQ14_B	VSS	DQS1_c_B	DQ01_t_B	VDDQ	DQ8_B	DQ8_D	VDDQ	DQS1_t_D	DQS1_c_D	VSS	DQ14_D	CA5_D	VSS	CK_c_D	CK_t_D	VSS	DQ6_D	VSS	DQ00_c_D	DQ00_t_D	DQ1_D	VDD1	AL
AM	DQ0_B	VDDQ	VSS	VSS	DQ4_B	VDDQ	CA1_B	VDD2	VSS	CA3_B	VSS	VDDQ	DQ12_B	VSS	VDDQ	DQ9_B	VDD2	VDD2	DQ9_D	VDDQ	VSS	DQ12_D	VDDQ	VSS	CA3_D	VSS	VDD2	CA1_D	VDDQ	DQ4_D	VSS	VSS	VDDQ	DQ0_D	AM
AN	VSS	DQ2_B	VDDQ	DM10_B	VDDQ	DQ7_B	VDD2	CS0_B	CKE0_B	VDD2	CA4_B	DQ15_B	VDDQ	DM11_B	DQ11_B	VSS	RFU	RFU	VSS	DQ11_D	DM11_D	VDDQ	DQ15_D	CA4_D	VDD2	CKE0_D	CS0_D	VDD2	DQ7_D	VDDQ	DM10_D	VDDQ	DQ2_D	VSS	AN
AP	NC	VDD2	DQ3_B	VSS	DQ5_B	ODT(ca)_B	CA0_B	CS1_B	CKE1_B	CA2_B	VSS	VSS	DQ13_B	VDD2	VDD1	DQ10_B	RFU	RFU	DQ10_D	VDD1	VDD2	DQ13_D	VSS	VSS	CA2_D	CKE1_D	CS1_D	CA0_D	ODT(ca)_D	DQ5_D	VSS	DQ3_D	VDD2	NC	AP
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

NOTE 1 14 mm x 14 mm, 0.4 mm pitch.

NOTE 2 376 ball count, 34 rows.

NOTE 3 Top View, A1 in top left corner.

NOTE 4 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 5 Package Channel a and Channel d shall be assigned to die Channel A of different LPDDR4 die.

NOTE 6 DRAM die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.2 144 ball ePoP MCP One-Channel FBGA (top view) using MO-323A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			
A	DNU	VSSm	VSSm	VCCQ _m	VSSm	VSSm	DAT5 _m	VCCQ _m	DAT0 _m	CLK _m	VCCm	DAT6 _m	VCCQ _m	DAT7 _m	VCCQ _m	VSSm	RSTm	VSSm	DNU			VCCm
B	VSSm	VSSm	VCCm	VSSm	VDDI	VCCm	DAT1 _m	DAT4 _m	VSSm	VCCQ _m	VSSm	DAT2 _m	DAT3 _m	VSSm	DSm	VSSm	CMDm	VCCm	VSSm		eMMC	VCCQ _m
C	VSSm	VCCm																VSSm	VSSm			VSSm
D	VSF1	VSF3																VSF5	VSF8			
E	VSF2	VSF4																VSF6	VSF9			
F	RESE _{T_n}	VSS																VSF7	RFU			VDDQ
G	ZQ1_A	ZQ0_A																RFU	RFU		DRAM	VDD1
H	VSS	VSS																VSS	VSS			VDD2
J	VDD1	VDD1																VDD1	VDD1			VSS
K	VDD2	VDD2																VDD2	VDD2			
L	VSS	VDDQ																VDDQ	VSS			
M	DQ8_A	DQ9_A																DQ1_A	DQ0_A			
N	VDD2	DQ10_A																DQ2_A	VDD2			
P	DQ11_A	VSS																VSS	DQ3_A			
R	DQS1_tA	DQS1_cA																DQS0_cA	DQS0_tA			
T	VSS	VDDQ																VDDQ	VSS			
U	DM1_A	VSS																VSS	DM0_A			
V	VDD2	VDDQ																VDDQ	VDD2			
W	DQ12_A	DQ13_A																DQ5_A	DQ4_A			
Y	VSS	VDD2	DQ14_A	VDD1	CA5_A	VSS	CA2_A	VDD2	CK_c_A	VSS	CKE0_A	CS0_A	CA1_A	VDD2	VSS	DQ7_A	DQ6_A	VDD2	VSS			
AA	DNU	VSS	VDDQ	DQ15_A	VDD2	CA4_A	CA3_A	VSS	CK_t_A	CKE1_A	CS1_A	VSS	CA0_A	ODT(ca)_A	VDD1	VDDQ	VSS	VSS	DNU			

NOTE 1 0.4 mm pitch, 2 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 Body size: 8 mm x 9.5 mm

NOTE 4 ODT(ca)_A balls are wired to ODT(ca)_A pads of Rank 0 DRAM die. ODT(ca) pads for other ranks (if present) are disabled in the package.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to V_{SS} package balls.

NOTE 6 The flash ball-out supports eMMC 5.x

NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.3 200-ball x32 Discrete Package, 0.80 mm x 0.65 mm using MO-311

0.80mm Pitch													
		1	2	3	4	5	6	7	8	9	10	11	12
	A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
	B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
	C	VSS	DQ1_A	DMIO_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
	D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
	E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
	F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
	G	VSS	ODTa	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
0.65mm Pitch	H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
	J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
	K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
	L												
	M												
	N	VDD2	VSS	VDD2	VSS	CS2_B			CKE2_B	VSS	VDD2	VSS	VDD2
	P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
	R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
	T	VSS	ODT_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
	U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
	V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
	W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
	Y	VSS	DQ1_B	DMIO_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
	AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
	AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

NOTE 1 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

NOTE 5 Die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.4 432-ball x64 HDI Discrete Package, 0.50 mm x 0.50 mm (MO-313)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ		VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ	A
B	VDDQ	VDD1	DQ0_A	VSS	CA0_A	VDD2		VDD2	CA4_A	VSS	DQ8_A	VDD1	VDDQ		VDDQ	VDD1	DQ0_C	VSS	CA0_C	VDD2		VDD2	CA4_C	VSS	DQ8_C	VDD1	VDDQ	B
C	VDDQ	DQ1_A	VSS	DQ5_A	VSS	CA2_A		CA3_A	VSS	DQ13_A	VSS	DQ9_A	VDDQ		VDDQ	DQ1_C	VSS	DQ5_C	VSS	CA2_C		CA3_C	VSS	DQ13_C	VSS	DQ9_C	VDDQ	C
D	VDDQ	VSS	DQ4_A	VSS	CA1_A	VDD2		VDD2	CA5_A	VSS	DQ12_A	VSS	VDDQ		VDDQ	VSS	DQ4_C	VSS	CA1_C	VDD2		VDD2	CA5_C	VSS	DQ12_C	VSS	VDDQ	D
E	VDDQ	DQ2_A	VSS	DQ6_A	VSS	CLK_t_A		CLK_c_A	VSS	DQ14_A	VSS	DQ10_A	VDDQ		VDDQ	DQ2_C	VSS	DQ6_C	VSS	CLK_t_C		CLK_c_C	VSS	DQ14_C	VSS	DQ10_C	VDDQ	E
F	VDDQ	VSS	DQS0_t_A	VSS	CS1_A	VDD2		VDD2	CKE0_A	VSS	DQS1_t_A	VSS	VDDQ		VDDQ	VSS	DQS0_t_C	VSS	CS1_C	VDD2		VDD2	CKE0_C	VSS	DQS1_t_C	VSS	VDDQ	F
G	VDDQ	DQ3_A	VSS	DQS0_c_A	VSS	CS0_A		CKE1_A	VSS	DQS1_c_A	VSS	DQ11_A	VDDQ		VDDQ	DQ3_C	VSS	DQS0_c_C	VSS	CS0_C		CKE1_C	VSS	DQS1_c_C	VSS	DQ11_C	VDDQ	G
H	VDDQ	VSS	DMI0_A	VSS	DQ7_A	VDD2		VDD2	DQ15_A	VSS	DMI1_A	VSS	VDDQ		VDDQ	VSS	DMI0_C	VSS	DQ7_C	VDD2		VDD2	DQ15_C	VSS	DMI1_C	VSS	VDDQ	H
J	VDDQ	ZQ3_A	ZQ2_A	ODT_ca_A	CS3_A	CS2_A		CKE3_A	CKE2_A	ZQ0_A	VSS	ZQ1_A	VDDQ		VDDQ	ZQ3_C	ZQ2_C	ODT_ca_C	CS3_C	CS2_C		CKE3_C	CKE2_C	ZQ0_C	VSS	ZQ1_C	VDDQ	J
K																												K
L	Notes: 1) 0.5mm ball pitch 2) 432 ball count 3) Top view, A1 in top left corner 4) ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package 5) Package Channel A and Channel C shall be assigned to die Channel A of different DRAM die 6) ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. ZQ3, CKE3_A, CKE3_B, CS3_A, and CS3_B balls are reserved for 4-rank package. For 1-rank and 2-rank package those balls are NC 7) Die pad VSS and VSSQ signals are combined to VSS package balls																										L	
M																											M	
N																											N	
P																											P	
R																											R	
T																												T
V	VDDQ	VSS	VSS	ODT_ca_B	CS3_B	CS2_B		CKE3_B	CKE2_B	VSS	VSS	RESET_n	VDDQ		VDDQ	VSS	VSS	ODT_ca_D	CS3_D	CS2_D		CKE3_D	CKE2_D	VSS	VSS	NC	VDDQ	V
W	VDDQ	VSS	DMI0_B	VSS	DQ7_B	VDD2		VDD2	DQ15_B	VSS	DMI1_B	VSS	VDDQ		VDDQ	VSS	DMI0_D	VSS	DQ7_D	VDD2		VDD2	DQ15_D	VSS	DMI1_D	VSS	VDDQ	W
Y	VDDQ	DQ3_B	VSS	DQS0_c_B	VSS	CS0_B		CKE1_B	VSS	DQS1_c_B	VSS	DQ11_B	VDDQ		VDDQ	DQ3_D	VSS	DQS0_c_D	VSS	CS0_D		CKE1_D	VSS	DQS1_c_D	VSS	DQ11_D	VDDQ	Y
AA	VDDQ	VSS	DQS0_t_B	VSS	CS1_B	VDD2		VDD2	CKE0_B	VSS	DQS1_t_B	VSS	VDDQ		VDDQ	VSS	DQS0_t_D	VSS	CS1_D	VDD2		VDD2	CKE0_D	VSS	DQS1_t_D	VSS	VDDQ	AA
AB	VDDQ	DQ2_B	VSS	DQ6_B	VSS	CLK_t_B		CLK_c_B	VSS	DQ14_B	VSS	DQ10_B	VDDQ		VDDQ	DQ2_D	VSS	DQ6_D	VSS	CLK_t_D		CLK_c_D	VSS	DQ14_D	VSS	DQ10_D	VDDQ	AB
AC	VDDQ	VSS	DQ4_B	VSS	CA1_B	VDD2		VDD2	CA5_B	VSS	DQ12_B	VSS	VDDQ		VDDQ	VSS	DQ4_D	VSS	CA1_D	VDD2		VDD2	CA5_D	VSS	DQ12_D	VSS	VDDQ	AC
AD	VDDQ	DQ1_B	VSS	DQ5_B	VSS	CA2_B		CA3_B	VSS	DQ13_B	VSS	DQ9_B	VDDQ		VDDQ	DQ1_D	VSS	DQ5_D	VSS	CA2_D		CA3_D	VSS	DQ13_D	VSS	DQ9_D	VDDQ	AD
AE	VDDQ	VDD1	DQ0_B	VSS	CA0_B	VDD2		VDD2	CA4_B	VSS	DQ8_B	VDD1	VDDQ		VDDQ	VDD1	DQ0_D	VSS	CA0_D	VDD2		VDD2	CA4_D	VSS	DQ8_D	VDD1	VDDQ	AE
AF	VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ		VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

2.3.5 254 ball eMMC MCP Two-Channel FBGA (top view) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0 _A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1 _A	VSS	VDDQ	VSS	DQ4 _A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2 _A	VSS	VSS	DQ5 _A	VSS	DQ7 _A	DQS0 _A				CA2 _A	VSS	CA5 _A	ZQ1			C
D			DQ3 _A	VSS	DMI0 _A	VSS	DQ6 _A	VSS	DQS0 _A				CA3 _A	VSS	VSS	ZQ2			D
E													CA4 _A	VSS	CS0 _A	CKE0 _A			E
F													CA1 _A	VSS	CS1 _A	CKE1 _A			F
G			DQ13 _A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0 _A	VSS	CLK _A			G
H			DMI1 _A	VSS	VDDQ	DQ14 _A	VSS	DQ15 _A	VDDQ				VSS	CS2 _A	VSS	CLK _A			H
J			DQ11 _A	VDDQ	VDDQ	VSS	DQ12 _A	VDDQ	DQS1 _A				ODT _A	CKE2 _A	VCCQ	VCCQ	VCCQ		J
K		VDD2	DQ10 _A	VSS	DQ8 _A	DQ9 _A	VSS	VSS	DQS1 _A				VSSm	VSSm	VCCQ	VSSm	NC		K
L							VDD2	VDD2	VDD2			VSSm	DAT7	DAT8	VSSm	VSSm	VDD1		L
M			VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			DS	VSSm	VSSm	DAT1	DAT4	VCC		M
N			VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST _n			VSSm	DAT2	DAT5	VSSm	VSSm	VCC		N
P							VDD2	VDD2	VDD2			CLK	VSSm	VSSm	DAT3	DAT0	VCC		P
R		VDD2	DQ10 _B	VSS	DQ8 _B	DQ9 _B	VSS	VSS	DQS1 _B				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11 _B	VDDQ	VDDQ	VSS	DQ12 _B	VDDQ	DQS1 _B				ODT _B	CKE2 _B	VCCQ	VCCQ	NC		T
U			DMI1 _B	VSS	VDDQ	DQ14 _B	VSS	DQ15 _B	VDDQ				VSS	CS2 _B	VSS	CLK _B			U
V			DQ13 _B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0 _B	VSS	CLK _B			V
W													CA1 _B	VSS	CS1 _B	CKE1 _B			W
Y													CA4 _B	VSS	CS0 _B	CKE0 _B			Y
AA			DQ3 _B	VSS	DMI0 _B	VSS	DQ6 _B	VSS	DQS0 _B				CA3 _B	VSS	VSS	RESE _{T n}			AA
AB			DQ2 _B	VSS	VSS	DQ5 _B	VSS	DQ7 _B	DQS0 _B				CA2 _B	VSS	CA5 _B	NC			AB
AC	DNU		DQ1 _B	VSS	VDDQ	VSS	DQ4 _B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0 _B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_CA [x] balls are wired to ODT_CA [x] pads of Rank 0 DRAM die. ODT(ca) [x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

NOTE 8 The flash ball-out supports eMMC 5.x.

2.3.6 254 ball UFS MCP Two-Channel FBGA (top view) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0 _A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1 _A	VSS	VDDQ	VSS	DQ4 _A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2 _A	VSS	VSS	DQ5 _A	VSS	DQ7 _A	DQS0 _A				CA2 _A	VSS	CA5 _A	ZQ1			C
D			DQ3 _A	VSS	DMI0 _A	VSS	DQ6 _A	VSS	DQS0 _A				CA3 _A	VSS	VSS	ZQ2			D
E													CA4 _A	VSS	CS0 _A	CKE0 _A			E
F													CA1 _A	VSS	CS1 _A	CKE1 _A			F
G			DQ13 _A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0 _A	VSS	CLK _A			G
H			DMI1 _A	VSS	VDDQ	DQ14 _A	VSS	DQ15 _A	VDDQ				VSS	CS2 _A	VSS	CLK _A			H
J			DQ11 _A	VDDQ	VDDQ	VSS	DQ12 _A	VDDQ	DQS1 _A				ODT _A	CKE2 _A	VCCQ ₂	VCCQ ₂	VCCQ ₂		J
K		VDD2	DQ10 _A	VSS	DQ8 _A	DQ9 _A	VSS	VSS	DQS1 _A				VSSm	VSSm	VCCQ ₂	VSSm	VDDI _{Q2}		K
L							VDD2	VDD2	VDD2			VSSm	DIN1 _A	DIN1 _A	VSSm	VSSm	VDDI		L
M			NC	VSF1	VSF3	VSF5	RFU	VSSm	RFU			RST _n	VSSm	VSSm	DIN0 _A	DIN0 _A	VCC		M
N			NC	VSF2	VSF4	VSF6	RFU	VSSm	RFU			VSSm	DOU1 _A	DOU1 _A	VSSm	VSSm	VCC		N
P							VDD2	VDD2	VDD2			REF _{CLK}	VSSm	VSSm	DOU0 _A	DOU0 _A	VCC		P
R		VDD2	DQ10 _B	VSS	DQ8 _B	DQ9 _B	VSS	VSS	DQS1 _B				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11 _B	VDDQ	VDDQ	VSS	DQ12 _B	VDDQ	DQS1 _B				ODT _B	CKE2 _B	VCCQ	VCCQ	VDDI _Q		T
U			DMI1 _B	VSS	VDDQ	DQ14 _B	VSS	DQ15 _B	VDDQ				VSS	CS2 _B	VSS	CLK _B			U
V			DQ13 _B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0 _B	VSS	CLK _B			V
W													CA1 _B	VSS	CS1 _B	CKE1 _B			W
Y													CA4 _B	VSS	CS0 _B	CKE0 _B			Y
AA			DQ3 _B	VSS	DMI0 _B	VSS	DQ6 _B	VSS	DQS0 _B				CA3 _B	VSS	VSS	RESE _{T n}			AA
AB			DQ2 _B	VSS	VSS	DQ5 _B	VSS	DQ7 _B	DQS0 _B				CA2 _B	VSS	CA5 _B	NC			AB
AC	DNU		DQ1 _B	VSS	VDDQ	VSS	DQ4 _B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0 _B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_CA[x] balls are wired to ODT_CA[x] pads of Rank 0 DRAM die. ODT(ca)[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.7 254 ball eMMC MCP One Channel FBGA (top view) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC	DNU	DNU	A
B	DNU		NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ0		DNU	B
C			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ1			C
D			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ2			D
E													NC	NC	NC	NC			E
F													NC	NC	NC	NC			F
G			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC			G
H			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC			H
J			NC	NC	NC	NC	NC	NC	NC				NC	NC	VCCQ	VCCQ	VCCQ		J
K		NC	NC	NC	NC	NC	NC	NC	NC				VSSm	VSSm	VCCQ	VSSm	NC		K
L							NC	NC	NC				VSSm	DAT7	DAT6	VSSm	VSSm	VDDI	L
M			VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD				DS	VSSm	VSSm	DAT1	DAT4	VCC	M
N			VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n				VSSm	DAT2	DAT5	VSSm	VSSm	VCC	N
P							VDD2	VDD2	VDD2				CLK	VSSm	VSSm	DAT3	DAT0	VCC	P
R		VDD2	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1_t_B					VCCQ	VCCQ	VSSm	VSSm	VSSm	R
T			DQ11_B	VDDQ	VDDQ	VSS	DQ12_B	VDDQ	DQS1_c_B				ODT(ca)_B	CKE2_B	VCCQ	VCCQ	NC		T
U			DMI1_B	VSS	VDDQ	DQ14_B	VSS	DQ15_B	VDDQ				VSS	CS2_B	VSS	CLK_t_B			U
V			DQ13_B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_c_B			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B				CA3_B	VSS	VSS	RESE_T_n			AA
AB			DQ2_B	VSS	VSS		DQ5_B	VSS	DQ7_B	DQS0_t_B			CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_(ca)_B ball is wired to ODT_(ca)_B pad of Rank 0 DRAM die. ODT_(ca) pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_B, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad V_{SS} and V_{SSQ} signals are combined to V_{SS} package balls.

NOTE 6 Vender specific function (VSF) – this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vender specific operations.

NOTE 7 The flash ball-out supports eMMC 5.x.

2.3.8 556 ball LPDDR4X 12.4 x 12.4 mm 4ch. PoP – Using MO-317C

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29		
A	NC	VDD2	VSS	VDDQ	VDD1	VDD2	CS0_0	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD2	VSS	VDD2	CS0_2	VDD2	VDD1	VDDQ	VSS	VDD2	NC	A	
B	VDD1	DQ2_0	DQS0_t_0	DQ4_0	VSS	CA0_0	CS1_0	CK_t_0	CA3_0	VDD1	DQ13_0	DQS1_t_0	DQ11_0	VDD1	NC	VDD1	DQ11_2	DQS1_t_2	DQ13_2	VDD1	CA3_2	CK_t_2	CS1_2	CA0_2	VSS	DQ4_2	DQS0_t_2	DQ2_2	VDD1	B	
C	DQ0_0	VSS	DQS0_e_0	VSS	DQ6_0	VSS	VDD2	CK_e_0	VDD2	DQ15_0	VSS	DQS1_e_0	VSS	DQ8_0	RESET_n	DQ8_2	VSS	DQS1_e_2	VSS	DQ15_2	VDD2	CK_e_2	VDD2	VSS	DQ6_2	VSS	DQS0_e_2	VSS	DQ0_2	C	
D	VDDQ	DQ3_0	VDDQ	DQ5_0	VDDQ	CA1_0	CKE0_0	VSS	CA4_0	VDDQ	DQ12_0	VDDQ	DQ10_0	VDDQ	ZQ1_0	VDDQ	DQ10_2	VDDQ	DQ12_2	VDDQ	CA4_2	VSS	CKE0_2	CA1_2	VDDQ	DQ6_2	VDDQ	DQ3_2	VDDQ	D	
E	DQ1_0	VSS	DM0_0	VSS	DQ7_0	ODT(ca)_0	CKE1_0	CA2_0	CA5_0	DQ14_0	VSS	DM1_0	VSS	DQ8_0	ZQ0_0	DQ8_2	VSS	DM1_2	VSS	DQ14_2	CA5_2	CA2_2	CKE1_2	ODT(ca)_2	DQ7_2	VSS	DM0_2	VSS	DQ1_2	E	
F	VDD2	VDD2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD2	VDD2	F
G	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	G	
H	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	H		
J	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	J		
K	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	K		
L	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	L		
M	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	M		
N	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	N		
P	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	P		
R	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	R		
T	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	T		
U	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	U		
V	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	V		
W	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	W		
Y	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	Y		
AA	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	AA		
AB	RFU	RFU	VSS	VSS	VSS																			VSS	VSS	VSS	RFU	RFU	AB		
AC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AC	
AD	VDD2	VDD2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD2	VDD2	AD	
AE	DQ1_1	VSS	DM0_1	VSS	DQ7_1	ODT(ca)_1	CKE1_1	CA2_1	CA5_1	DQ14_1	VSS	DM1_1	VSS	DQ8_1	ZQ0_1	DQ8_3	VSS	DM1_3	VSS	DQ14_3	CA5_3	CA2_3	CKE1_3	ODT(ca)_3	DQ7_3	VSS	DM0_3	VSS	DQ1_3	AE	
AF	VDDQ	DQ3_1	VDDQ	DQ5_1	VDDQ	CA1_1	CKE0_1	VSS	CA4_1	VDDQ	DQ12_1	VDDQ	DQ10_1	VDDQ	ZQ1_1	VDDQ	DQ10_3	VDDQ	DQ12_3	VDDQ	CA4_3	VSS	CKE0_3	CA1_3	VDDQ	DQ6_3	VDDQ	DQ3_3	VDDQ	AF	
AG	DQ0_1	VSS	DQS0_e_1	VSS	DQ6_1	VSS	VDD2	CK_e_1	VDD2	DQ15_1	VSS	DQS1_e_1	VSS	VDD2	NC	DQ8_1	VSS	DQS1_e_3	VSS	DQ15_3	VDD2	CK_e_3	VDD2	VSS	DQ6_3	VSS	DQS0_e_3	VSS	DQ0_3	AG	
AH	VDD1	DQ2_1	DQS0_t_1	DQ4_1	VSS	CA0_1	CS1_1	CK_t_1	CA3_1	VDD1	DQ13_1	DQS1_t_1	DQ11_1	VDD1	NC	VDD1	DQ11_3	DQS1_t_3	DQ13_3	VDD1	CA3_3	CK_t_3	CS1_3	CA0_3	VSS	DQ4_3	DQS0_t_3	DQ2_3	VDD1	AH	
AJ	NC	VDD2	VSS	VDDQ	VDD1	VDD2	CS0_1	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD2	VSS	VDD2	VDDQ	VSS	VDDQ	VDD2	VSS	VDD2	CS0_3	VDD2	VDD1	VDDQ	VSS	VDD2	NC	AJ	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29		

NOTE 1 Package Channel 0 and Channel 3 shall be assigned to die Channel A of different LPDDR4 die.

NOTE 2 ODT(ca) for Rank 0 of each channel is wired to the respective ODT(ca) ball. ODT(ca) for other ranks (if present) is disabled in the DRAM package.

NOTE 3 ZQ0_0 ball is wired to Rank 0 of the die supporting Channel 0. ZQ0_3 ball is wired to Rank 0 of the die supporting Channel 3. ZQ1_x balls are wired in the same manner to Rank 1 (if present).