

JEDEC STANDARD

Low Power Double Data Rate 4 (LPDDR4)

JESD209-4E

(Revision of JESD209-4D, June 2021)

June 2024

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Low Power Double Data Rate 4 (LPDDR4)

(From JEDEC Board Ballot JCB-24-16, formulated under the cognizance of the JC-42.6 subcommittee on Low Power Memories, item number 1847.28).

1 Scope

This document defines the LPDDR4 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit per channel SDRAM device with either one or two channels. LPDDR4 dual channel device density ranges from 2 Gb through 32 Gb and single channel density ranges from 1 Gb through 16 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), and LPDDR3 (JESD209-3).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated into JEDEC Board Ballot to prepare the LPDDR4 standard.

2 Die Configuration, Package Ballout, and Pin Definition

2.1 Die Configuration

LPDDR4 SDRAM supports six die configurations. Figure 1 and Figure 2 show the pad signals used for each configuration. The channel numbers and the data bus configuration is defined by the DRAM manufacturer and cannot be changed by the system.

1. Dual channel die
 - a) Standard - 16-bit width
 - b) Byte-mode (lower byte) - 8-bit width
 - c) Byte-mode (upper byte) - 8-bit width
2. Single channel die
 - a) Standard - 16-bit width
 - b) Byte-mode (lower byte) - 8-bit width
 - c) Byte-mode (upper byte) - 8-bit width

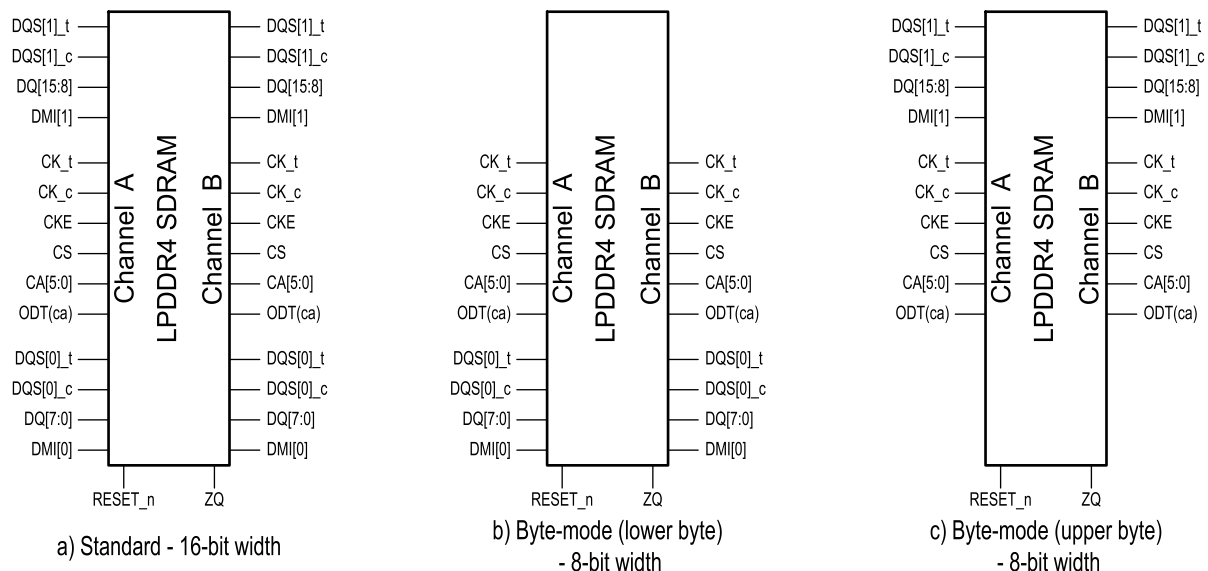


Figure 1 — Dual Channel Die

2.1 Die Configuration (cont'd)

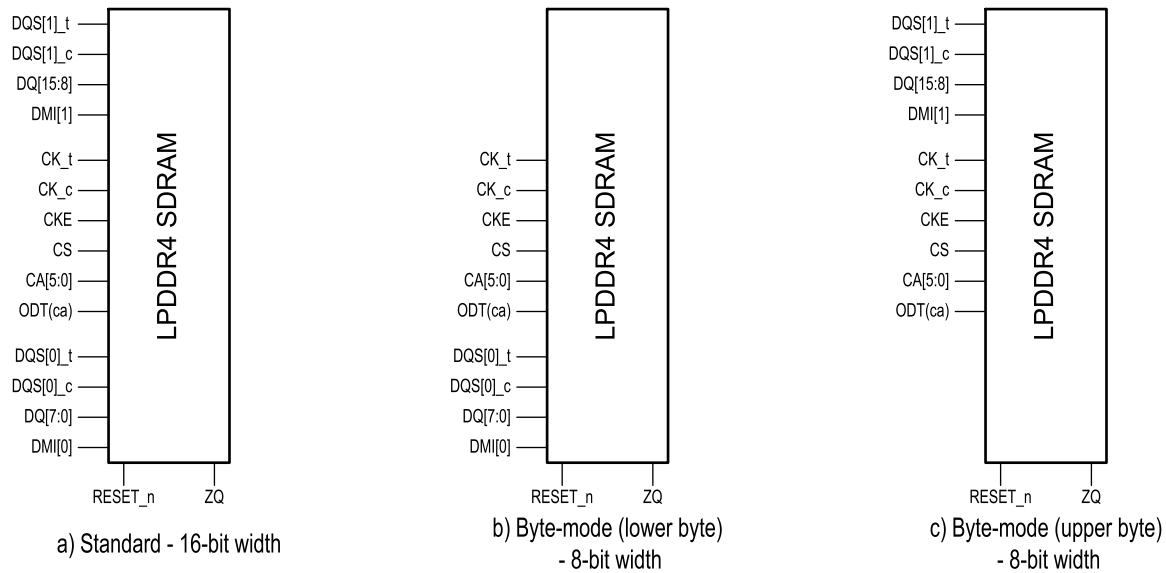


Figure 2 — Single Channel Die

Two byte-mode (one lower byte and one upper byte) die of a given density can be logically and physically combined into a 16-bit standard configuration with twice the given density. See Figure 3 for an example. Configurations using byte mode die differ from standard configurations in other characteristics such as latency, calibration considerations and total loading.

2.1 Die Configuration (Cont'd)

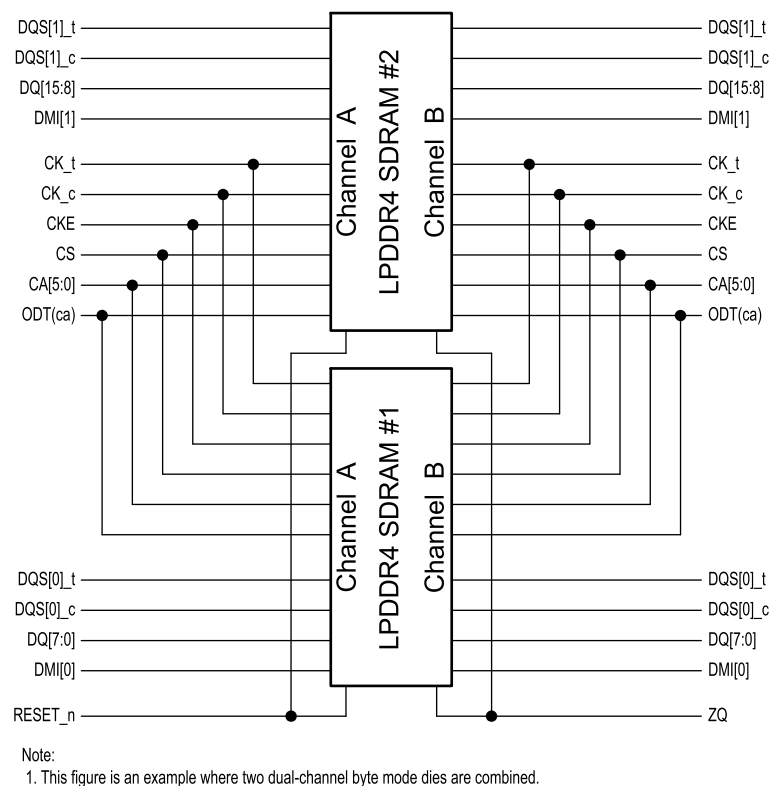


Figure 3 — Two Byte Mode Die Configuration

2.2 Pad Order

2.2.1 Pad Order for Dual Channel

Ch. A Top	
1	VDD2
2	VSS
3	VDD1
4	VDD2
5	VSS
6	VSSQ
7	DQ8_A
8	VDDQ
9	DQ9_A
10	VSSQ
11	DQ10_A
12	VDDQ
13	DQ11_A
14	VSSQ
15	DQS1_t_A
16	DQS1_c_A
17	VDDQ
18	DMI1_A
19	VSSQ
20	DQ12_A
21	VDDQ
22	DQ13_A
23	VSSQ
24	DQ14_A
25	VDDQ
26	DQ15_A
27	VSSQ
28	ZQ
29	VDDQ
30	VDD2
31	VDD1
32	VSS
33	CA5_A
34	CA4_A
35	VDD2
36	CA3_A
37	CA2_A
38	VSS
39	CK_c_A
40	CK_t_A

41	VDD2
42	CKE_A
43	CS_A
44	VSS
45	CA1_A
46	CA0_A
47	VDD2
48	ODT(ca)_A
49	VSS
50	VDD1
51	VSSQ
52	DQ7_A
53	VDDQ
54	DQ6_A
55	VSSQ
56	DQ5_A
57	VDDQ
58	DQ4_A
59	VSSQ
60	DMI0_A
61	VDDQ
62	DQS0_c_A
63	DQS0_t_A
64	VSSQ
65	DQ3_A
66	VDDQ
67	DQ2_A
68	VSSQ
69	DQ1_A
70	VDDQ
71	DQ0_A
72	VSSQ
73	VSS
74	VDD2
75	VDD1
76	VSS
77	VDD2
Ch. A Bottom	

Ch. B Top	
101	VDD2
102	VSS
103	VDD1
104	VDD2
105	VSS
106	VSSQ
107	DQ8_B
108	VDDQ
109	DQ9_B
110	VSSQ
111	DQ10_B
112	VDDQ
113	DQ11_B
114	VSSQ
115	DQS1_t_B
116	DQS1_c_B
117	VDDQ
118	DMI1_B
119	VSSQ
120	DQ12_B
121	VDDQ
122	DQ13_B
123	VSSQ
124	DQ14_B
125	VDDQ
126	DQ15_B
127	VSSQ
128	RESET_n
129	VDDQ
130	VDD2
131	VDD1
132	VSS
133	CA5_B
134	CA4_B
135	VDD2
136	CA3_B
137	CA2_B
138	VSS
139	CK_c_B
140	CK_t_B

141	VDD2
142	CKE_B
143	CS_B
144	VSS
145	CA1_B
146	CA0_B
147	VDD2
148	ODT(ca)_B
149	VSS
150	VDD1
151	VSSQ
152	DQ7_B
153	VDDQ
154	DQ6_B
155	VSSQ
156	DQ5_B
157	VDDQ
158	DQ4_B
159	VSSQ
160	DMI0_B
161	VDDQ
162	DQS0_c_B
163	DQS0_t_B
164	VSSQ
165	DQ3_B
166	VDDQ
167	DQ2_B
168	VSSQ
169	DQ1_B
170	VDDQ
171	DQ0_B
172	VSSQ
173	VSS
174	VDD2
175	VDD1
176	VSS
177	VDD2
Ch. B Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

2.2.2 Pad Order for Single Channel

TOP			
1	VDD2	40	CK_c
2	VSS	41	CK_t
3	VDD1	42	VDD2
4	VDD2	43	CKE
5	VSS	44	CS
6	VSSQ	45	VSS
7	DQ8	46	CA1
8	VDDQ	47	CA0
9	DQ9	48	VDD2
10	VSSQ	49	ODT(ca)
11	DQ10	50	VSS
12	VDDQ	51	VDD1
13	DQ11	52	VSSQ
14	VSSQ	53	DQ7
15	DQS1_t	54	VDDQ
16	DQS1_c	55	DQ6
17	VDDQ	56	VSSQ
18	DMI1	57	DQ5
19	VSSQ	58	VDDQ
20	DQ12	59	DQ4
21	VDDQ	60	VSSQ
22	DQ13	61	DMI0
23	VSSQ	62	VDDQ
24	DQ14	63	DQS0_c
25	VDDQ	64	DQS0_t
26	DQ15	65	VSSQ
27	VSSQ	66	DQ3
28	ZQ	67	VDDQ
29	VDDQ	68	DQ2
30	VDD2	69	VSSQ
31	RESET_n	70	DQ1
32	VDD1	71	VDDQ
33	VSS	72	DQ0
34	CA5	73	VSSQ
35	CA4	74	VSS
36	VDD2	75	VDD2
37	CA3	76	VDD1
38	CA2	77	VSS
39	VSS	78	VDD2
		Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 A RESET_n pad is added. The RESET_n pad location is vendor specific. See vendor device data sheets for details about RESET_n pad location.

2.3 Package Ballout

2.3.1 272 Ball 15 mm x 15 mm 0.4 mm Pitch, Quad-Channel POP FBGA (Top View) using Variation VFFCDB for MO-273

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A	DNU	VSS	VDD1	CA4_a	VDDQ	ZQ1_a	VDDQ	DQ15_a	VDD2	DQ13_a	VDD2	DMI1_a	VDDQ	DQS1_c_a	VDDQ	DQ10_a	VSS	DQ8_a	DQ0_c	VDD1	DQ2_c	VDDQ	DQS0_c_c	VDDQ	DQ4_c	VDD2	DQ5_c	VDD2	DQ7_c	VDDQ	CA0_c	VDDQ	CS1_c	VDD1	VSS	DNU
B	VSS	VDD2	CA3_a	VSS	CA5_a	VSS	ZQ0_a	VSS	DQ14_a	VSS	DQ12_a	VSS	DQS1_t_a	VSS	DQ11_a	VSS	DQ9_a	VDD2	VSS	DQ1_c	VSS	DQ3_c	VSS	DQS0_t_c	VSS	DMI0_c	VSS	DQ6_c	VSS	ODTca_c	VSS	CA1_c	VSS	CS0_c	VDD2	VSS
C	CA2_a	CK_c_a																																	CKE0_c	CKE1_c
D	VDD2	CK_t_a																																	CK_t_c	VDD2
E	CKE0_a	VSS																																	VSS	CK_c_c
F	CKE1_a	CS0_a																																	CA2_c	CA3_c
G	VDD2	CS1_a																																	CA4_c	VDD2
H	CA1_a	VSS																																	VSS	CA5_c
J	CA0_a	ODTca_a																																	ZQ0_c	ZQ1_c
K	VDDQ	DQ7_a																																	DQ15_c	VDDQ
L	DQ6_a	VSS																																	VSS	DQ14_c
M	DQ5_a	DQ4_a																																	DQ12_c	DQ13_c
N	VDDQ	DMI0_a																																	DMI1_c	VDDQ
P	DQS0_c_a	VSS																																	VSS	DQS1_c_c
R	DQ3_a	DQS0_t_a																																	DQS1_t_c	DQ11_c
T	VDDQ	DQ2_a																																	DQ10_c	VDDQ
U	DQ1_a	VSS																																	VSS	DQ9_c
V	VDD1	DQ0_a																																	DQ8_c	VDD1
W	DQ0_b	VDD2																																	VDD2	DQ8_d
Y	DQ1_b	VSS																																	VSS	DQ9_d
AA	VDDQ	DQ2_b																																	DQ10_d	VDDQ
AB	DQ3_b	DQS0_t_b																																	DQS1_t_d	DQ11_d
AC	DQS0_c_b	VSS																																	VSS	DQS1_c_d
AD	VDDQ	DMI0_b																																	DMI1_d	VDDQ
AE	DQ5_b	DQ4_b																																	DQ12_d	DQ13_d
AF	DQ6_b	VSS																																	VSS	DQ14_d
AG	VDDQ	DQ7_b																																	DQ15_d	VDDQ
AH	CA0_b	ODTca_b																																	NC	NC
AJ	CA1_b	VSS																																	VSS	CA5_d
AK	VDD2	CS1_b																																	CA4_d	VDD2
AL	CKE1_b	CS0_b																																	CA2_d	CA3_d
AM	CKE0_b	VSS																																	VSS	CK_c_d
AN	VDD2	CK_t_b																																	CK_t_d	VDD2
AP	CA2_b	CK_c_b																																	CKE0_d	CKE1_d
AR	VSS	VDD2	CA3_b	VSS	CA5_b	VSS	RESET_n	VSS	DQ14_b	VSS	DMI1_b	VSS	DQS1_t_b	VSS	DQ11_b	VSS	DQ9_b	VDD2	VSS	DQ1_d	VSS	DQ3_d	VSS	DQS0_t_d	VSS	DQ4_d	VSS	DQ6_d	VSS	ODTca_d	VSS	CA1_d	VSS	CS0_d	VDD2	VSS
AT	DNU	VSS	VDD1	CA4_b	VDDQ	NC	VDDQ	DQ15_b	VDD2	DQ13_b	VDD2	DQ12_b	VDDQ	DQS1_c_b	VDDQ	DQ10_b	VSS	DQ8_b	DQ0_d	VDD1	DQ2_d	VDDQ	DQS0_c_d	VDDQ	DMI0_d	VDD2	DQ5_d	VDD2	DQ7_d	VDDQ	CA0_d	VDDQ	CS1_d	VDD1	VSS	DNU

- VDD1

VDD2

VDDQ

VSS

CK_t, CK_c

DMI

DQ, CA, CS,

DNU, NC

DQS_t, DQS_c

RESET_n, ZQ,
- NOTE 1

15 mm x 15 mm, 0.4 mm pitch.
- NOTE 2

272 ball count, 36 rows.
- NOTE 3

Top View, A1 in top left corner.
- NOTE 4

ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.
- NOTE 5

Package Channel a and Channel c shall be assigned to die Channel A of different DRAM die.
- NOTE 6

Die pad VSS and VSSQ signals are combined to VSS package balls.
- NOTE 7

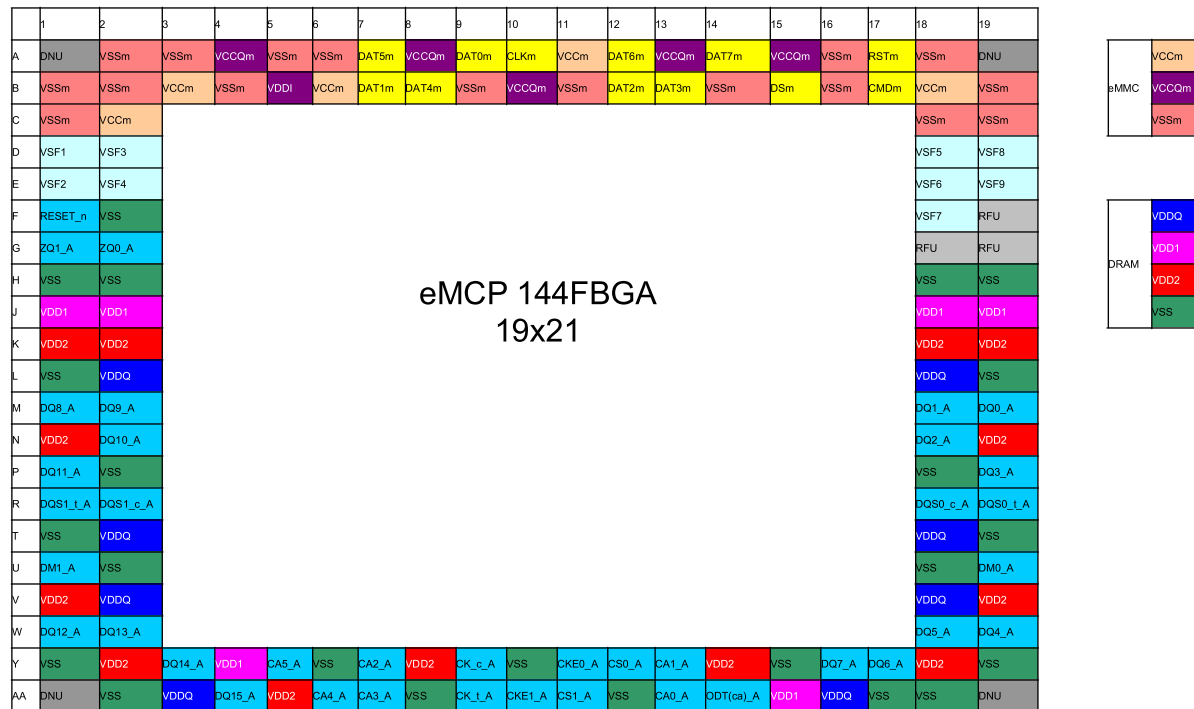
Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.2 LPDDR4 34x34 Quad x16 Channel (Fits 14x14 0.4 mm Pitch) - using MO-317A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34		
A	NC	VDD2	DQ3_A	VSS	DQ5_A	ODT(ca)_A	CA0_A	CS1_A	CKE1_A	CA2_A	VSS	VSS	DQ13_A	VDD2	VDD1	DQ10_A	ZQ1_A	ZQ1_D	DQ10_C	VDD1	VDD2	DQ13_C	VSS	VSS	CA2_C	CKE1_C	CS1_C	CA0_C	ODT(ca)_C	DQ5_C	VSS	DQ3_C	VDD2	NC	A	
B	VSS	DQ2_A	VDDQ	DM10_A	VDDQ	DQ7_A	VDD2	CS0_A	CKE0_A	VDD2	CA4_A	DQ15_A	VDDQ	DM11_A	DQ11_A	VSS	ZQ0_A	ZQ0_D	VSS	DQ11_C	DM11_C	VDDQ	DQ15_C	CA4_C	VDD2	CKE0_C	CS0_C	VDD2	DQ7_C	VDDQ	DM10_C	VDDQ	DQ2_C	VSS	B	
C	DQ0_A	VDDQ	VSS	VSS	DQ4_A	VDDQ	CA1_A	VDD2	VSS	CA3_A	VSS	VDDQ	DQ12_A	VSS	VDDQ	DQ9_A	RESET_n	RFU	DQ9_C	VDDQ	VSS	DQ12_C	VDDQ	VSS	CA3_C	VSS	VDD2	CA1_C	VDDQ	DQ4_C	VSS	VSS	VDDQ	DQ0_C	C	
D	VDD1	DQ1_A	DQ50_t_A	DQ50_c_A	VSS	DQ6_A	VSS	CK_t_A	CK_c_A	VSS	CAS_A	DQ14_A	VSS	DQ51_c_A	DQ51_t_A	VDDQ	DQ8_A	DQ8_C	VDDQ	DQ51_t_C	DQ51_c_C	VSS	VSS	DQ14_C	CAS_C	VSS	CK_c_C	CK_t_C	VSS	DQ6_C	VSS	DQ50_c_C	DQ50_t_C	DQ1_C	VDD1	D
E	VDD2	VSS																															VSS	VDD2	E	
F	VDD2	VDD2																															VDD2	VDD2	F	
G	VSS	VSS																															VSS	VSS	G	
H	RFU	RFU																															RFU	RFU	H	
J	RFU	RFU																															RFU	RFU	J	
K	RFU	RFU																															RFU	RFU	K	
L	RFU	RFU																															RFU	RFU	L	
M	RFU	RFU																															RFU	RFU	M	
N	RFU	RFU																															RFU	RFU	N	
P	RFU	RFU																															RFU	RFU	P	
R	RFU	RFU																															RFU	RFU	R	
T	RFU	RFU																															RFU	RFU	T	
U	RFU	RFU																															RFU	RFU	U	
V	RFU	RFU																															RFU	RFU	V	
W	RFU	RFU																															RFU	RFU	W	
Y	RFU	RFU																															RFU	RFU	Y	
AA	RFU	RFU																															RFU	RFU	AA	
AB	RFU	RFU																															RFU	RFU	AB	
AC	RFU	RFU																															RFU	RFU	AC	
AD	RFU	RFU																															RFU	RFU	AD	
AE	RFU	RFU																															RFU	RFU	AE	
AF	RFU	RFU																															RFU	RFU	AF	
AG	RFU	RFU																															RFU	RFU	AG	
AH	VSS	VSS																															VSS	VSS	AH	
AJ	VDD2	VDD2																															VDD2	VDD2	AJ	
AK	VDD2	VSS																															VSS	VDD2	AK	
AL	VDD1	DQ1_B	DQ50_t_B	DQ50_c_B	VSS	DQ6_B	VSS	CK_t_B	CK_c_B	VSS	CAS_B	DQ14_B	VSS	DQ51_c_B	DQ51_t_B	VDDQ	DQ8_B	DQ8_D	VDDQ	DQ51_t_D	DQ51_c_D	VSS	DQ14_D	CAS_D	VSS	CK_c_D	CK_t_D	VSS	DQ6_D	VSS	DQ50_c_D	DQ50_t_D	DQ1_D	VDD1	AL	
AM	DQ0_B	VDDQ	VSS	VSS	DQ4_B	VDDQ	CA1_B	VDD2	VSS	CA3_B	VSS	VDDQ	DQ12_B	VSS	VDDQ	DQ9_B	VDD2	VDD2	DQ9_D	VDDQ	VSS	DQ12_D	VDDQ	VSS	CA3_D	VSS	VDD2	CA1_D	VDDQ	DQ4_D	VSS	VSS	VDDQ	DQ0_D	AM	
AN	VSS	DQ2_B	VDDQ	DM10_B	VDDQ	DQ7_B	VDD2	CS0_B	CKE0_B	VDD2	CA4_B	DQ15_B	VDDQ	DM11_B	DQ11_B	VSS	RFU	RFU	VSS	DQ11_D	DM11_D	VDDQ	DQ15_D	CA4_D	VDD2	CKE0_D	CS0_D	VDD2	DQ7_D	VDDQ	DM10_D	VDDQ	DQ2_D	VSS	AN	
AP	NC	VDD2	DQ3_B	VSS	DQ5_B	ODT(ca)_B	CA0_B	CS1_B	CKE1_B	CA2_B	VSS	VSS	DQ13_B	VDD2	VDD1	DQ10_B	RFU	RFU	DQ10_D	VDD1	VDD2	DQ13_D	VSS	VSS	CA2_D	CKE1_D	CS1_D	CA0_D	ODT(ca)_D	DQ5_D	VSS	DQ3_D	VDD2	NC	AP	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34		

- NOTE 1
- 14 mm x 14 mm, 0.4 mm pitch.
- NOTE 2
- 376 ball count, 34 rows.
- NOTE 3
- Top View, A1 in top left corner.
- NOTE 4
- ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.
- NOTE 5
- Package Channel a and Channel d shall be assigned to die Channel A of different LPDDR4 die.
- NOTE 6
- DRAM die pad VSS and VSSQ signals are combined to VSS package balls.
- NOTE 7
- Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.3 144 Ball ePoP MCP One-Channel FBGA (Top View) using MO-323A



- NOTE 1 0.4 mm pitch, 2 rows.
 NOTE 2 Top View, A1 in top left corner.
 NOTE 3 Body size: 8 mm x 9.5 mm
 NOTE 4 ODT(ca)_A balls are wired to ODT(ca)_A pads of Rank 0 DRAM die. ODT(ca) pads for other ranks (if present) are disabled in the package.
 NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.
 NOTE 6 The flash ball-out supports eMMC 5.x
 NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.4 200 Ball Packages

2.3.4.1 200 Ball x32 Discrete Package, 0.80 mm x 0.65 mm using MO-311

0.80 mm Pitch												
	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT(ca)_A	VSS	VDD1	VSS			VSS	VDD1	VSS	ZQ2	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
0.65 mm Pitch	N	VDD2	VSS	VDD2	VSS	CS2_B		CKE2_B	VSS	VDD2	VSS	VDD2
	P	VSS	CA1_B	VSS	CKE0_B	CKE1_B		CK_t_B	CK_c_B	VSS	CA5_B	VSS
	R	VDD2	CA0_B	CS1_B	CS0_B	VDD2		VDD2	CA2_B	CA3_B	CA4_B	VDD2
	T	VSS	ODT(ca)_B	VSS	VDD1	VSS		VSS	VDD1	VSS	RESET_n	VSS
	U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2		VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
	V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS		VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
	W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ		VDDQ	VSS	DQS1_t_B	VSS	VDDQ
	Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS		VSS	DQ14_B	DMI1_B	DQ9_B	VSS
	AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ		VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
	AB	DNU	DNU	VSS	VDD2	VSS		VSS	VDD2	VSS	DNU	DNU

NOTE 1 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_x balls are wired to ODT(ca)_x pads of Rank 0 DRAM die. ODT(ca)_x pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

NOTE 5 Die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.4.2 200 Ball 1CHx16 Discrete Package, 0.80 mm x 0.65 mm using MO-311

0.80 mm Pitch												
	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT(c_a)_A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	CS2_A			CKE2_A	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	CS3_A			CKE3_A	VSS	VDD2	VSS	VDD2
P	VSS	NC	VSS	NC	NC			NC	NC	VSS	NC	VSS
R	VDD2	NC	NC	NC	VDD2			VDD2	NC	NC	NC	VDD2
T	VSS	NC	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	NC	VDDQ	NC	VDD2			VDD2	NC	VDDQ	NC	VDD1
V	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
W	VDDQ	VSS	NC	VSS	VDDQ			VDDQ	VSS	NC	VSS	VDDQ
Y	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
A A	DNU	NC	VDDQ	NC	VDDQ			VDDQ	NC	VDDQ	NC	DNU
A B	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU

NOTE 1 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_x balls are wired to ODT(ca)_x pads of Rank 0 DRAM die. ODT(ca)_x pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. For 1-rank and 2-rank package those balls are NC.

NOTE 5 Die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.4.2 200 Ball 1CHx16 Discrete Package, 0.80 mm x 0.65 mm using MO-311 (cont'd)

NOTE 7 For packages with greater than two ranks using only standard devices, Ranks 0/1 shall be wired to one ZQ ball and Ranks 2/3 (if present) shall be wired to the opposite ZQ ball. ZQ Calibration commands issued to any or all DRAM's in Rank 0/1 apply under the same conditions normally associated with channels (See Section 4.38.2 Multi-Channel Considerations for Dual Channel Devices). Similarly, this note applies separately to Ranks 2/3 (if present).

NOTE 8 In configurations that include byte mode devices where ZQ is wired by byte instead of by rank, ZQ Calibration commands issued to any or all DRAM's in Rank 0/1 apply under the same conditions normally associated with channels (See Section 4.38.2 Multi-Channel Considerations for Dual Channel Devices). Similarly, this note applies separately to Ranks 2/3 (if present). In addition, ZQ Calibration commands shall not be overlapping between Ranks 0/1 and Ranks 2/3.

2.3.5 203 Ball Discrete Two-Channel FBGA (Top View) using MO-311

	1	2	3	4	5	6	7	8	9	10	11	12	
A	DNU	DNU	VDD2	VDDQ	VDDQ	VDD2	VDD1		VDDQ	VDDQ	DNU	DNU	A
B	DNU	DQ0_A	DQ3_A	VSS	DQ4_A	VSS	VDD2		VSS	VDD2	VDD1	DNU	B
C	DQ1_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0_t_A		VSS	VSS	VSS	ZQ2_A	C
D	DQ2_A	VSS	DMI0_A	VSS	DQ6_A	VSS	DQS0_c_A		CA2_A	VSS	CA5_A	ZQ0_A	D
E									CA3_A	VSS	VSS	ZQ1_A	E
F									CA4_A	VSS	CS0_A	CKE0_A	F
G	DQ13_A	VSS	VSS	VSS	VSS	VSS	VDDQ		CA1_A	VSS	VSS	CKE1_A	G
H	DMI1_A	VSS	VSS	DQ14_A	VSS	DQ15_A	VDDQ		VSS	CA0_A	CKE2_A	CLK_c_A	H
J	DQ11_A	VSS	VSS	VSS	DQ12_A	VDDQ	DQS1_c_A		VSS	VSS	CS1_A	CLK_t_A	J
K	DQ10_A	VSS	DQ8_A	DQ9_A	VSS	VDDQ	DQS1_t_A		VSS	VSS	CS2_A	ODT ca_A	K
L	VSS	VSS	VSS	VSS	VSS	VDDQ	VDDQ		VDD2	VDD2	VDD2	VDD2	L
M	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VDDQ	DQS1_t_B		VSS	VSS	CS2_B	ODT ca_B	M
N	DQ11_B	VSS	VSS	VSS	DQ12_B	VDDQ	DQS1_c_B		VSS	VSS	CS1_B	CLK_t_B	N
P	DMI1_B	VSS	VSS	DQ14_B	VSS	DQ15_B	VDDQ		VSS	CA0_B	CKE2_B	CLK_c_B	P
R	DQ13_B	VSS	VSS	VSS	VSS	VSS	VDDQ		CA1_B	VSS	VSS	CKE1_B	R
T									CA4_B	VSS	CS0_B	CKE0_B	T
U									CA3_B	VSS	VSS	RESET_n	U
V	DQ2_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B		CA2_B	VSS	CA5_B	NC	V
W	DQ1_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B		VSS	VSS	VSS	NC	W
Y	DNU	DQ0_B	DQ3_B	VSS	DQ4_B	VSS	VDD2		VSS	VDD2	VDD1	DNU	Y
AA	DNU	DNU	VDD2	VDDQ	VDDQ	VDD2	VDD1		VDDQ	VDDQ	DNU	DNU	AA
	1	2	3	4	5	6	7	8	9	10	11	12	

NOTE 1 0.8 mm pitch (X-axis), 0.65mm pitch (Y-axis), 21 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2_A, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 Die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.6 432 Ball x64 HDI Discrete Package, 0.50mm x 0.50mm (MO-313)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ		VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ	A
B	VDDQ	VDD1	DQ0_A	VSS	CA0_A	VDD2		VDD2	CA4_A	VSS	DQ8_A	VDD1	VDDQ		VDDQ	VDD1	DQ0_C	VSS	CA0_C	VDD2		VDD2	CA4_C	VSS	DQ8_C	VDD1	VDDQ	B
C	VDDQ	DQ1_A	VSS	DQ5_A	VSS	CA2_A		CA3_A	VSS	DQ13_A	VSS	DQ9_A	VDDQ		VDDQ	DQ1_C	VSS	DQ5_C	VSS	CA2_C		CA3_C	VSS	DQ13_C	VSS	DQ9_C	VDDQ	C
D	VDDQ	VSS	DQ4_A	VSS	CA1_A	VDD2		VDD2	CA5_A	VSS	DQ12_A	VSS	VDDQ		VDDQ	VSS	DQ4_C	VSS	CA1_C	VDD2		VDD2	CA5_C	VSS	DQ12_C	VSS	VDDQ	D
E	VDDQ	DQ2_A	VSS	DQ6_A	VSS	CLK_I_A		CLK_e_A	VSS	DQ14_A	VSS	DQ10_A	VDDQ		VDDQ	DQ2_C	VSS	DQ6_C	VSS	CLK_I_C		CLK_e_C	VSS	DQ14_C	VSS	DQ10_C	VDDQ	E
F	VDDQ	VSS	DQS0_I_A	VSS	CS1_A	VDD2		VDD2	CKE0_A	VSS	DQS1_I_A	VSS	VDDQ		VDDQ	VSS	DQS0_I_C	VSS	CS1_C	VDD2		VDD2	CKE0_C	VSS	DQS1_I_C	VSS	VDDQ	F
G	VDDQ	DQ3_A	VSS	DQS0_e_A	VSS	CS0_A		CKE1_A	VSS	DQS1_e_A	VSS	DQ11_A	VDDQ		VDDQ	DQ3_C	VSS	DQS0_e_C	VSS	CS0_C		CKE1_C	VSS	DQS1_e_C	VSS	DQ11_C	VDDQ	G
H	VDDQ	VSS	DMI0_A	VSS	DQ7_A	VDD2		VDD2	DQ15_A	VSS	DMI1_A	VSS	VDDQ		VDDQ	VSS	DMI0_C	VSS	DQ7_C	VDD2		VDD2	DQ15_C	VSS	DMI1_C	VSS	VDDQ	H
J	VDDQ	ZQ3_A	ZQ2_A	ODT_ca_A	CS3_A	CS2_A		CKE3_A	CKE2_A	ZQ0_A	VSS	ZQ1_A	VDDQ		VDDQ	ZQ3_C	ZQ2_C	ODT_ca_C	CS3_C	CS2_C		CKE3_C	CKE2_C	ZQ0_C	VSS	ZQ1_C	VDDQ	J
K	NOTE 1 0.5 mm ball pitch.																										K	
L	NOTE 2 432 ball count.																										L	
M	NOTE 3 Top View, A1 in top left corner.																										M	
N	NOTE 4 ODT(ca)_x] balls are wired to ODT(ca)_x] pads of Rank 0 DRAM die. ODT(ca)_x] pads for other ranks (if present) are disabled in the package.																										N	
P	NOTE 5 Package requires dual channel die or functional equivalent of single channel die-stack. Package Channel A and Channel C shall be assigned to die Channel A of different DRAM die.																										P	
R	NOTE 6 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3-rank package. ZQ3, CKE3_A, CKE3_B, CS3_A, and CS3_B balls are reserved for 4-rank package. For 1-rank and 2-rank package those balls are NC.																										R	
T	NOTE 7 Die pad VSS and VSSQ signals are combined to VSS package balls.																										T	
	NOTE 8 Package requires dual channel die or functional equivalent of single channel die-stack.																											
U	VDDQ	VSS	VSS	ODT_ca_B	CS3_B	CS2_B		CKE3_B	CKE2_B	VSS	VSS	RESET_n	VDDQ		VDDQ	VSS	VSS	ODT_ca_D	CS3_D	CS2_D		CKE3_D	CKE2_D	VSS	VSS	NC	VDDQ	U
V	VDDQ	VSS	DMI0_B	VSS	DQ7_B	VDD2		VDD2	DQ15_B	VSS	DMI1_B	VSS	VDDQ		VDDQ	VSS	DMI0_D	VSS	DQ7_D	VDD2		VDD2	DQ15_D	VSS	DMI1_D	VSS	VDDQ	V
W	VDDQ	DQ3_B	VSS	DQS0_e_B	VSS	CS0_B		CKE1_B	VSS	DQS1_e_B	VSS	DQ11_B	VDDQ		VDDQ	DQ3_D	VSS	DQS0_e_D	VSS	CS0_D		CKE1_D	VSS	DQS1_e_D	VSS	DQ11_D	VDDQ	W
Y	VDDQ	VSS	DQS0_I_B	VSS	CS1_B	VDD2		VDD2	CKE0_B	VSS	DQS1_I_B	VSS	VDDQ		VDDQ	VSS	DQS0_I_D	VSS	CS1_D	VDD2		VDD2	CKE0_D	VSS	DQS1_I_D	VSS	VDDQ	Y
AA	VDDQ	DQ2_B	VSS	DQ6_B	VSS	CLK_I_B		CLK_e_B	VSS	DQ14_B	VSS	DQ10_B	VDDQ		VDDQ	DQ2_D	VSS	DQ6_D	VSS	CLK_I_D		CLK_e_D	VSS	DQ14_D	VSS	DQ10_D	VDDQ	AA
AB	VDDQ	VSS	DQ4_B	VSS	CA1_B	VDD2		VDD2	CA5_B	VSS	DQ12_B	VSS	VDDQ		VDDQ	VSS	DQ4_D	VSS	CA1_D	VDD2		VDD2	CA5_D	VSS	DQ12_D	VSS	VDDQ	AB
AC	VDDQ	DQ1_B	VSS	DQ5_B	VSS	CA2_B		CA3_B	VSS	DQ13_B	VSS	DQ9_B	VDDQ		VDDQ	DQ1_D	VSS	DQ5_D	VSS	CA2_D		CA3_D	VSS	DQ13_D	VSS	DQ9_D	VDDQ	AC
AD	VDDQ	VDD1	DQ0_B	VSS	CA0_B	VDD2		VDD2	CA4_B	VSS	DQ8_B	VDD1	VDDQ		VDDQ	VDD1	DQ0_D	VSS	CA0_D	VDD2		VDD2	CA4_D	VSS	DQ8_D	VDD1	VDDQ	AD
AE	VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ		VDDQ	VDD1	VDDQ	VDDQ	VDDQ	VDD2		VDD2	VDDQ	VDDQ	VDDQ	VDD1	VDDQ	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

2.3.7 324 Ball x64 Non HDI Discrete Package

LPDDR4 324 Ball x64 Non HDI Discrete Package, Pitch: 0.8 mm x 0.8 mm; 0.65 mm x 0.65 mm; and 0.65 mm (X-axis) x 0.8 mm (Y-axis) pitch using MO-315

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU	VDD Q	DQ0_ B	VDD2	DQ1_ B	VDD Q	CA0_ B	CA1_ B	CA1_ A	CA0_ A	VDD Q	DQ1_ A	VDD2	DQ0_ A	VDD Q	DNU	DNU
B	DNU	DQS0_ T_B	DQS0_ C_B	VSS	DQ3_ B	VSS	DQ2_ B	VDD Q	CKE0_ B	CKE0_ A	VDD Q	DQ3_ A	VSS	DQ2_ A	VSS	DQS0_ C_A	DQS0_ T_A	DNU
C	VDD Q	DQ5_ B	VSS	DQ4_ B	VSS	DMI0_ B	VDD Q	CKE1_ B	VSS	VSS	CKE1_ A	VDD Q	DMI0_ A	VSS	DQ4_ A	VSS	DQ5_ A	VDD Q
D	DQ7_ B	VSS	DQ13_ B	VDD2	DQ6_ B	VSS	ODT_ CA_B	VDD2	CK_T_ B	CK_T_ A	VDD2	ODT_ CA_A	VSS	DQ6_ A	VDD2	DQ13_ A	VSS	DQ7_ A
E	VDD2	DQ14_ B	VSS	DQ12_ B	VDD2	CS0_ B	VSS	VDD2	CK_C_ B	CK_C_ A	VDD2	VSS	CS0_ A	VDD2	DQ12_ A	VSS	DQ14_ A	VDD2
F	DQ15_ B	VSS	DQS1_ C_B	VSS	VSS	VDD2	CS1_ B	VSS	CA2_ B	CA2_ A	VSS	CS1_ A	VDD2	VSS	VSS	DQS1_ C_A	VSS	DQ15_ A
G	VDD Q	DMI1_ B	VDD Q	DQS1_ T_B	VSS	VSS	VDD2	CA3_ B	VSS	VSS	CA3_ A	VDD2	VSS	VSS	DQS1_ T_A	VDD Q	DMI1_ A	VDD Q
H	DQ11_ B	VDD Q	DQ10_ B	VDD2	RESE T_N	VSS	ZQ1_ A	VDD2	CA4_ B	CA4_ A	VDD2	ZQ0_ A	VSS	NC	VDD2	DQ10_ A	VDD Q	DQ11_ A
J	VDD1	DQ8_ B	VSS	DQ9_ B	VDD2	NC	VSS	CA5_ B	VDD2	VDD2	CA5_ A	VSS	NC	VDD2	DQ9_ A	VSS	DQ8_ A	VDD1
K	VDD1	DQ8_ C	VSS	DQ9_ C	VDD2	NC	VSS	CA5_ C	VDD2	VDD2	CA5_ D	VSS	NC	VDD2	DQ9_ D	VSS	DQ8_ D	VDD1
L	DQ11_ C	VDD Q	DQ10_ C	VDD2	NC	VSS	ZQ0_ C	VDD2	CA4_ C	CA4_ D	VDD2	ZQ1_ C	VSS	NC	VDD2	DQ10_ D	VDD Q	DQ11_ D
M	VDD Q	DMI1_ C	VDD Q	DQS1_ T_C	VSS	VSS	VDD2	CA3_ C	VSS	VSS	CA3_ D	VDD2	VSS	VSS	DQS1_ T_D	VDD Q	DMI1_ D	VDD Q
N	DQ15_ C	VSS	DQS1_ C_C	VSS	VSS	VDD2	CS1_ C	VSS	CA2_ C	CA2_ D	VSS	CS1_ D	VDD2	VSS	VSS	DQS1_ C_D	VSS	DQ15_ D
P	VDD2	DQ14_ C	VSS	DQ12_ C	VDD2	CS0_ C	VSS	VDD2	CK_C_ C	CK_C_ D	VDD2	VSS	CS0_ D	VDD2	DQ12_ D	VSS	DQ14_ D	VDD2
R	DQ7_ C	VSS	DQ13_ C	VDD2	DQ6_ C	VSS	ODT_ CA_C	VDD2	CK_T_ C	CK_T_ D	VDD2	ODT_ CA_D	VSS	DQ6_ D	VDD2	DQ13_ D	VSS	DQ7_ D
T	VDD Q	DQ5_ C	VSS	DQ4_ C	VSS	DMI0_ C	VDD Q	CKE1_ C	VSS	VSS	CKE1_ D	VDD Q	DMI0_ D	VSS	DQ4_ D	VSS	DQ5_ D	VDD Q
U	DNU	DQS0_ T_C	DQS0_ C_C	VSS	DQ3_ C	VSS	DQ2_ C	VDD Q	CKE0_ C	CKE0_ D	VDD Q	DQ2_ D	VSS	DQ3_ D	VSS	DQS0_ C_D	DQS0_ T_D	DNU
V	DNU	DNU	VDD Q	DQ0_ C	VDD2	DQ1_ C	VDD Q	CA0_ C	CA1_ C	CA1_ D	CA0_ D	VDD Q	DQ1_ D	VDD2	DQ0_ D	VDD Q	DNU	DNU

NOTE 1 Mix pitch: 0.8 mm x 0.8 mm; 0.65 mm x 0.65 mm; & 0.65 mm (X-axis) x 0.8 mm (Y-axis) pitch

NOTE 2 18 Rows; 18 Column; 324 Balls; Package Size: 14.5 mm x 14.5 mm

NOTE 3 Top View, A1 in top left corner

NOTE 4 Package channel ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 5 Package Channel a and Channel c shall be assigned to die Channel A of different DRAM die.

NOTE 6 Die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.8 275 Ball MCP Two-Channel FBGA (Top View) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	DNU	DNU	DQ0_A	VSS	VDD2	VDDQ	VDDQ	VDD2	VDD1						VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1_A	VSS	VSS	VSS	DQ4_A	VSS	VDD2						VSS	VDD2	VDD2	VDD1		DNU	B
C			DQ2_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0_t_A						VSS	VSS	VSS	ZQ2_A			C
D			DQ3_A	VSS	DMI0_A	VSS	DQ6_A	VSS	DQS0_c_A						CA2_A	VSS	CA5_A	ZQ0_A			D
E															CA3_A	VSS	VSS	ZQ1_A			E
F															CA4_A	VSS	CS0_A	CKE0_A			F
G			DQ13_A	VSS	VSS	VSS	VSS	VSS	VDDQ						CA1_A	VSS	VSS	CKE1_A			G
H			DMI1_A	VSS	VSS	DQ14_A	VSS	DQ15_A	VDDQ						VSS	CA0_A	CKE2_A	CLK_c_A			H
J			DQ11_A	VSS	VSS	VSS	DQ12_A	VDDQ	DQS1_c_A						VSS	VSS	CS1_A	CLK_t_A			J
K			DQ10_A	VSS	DQ8_A	DQ9_A	VSS	VDDQ	DQS1_t_A						VSS	VSS	CS2_A	ODT_ca_A			K
L						VSS	VSS	VDDQ	VDDQ						VCCQ	VSSm	DAT1	DAT5			L
M			VSS	VSS	VSS	VSS	VCC	VCC	VSSm						VSSm	VSSm	VSSm	VSSm			M
N			VSF1	VSF3	VSF5	VSF7	VSF9	VCCQ	VSSm						RST_n	VSSm	DAT0	DAT4			N
P			NC	NC	NC	NC	NC	VCCQ	VCCQ						VSSm	CLK	VCCQ	VCCQ			P
R			VSF2	VSF4	VSF6	VSF8	NC	VCCQ	VSSm						DS	VSSm	DAT2	DAT6			R
T			VSS	VSS	VSS	VSS	VCC	VCC	VSSm						VCCQ	CMD	VSSm	VSSm			T
U						VSS	VSS	VDDQ	VDDQ						VCC	VDDI	DAT3	DAT7			U
V			DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VDDQ	DQS1_t_B						VSS	VSS	CS2_B	ODT_ca_B			V
W			DQ11_B	VSS	VSS	VSS	DQ12_B	VDDQ	DQS1_c_B						VSS	VSS	CS1_B	CLK_t_B			W
Y			DMI1_B	VSS	VSS	DQ14_B	VSS	DQ15_B	VDDQ						VSS	CA0_B	CKE2_B	CLK_c_B			Y
AA			DQ13_B	VSS	VSS	VSS	VSS	VSS	VDDQ						CA1_B	VSS	VSS	CKE1_B			AA
AB															CA4_B	VSS	CS0_B	CKE0_B			AB
AC															CA3_B	VSS	VSS	RESET_n			AC
AD			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B						CA2_B	VSS	CA5_B	NC			AD
AE			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B						VSS	VSS	VSS	NC			AE
AF	DNU		DQ1_B	VSS	VSS	VSS	DQ4_B	VSS	VDD2						VSS	VDD2	VDD2	VDD1		DNU	AF
AG	DNU	DNU	DQ0_B	VSS	VDD2	VDDQ	VDDQ	VDD2	VDD1						VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

NOTE 1 0.5 mm pitch, 27 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2_A, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 The flash ball-out supports eMMC 5.x.

NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

NOTE 8 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.9 254 Ball eMMC MCP Two-Channel FBGA (Top View) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0_A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1_A	VSS	VDDQ	VSS	DQ4_A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0_t_A				CA2_A	VSS	CA5_A	ZQ1			C
D			DQ3_A	VSS	DMI0_A	VSS	DQ6_A	VSS	DQS0_c_A				CA3_A	VSS	VSS	ZQ2			D
E													CA4_A	VSS	CS0_A	CKE0_A			E
F													CA1_A	VSS	CS1_A	CKE1_A			F
G			DQ13_A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_A	VSS	CLK_c_A			G
H			DMI1_A	VSS	VDDQ	DQ14_A	VSS	DQ15_A	VDDQ				VSS	CS2_A	VSS	CLK_t_A			H
J			DQ11_A	VDDQ	VDDQ	VSS	DQ12_A	VDDQ	DQS1_c_A				ODT(ca)_A	CKE2_A	VCCQ	VCCQ	VCCQ		J
K		VDD2	DQ10_A	VSS	DQ8_A	DQ9_A	VSS	VSS	DQS1_t_A				VSSm	VSSm	VCCQ	VSSm	NC		K
L							VDD2	VDD2	VDD2			VSSm	DAT7	DAT6	VSSm	VSSm	VDDI		L
M			VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			DS	VSSm	VSSm	DAT1	DAT4	VCC		M
N			VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n			VSSm	DAT2	DAT5	VSSm	VSSm	VCC		N
P							VDD2	VDD2	VDD2			CLK	VSSm	VSSm	DAT3	DAT0	VCC		P
R		VDD2	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1_t_B				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11_B	VDDQ	VDDQ	VSS	DQ12_B	VDDQ	DQS1_c_B				ODT(ca)_B	CKE2_B	VCCQ	VCCQ	NC		T
U			DMI1_B	VSS	VDDQ	DQ14_B	VSS	DQ15_B	VDDQ				VSS	CS2_B	VSS	CLK_t_B			U
V			DQ13_B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_c_B			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B				CA3_B	VSS	VSS	RESET_n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 The flash ball-out supports eMMC 5.x.

NOTE 6 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 7 Package requires dual channel die or functional equivalent of single channel die-stack.

NOTE 8 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.10 254 Ball UFS MCP Two-Channel FBGA (Top View) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0_A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1_A	VSS	VDDQ	VSS	DQ4_A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0_t_A				CA2_A	VSS	CA5_A	ZQ1			C
D			DQ3_A	VSS	DMI0_A	VSS	DQ6_A	VSS	DQS0_c_A				CA3_A	VSS	VSS	ZQ2			D
E													CA4_A	VSS	CS0_A	CKE0_A			E
F													CA1_A	VSS	CS1_A	CKE1_A			F
G			DQ13_A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_A	VSS	CLK_c_A			G
H			DMI1_A	VSS	VDDQ	DQ14_A	VSS	DQ15_A	VDDQ				VSS	CS2_A	VSS	CLK_t_A			H
J			DQ11_A	VDDQ	VDDQ	VSS	DQ12_A	VDDQ	DQS1_c_A				ODT(ca)_A	CKE2_A	VCCQ2	VCCQ2	VCCQ2		J
K		VDD2	DQ10_A	VSS	DQ8_A	DQ9_A	VSS	VSS	DQS1_t_A				VSSm	VSSm	VCCQ2	VSSm	VDDIQ2		K
L							VDD2	VDD2	VDD2				VSSm	DIN1_c	DIN1_t	VSSm	VSSm	VDDI	L
M			NC	VSF1	VSF3	VSF5	RFU	VSSm	RFU				RST_n	VSSm	VSSm	DIN0_c	DIN0_t	VCC	M
N			NC	VSF2	VSF4	VSF6	RFU	VSSm	RFU				VSSm	DOUT1_c	DOUT1_t	VSSm	VSSm	VCC	N
P							VDD2	VDD2	VDD2				REF_CLK	VSSm	VSSm	DOUT0_c	DOUT0_t	VCC	P
R		VDD2	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1_t_B				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11_B	VDDQ	VDDQ	VSS	DQ12_B	VDDQ	DQS1_c_B				ODT(ca)_B	CKE2_B	VCCQ	VCCQ	VDDIQ		T
U			DMI1_B	VSS	VDDQ	DQ14_B	VSS	DQ15_B	VDDQ				VSS	CS2_B	VSS	CLK_t_B			U
V			DQ13_B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_c_B			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B				CA3_B	VSS	VSS	RESET_n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.11 254 Ball eMMC MCP One Channel FBGA (Top View) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC	DNU	DNU	A
B	DNU		NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ0		DNU	B
C			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ1			C
D			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	ZQ2			D
E													NC	NC	NC	NC			E
F													NC	NC	NC	NC			F
G			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC			G
H			NC	NC	NC	NC	NC	NC	NC				NC	NC	NC	NC			H
J			NC	NC	NC	NC	NC	NC	NC				NC	NC	VCCQ	VCCQ	VCCQ		J
K		NC	NC	NC	NC	NC	NC	NC	NC				VSSm	VSSm	VCCQ	VSSm	NC		K
L							NC	NC	NC			VSSm	DAT7	DAT6	VSSm	VSSm	VDDI		L
M			VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			DS	VSSm	VSSm	DAT1	DAT4	VCC		M
N			VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n			VSSm	DAT2	DAT5	VSSm	VSSm	VCC		N
P								VDD2	VDD2	VDD2			CLK	VSSm	VSSm	DAT3	DAT0	VCC	P
R		VDD2	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1_t_B				VCCQ	VCCQ	VSSm	VSSm	VSSm		R
T			DQ11_B	VDDQ	VDDQ	VSS	DQ12_B	VDDQ	DQS1_c_B				ODT(ca)_B	CKE2_B	VCCQ	VCCQ	NC		T
U			DMI1_B	VSS	VDDQ	DQ14_B	VSS	DQ15_B	VDDQ				VSS	CS2_B	VSS	CLK_t_B			U
V			DQ13_B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CLK_c_B			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMI0_B	VSS	DQ6_B	VSS	DQS0_c_B				CA3_B	VSS	VSS	RESET_n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5 mm pitch, 24 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_[x] balls are wired to ODT(ca)_[x] pads of Rank 0 DRAM die. ODT(ca)_[x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_B, and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 The flash ball-out supports eMMC 5.x.

NOTE 6 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 7 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.12 LPDDR4/4X Single Channel MCP (x8 NAND) using MO-TBD

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DNU	DNU											DNU	DNU	A
B	DNU	NC	NC	NC	NC	NC	NC			NC	NC	VCC	NC	DNU	B
C	NC	NC	NC	WP_n	R/B_n	VSSm	WE_n			VSSm	IO7	IO6	VCC	NC	C
D	NC	NC	NC	NC	CE_n	VSSm	RE_n			ALE	VSSm	VSSm	IO1	IO4	D
E					VDD2	VDD2	VDD2			VSSm	IO2	IO5	VCC	VCC	E
F	DQ10	VDD2	DQ8	DQ9	VSS	VSS	DQS1_t			CLE	VSSm	VSSm	IO3	IO0	F
G	DQ11	VDDQ	VDDQ	VSS	DQ12	VDDQ	DQS1_c				ODT(ca)	NC	NC	NC	G
H	DMI1	VSS	VDDQ	DQ14	VSS	DQ15	VDDQ				VSS	NC	VSS	CLK_t	H
J	DQ13	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0	VSS	CLK_c	J
K											CA1	VSS	CS1	CKE1	K
L											CA4	VSS	CS0	CKE0	L
M	DQ3	VSS	DMI0	VSS	DQ6	VSS	DQS0_c				CA3	VSS	VSS	RESET_n	M
N	DQ2	VSS	VSS	DQ5	VSS	DQ7	DQS0_t				CA2	VSS	CA5	ZQ1	N
P	DQ1	DQ0	VDDQ	VSS	DQ4	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0	P
R	DNU	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	DNU	R
T	DNU	DNU											DNU	DNU	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

NOTE 1 149 ball count, 0.5 mm pitch, 14 x 16 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_(ca) ball is wired to ODT_(ca) pad of Rank 0 DRAM die. ODT_(ca) pads for other ranks (if present) are disabled in the package.

NOTE 4 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

2.3.13 LPDDR4/4X Single Channel MCP (eMMC) using MO-TBD

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DNU	DNU											DNU	DNU	A
B	DNU	NC	NC	NC	NC	NC	NC			VCCQ	VCCQ	VCC	NC	DNU	B
C	VSF1	VSF3	VSF5	VSF7	VSF9	VSSm	CMD			VSSm	DAT7	DAT6	VCC	VDDI	C
D	VSF2	VSF4	VSF6	VSF8	NC	VSSm	RST_n			DS	VSSm	VSSm	DAT1	DAT4	D
E					VDD2	VDD2	VDD2			VSSm	DAT2	DAT5	VCC	VCC	E
F	DQ10	VDD2	DQ8	DQ9	VSS	VSS	DQS1_t			CLK	VSSm	VSSm	DAT3	DAT0	F
G	DQ11	VDDQ	VDDQ	VSS	DQ12	VDDQ	DQS1_c				ODT(ca)	NC	VCCQ	VCCQ	G
H	DMI1	VSS	VDDQ	DQ14	VSS	DQ15	VDDQ				VSS	NC	VSS	CLK_t	H
J	DQ13	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0	VSS	CLK_c	J
K											CA1	VSS	CS1	CKE1	K
L											CA4	VSS	CS0	CKE0	L
M	DQ3	VSS	DMI0	VSS	DQ6	VSS	DQS0_c				CA3	VSS	VSS	RESET_n	M
N	DQ2	VSS	VSS	DQ5	VSS	DQ7	DQS0_t				CA2	VSS	CA5	ZQ1	N
P	DQ1	DQ0	VDDQ	VSS	DQ4	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0	P
R	DNU	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	DNU	R
T	DNU	DNU											DNU	DNU	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

NOTE 1 149 ball count, 0.5 mm pitch, 14 x 16 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT_(ca) ball is wired to ODT_(ca) pad of Rank 0 DRAM die. ODT_(ca) pads for other ranks (if present) are disabled in the package.

NOTE 4 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 5 The flash ball-out supports eMMC 5.x

NOTE 6 Vendor specific function (VSF) - this terminal should not have any external electrical connections, but it may have an internal connection. The terminal may be routed to provide accessibility and may be used for general purpose vendor specific operations.

2.3.14 LPDDR4/4X 254 Ball NAND MCP Two-Channel FBGA (Top View) using MO-276

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU	DQ0_A	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	A
B	DNU		DQ1_A	VSS	VDDQ	VSS	DQ4_A	VSS	VDD2				VDD2	VDD2	VDD1	ZQ0		DNU	B
C			DQ2_A	VSS	VSS	DQ5_A	VSS	DQ7_A	DQS0_t_A				CA2_A	VSS	CA5_A	ZQ1			C
D			DQ3_A	VSS	DMIO_A	VSS	DQ6_A	VSS	DQS0_c_A				CA3_A	VSS	VSS	ZQ2			D
E													CA4_A	VSS	CS0_A	CKE0_A			E
F													CA1_A	VSS	CS1_A	CKE1_A			F
G			DQ13_A	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_A	VSS	CK_c_A			G
H			DM11_A	VSS	VDDQ	DQ14_A	VSS	DQ15_A	VDDQ				VSS	CS2_A	VSS	CK_t_A			H
J			DQ11_A	VDDQ	VDDQ	VSS	DQ12_A	VDDQ	DQS1_c_A				ODT(c_a)_A	CKE2_A	VCC	VCC	VCC		J
K		VDD2	DQ10_A	VSS	DQ8_A	DQ9_A	VSS	VSS	DQS1_t_A				VSSm	VSSm	VCC	VSSm	NC		K
L							VDD2	VDD2	VDD2				VSSm	IO7	IO6	VSSm	VSSm	NC	L
M			RFU	RFU	RFU	WP_n	R/B_n	VSSm	CLE				RE_n	VSSm	VSSm	IO3	IO2	NC	M
N			RFU	RFU	RFU	NC	CE_n	VSSm	ALE				VSSm	IO5	IO4	VSSm	VSSm	NC	N
P							VDD2	VDD2	VDD2				WE_n	VSSm	VSSm	IO1	IO0	NC	P
R		VDD2	DQ10_B	VSS	DQ8_B	DQ9_B	VSS	VSS	DQS1_t_B				VCC	VCC	VSSm	VSSm	VSSm		R
T			DQ11_B	VDDQ	VDDQ	VSS	DQ12_B	VDDQ	DQS1_c_B				ODT(c_a)_B	CKE2_B	VCC	VCC	NC		T
U			DM11_B	VSS	VDDQ	DQ14_B	VSS	DQ15_B	VDDQ				VSS	CS2_B	VSS	CK_t_B			U
V			DQ13_B	VSS	VSS	VSS	VDD2	VDD2	VDD2				VSS	CA0_B	VSS	CK_c_B			V
W													CA1_B	VSS	CS1_B	CKE1_B			W
Y													CA4_B	VSS	CS0_B	CKE0_B			Y
AA			DQ3_B	VSS	DMIO_B	VSS	DQ6_B	VSS	DQS0_c_B				CA3_B	VSS	VSS	RESET_n			AA
AB			DQ2_B	VSS	VSS	DQ5_B	VSS	DQ7_B	DQS0_t_B				CA2_B	VSS	CA5_B	NC			AB
AC	DNU		DQ1_B	VSS	VDDQ	VSS	DQ4_B	VSS	VDD2				VDD2	VDD2	VDD1	NC		DNU	AC
AD	DNU	DNU	DQ0_B	VDD1	VDD2	VDDQ	VDDQ	VDD2	VDD1				VDDQ	VDDQ	VDD1	VDD1	DNU	DNU	AD
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

NOTE 1 0.5mm pitch, 24 rows x 18 columns.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 ODT(ca)_x] balls are wired to ODT(ca)_x] pads of Rank 0 DRAM die. ODT(ca)_x] pads for other ranks (if present) are disabled in the package.

NOTE 4 ZQ2, CKE2_A, CKE2_B, CS2_A and CS2_B balls are reserved for 3 rank package, and for 1 rank and 2 rank package those balls are NC.

NOTE 5 DRAM die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 6 Package requires dual channel die or functional equivalent of single channel die-stack.

2.3.15 100 Ball x16 Discrete Package, 0.80 mm x 0.65 mm using MO-311F

		0.80 mm Pitch											
		1	2	3	4	5	6	7	8	9	10	11	12
0.65 mm Pitch	A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
	B	DNU	DQ0	VDDQ	DQ7	VDDQ			VDDQ	DQ15	VDDQ	DQ8	DNU
	C	VSS	DQ1	DMI0	DQ6	VSS			VSS	DQ14	DMI1	DQ9	VSS
	D	VDDQ	VSS	DQS0_t	VSS	VDDQ			VDDQ	VSS	DQS1_t	VSS	VDDQ
	E	VSS	DQ2	DQS0_c	DQ5	VSS			VSS	DQ13	DQS1_c	DQ10	VSS
	F	VDD1	DQ3	VDDQ	DQ4	VDD2			VDD2	DQ12	VDDQ	DQ11	VDD1
	G	VSS	ODT_CA	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
	H	VDD2	CA0	CS1	CS0	VDD2			VDD2	CA2	CA3	CA4	VDD2
	J	VSS	CA1	VSS	CKE0	CKE1			CK_t	CK_c	VSS	CA5	VSS
	K	VDD2	VSS	VDD2	VSS	RFU			RFU	VSS	VDD2	VSS	VDD2

NOTE 1: 0.8 mm pitch (X-axis), 0.65 mm pitch (Y-axis), 10 rows.

NOTE 2: Top View, A1 in top left corner.

NOTE 3: ODT_CA ball is wired to ODT_CA pad of Rank 0 DRAM die. ODT_CA pad for other ranks (if present) is disabled in the package.

NOTE 4: Die pad VSS and VSSQ signals are combined to VSS package balls.

NOTE 5: Package requires single channel die.

NOTE 6: For packages with two ranks using only standard devices, ZQ pad of Ranks 0 shall be wired to one ZQ0 ball and ZQ pad of Ranks 1 shall be wired to one ZQ1 ball

NOTE 7: In configurations that include byte mode devices where ZQ is wired by byte instead of by rank, ZQ Calibration commands issued to any or all DRAM's in Rank 0/1 apply under the same conditions normally associated with channels (See Section 4.38.2 Multi-Channel Considerations for Dual Channel Devices).

2.4 Package Configuration

Two Byte-Mode LPDDR4 SDRAM's can be logically combined into a Standard LPDDR4 SDRAM. A Standard die features either one or two 16-bit channels where each 16-bit channel supports its own CA bus. A Byte Mode die features either one or two 8-bit channels where each 8-bit channel supports its own CA bus. The inputs are ganged and the DQ busses from the two dies are assigned individually to the 16-bit channels. This approach allows for high-density packages, but requires consideration of input loading.

Packages for Standard and Byte-Mode dies share the same ballmaps. This section describes internal wiring changes and system considerations when using packages containing Byte-Mode dies.

Three different die combinations are supported:

1. Standard - Packages configured with only Standard LPDDR4 die
2. Byte-Mode - Packages configured with only Byte-Mode LPDDR4 die
3. Mixed - Packages configured with both Standard and Byte-Mode LPDDR4 die. In this mixed configuration, some ranks contain only Standard die and other ranks contain only Byte-Mode die (See package configuration example in Figure 4).

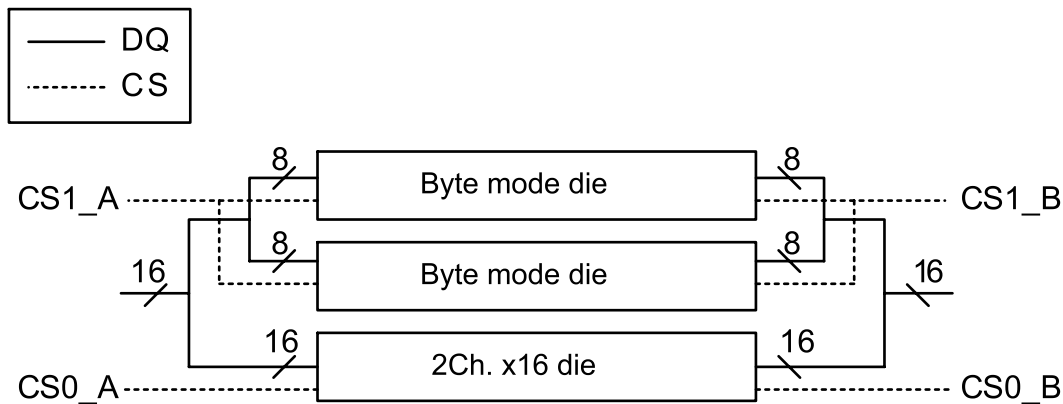


Figure 4 — Mixed Package Configuration Example

2.5 ZQ Wiring

Standard LPDDR4 package ballmaps allocate one ZQ ball per die. Byte-Mode packages potentially support more die for higher package memory density. In order to use ballmaps developed for Standard LPDDR4, an alternate ZQ ball wiring strategy is employed when packages contain Byte-Mode dies as shown in Figure 5.

Since this wiring strategy for Byte-Mode and Mixed packages shares a single ZQ resistor between ranks and channels, applications must ensure that the ZQCal's do not overlap between the dies sharing the resistor.

- **Applications shall ensure that ZQCal_Start commands to one rank on any dies sharing a ZQ resistor must complete (tZQCal satisfied) prior to issuing a ZQCal_Start command to a different rank tied to the resistor. (Applications can satisfy this requirement, for example, by either:**
 - **Issuing ZQCal_Start commands simultaneously to both DRAM channels**
 - **Issuing ZQCal_Start commands to one DRAM channel only)**
- **DRAM shall ensure that ZQCal_Start can be sent independently to the two channels on a die. If a ZQCal_Start command is received while a ZQ calibration is in progress on the die, the second ZQCal_Start command will be ignored and the in progress calibration will not be interrupted.**

(See Section 4.38.3, 'ZQ External Resistor, Tolerance, and Capacitive Loading' for more information.)

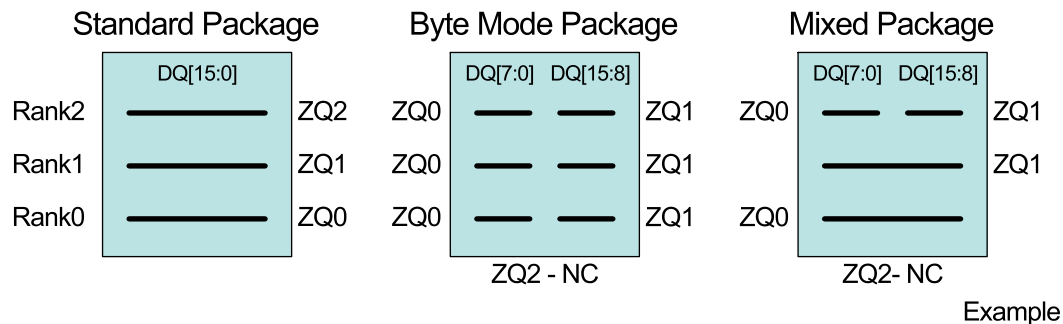


Figure 5 — ZQ Wiring Overview

Below are specific wiring notes for LPDDR4 packages.

1. For packages using only standard dies
 - ZQ0 is connected to rank 0 DRAM
 - ZQ1 is connected to rank 1 DRAM (if present)
 - ZQ2 is connected to rank 2 DRAM (if present)
2. For packages using only byte-mode dies
 - ZQ0 is connected to all lower byte [7:0] or upper byte [15:8] DRAM(s)
 - ZQ1 is connected to opposite byte of all DRAM(s) from ZQ0
 - ZQ2 is NC
3. For packages using both standard and byte-mode dies
 - ZQ0 is connected to all lower byte [7:0] or upper byte [15:8] DRAM(s)
 - ZQ1 is connected to opposite byte of all DRAM(s) from ZQ0
 - Standard DRAM(s) may be connected to either ZQ0 or ZQ1
 - ZQ2 is NC

Multi-rank packages containing Byte Mode dies place additional loading on the I/O and power topologies and therefore may not be appropriate for all application environments.

2.6 Pad Definition and Description

2.6.1 Dual Channel per Die Device

Table 1 — Pad Definition and Description for Dual channel

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A CS_B	Input	Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT(ca)_A ODT(ca)_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output: Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a $240\ \Omega \pm 1\%$ resistor.
VDDQ, VDD1, VDD2	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	Ground Reference: Power supply ground reference
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.
NOTE "_A" and "_B" indicate DRAM channel "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only.		

2.6.2 Single Channel Per Die Device

Table 2 — Pad Definition and Description for Single channel

Symbol	Type	Description
CK _t , CK _c	Input	Clock: CK _t and CK _c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK _t and the negative edge of CK _c . AC timings for CA parameters are referenced to CK.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code.
CS	Input	Chip Select: CS is part of the command code.
CA[5:0]	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table.
ODT(ca)	Input	CA ODT Control: The ODT _{CA} pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]	I/O	Data Input/Output: Bi-direction data bus.
DQS[1:0] _t , DQS[1:0] _c	I/O	Data Strobe: DQS _t and DQS _c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair.
DMI[1:0]	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240 Ω ± 1% resistor.
VDDQ, VDD1, VDD2	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	Ground Reference: Power supply ground reference
RESET _n	Input	RESET: When asserted LOW, the RESET _n signal resets all channels of the die. There is one RESET _n pad per die.

3 Functional Description

LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured with either 1 or 2 channels. Single-channel is comprised of 8-banks with from 1 Gb to 16 Gb per channel density. Dual channel is comprised of 8-banks with from 2 Gb to 32 Gb total die density.

Single-channel SDRAM devices contain the following number of bits:

- 1Gb has 1,073,741,824 bits
- 2Gb has 2,147,483,648 bits
- 3Gb has 3,221,225,472 bits
- 4Gb has 4,294,967,296 bits
- 6Gb has 6,442,450,944 bits
- 8Gb has 8,589,934,592 bits
- 12Gb has 12,884,901,888 bits
- 16Gb has 17,179,869,184 bits

Dual-channel SDRAM devices contain the following number of bits:

- 2Gb has 2,147,483,648 bits
- 4Gb has 4,294,967,296 bits
- 6Gb has 6,442,450,944 bits
- 8Gb has 8,589,934,592 bits
- 12Gb has 12,884,901,888 bits
- 16Gb has 17,179,869,184 bits
- 24Gb has 25,769,803,776 bits
- 32Gb has 34,359,738,368 bits

LPDDR4 devices use a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See command truth table for details.

These devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command.

The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 LPDDR4 SDRAM Addressing

Table 3 — LPDDR4 SDRAM x16 mode Addressing for Dual Channel SDRAM Die

Memory Density (per Die)	2Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Memory Density (per x16 channel)	1Gb	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb
Configuration	8Mb x 16DQ x 8 banks x 2 channels	16Mb x 16DQ x 8 banks x 2 channels	24Mb x 16DQ x 8 banks x 2 channels	32Mb x 16DQ x 8 banks x 2 channels	48Mb x 16DQ x 8 banks x 2 channels	64Mb x 16DQ x 8 banks x 2 channels	96Mb x 16DQ x 8 banks x 2 channels	128Mb x 16DQ x 8 banks x 2 channels
Number of Channels (per die)	2	2	2	2	2	2	2	2
Number of Banks (per Channel)	8	8	8	8	8	8	8	8
Array Pre-Fetch (bits, per channel)	256	256	256	256	256	256	256	256
Number of Rows (per Channel)	8,192	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of Columns (fetch boundaries)	64	64	64	64	64	64	64	64
Page Size (Bytes)	2048	2048	2048	2048	2048	2048	2048	2048
Channel Density (Bits per channel)	1,073,741,824	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184

Table 3 — LPDDR4 SDRAM x16 mode Addressing for Dual Channel SDRAM Die (cont'd)

Memory Density (per Die)		2Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Total Density (Bits per die)		2,147,483,648	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address		BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2	BA0 - BA2
x16	Row Addresses	R0 - R12	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16
	Column Addresses	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9	C0 - C9
Burst Starting Address Boundary		64 - bit	64 - bit	64 - bit	64 - bit	64 - bit	64 - bit	64 - Bit	64 - bit
NOTE 1 The lower two column addresses (C0 - C1) are assumed to be “zero” and are not transmitted on the CA bus. NOTE 2 Row and Column address values on the CA bus that are not used for a particular density are required to be at valid logic levels. NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is “HIGH”, then the MSB - 1 address bit must be “LOW”. NOTE 4 The row address input which violates restriction described in note 3 in this table may result in undefined or vendor specific behavior. Consult memory vendor for more information. NOTE 5 For device densities not requiring R17 and R18, R17 and R18 must both be driven High for every ACT-2 command to maintain backward compatibility. For device densities not requiring R18, R18 must be driven High for every ACT-2 command to maintain backward compatibility.									