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Low Power Double Data Rate (LPDDR) 5/5X

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LOW POWER DOUBLE DATA RATE (LPDDR) 5/5X

From JEDEC Board Ballet JCB-23-19, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories, item 1854.99C.

1 Scope

This document defines the LPDDR5/LPDDR5X standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant x16 one channel SDRAM device and x8 one channel SDRAM device. LPDDR5/LPDDR5X device density ranges from 2 Gb through 32 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3), and LPDDR4 (JESD209-4).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR5/LPDDR5X standard.

2 Overview

2.1 Features

TBD

2.2 Functional Description

LPDDR5/LPDDR5X SDRAM is a high-speed synchronous SDRAM device internally configured with 1 channel containing either 16 or 8 DQ signals. The bank architecture is user-selectable and can be either eight banks (8B Mode), four banks with four bank groups (BG Mode), or sixteen banks (16B Mode) for LPDDR5 SDRAM, and either four banks with four bank groups (BG Mode), or sixteen banks (16B Mode) for LPDDR5X SDRAM. See 2.2.3 for more information.

Density can range from 2 Gb to 32 Gb. These LPDDR5 SDRAM devices contain the following number of bits:

- 2 Gb has 2,147,483,648 bits
- 3 Gb has 3,221,225,472 bits
- 4 Gb has 4,294,967,296 bits
- 6 Gb has 6,442,450,944 bits
- 8 Gb has 8,589,934,592 bits
- 12 Gb has 12,884,901,888 bits
- 16 Gb has 17,179,869,184 bits
- 24 Gb has 25,769,803,776 bits
- 32 Gb has 34,359,738,368 bits

LPDDR5 SDRAM devices use a command clock (CK) that operates at a reduced rate from per-byte data clock (WCK). There are seven (DDR) command/address (CA) pins that the memory controller uses to transmit command, address, bank, configuration, and training information to the SDRAM. CA signals are latched on both the rising and falling CK edges when indicated by a high signal on the single (SDR) CS pin. Most commands are 1 nCK in duration. See Table 201 for details.

2.2 Functional Description (Cont'd)

The WCK:CK ratio is user-selectable as either 2:1 or 4:1. For low-power operation the WCK is generally designed to operate only when read or write data needs to be transmitted on the bus. Due to the high speeds required for WCK, the LPDDR5 SDRAM generally implements circuitry to divide the WCK frequency immediately after the WCK receiver. This leads to a requirement to synchronize WCK to CK when the WCK needs to be re-started from an idle time. See 7.2.1 for details.

The double-data-rate I/O signalling in high-speed modes is designed to operate with on-die termination on both the memory controller and the LPDDR5 SDRAM. The high-speed I/O was designed to operate with a VDDQ of 0.5 V nominal. Signals from the memory controller to the SDRAM were designed assuming a V_{oh} of $0.5 \times VDDQ$, or 250 mV. Signals from the SDRAM to the memory controller are calibrated to $0.5 \times VDDQ$, or 250 mV nominal. In low-speed modes the signalling may operate unterminated with nominal VDDQ in a range from 0.3 V – 0.5 V both to and from the SDRAM, with some limitations.

Data access size depends on the bank configuration, with 16n and 32n prefetches supported. A single BL16 Read or Write access for a x16, BG mode LPDDR5 SDRAM, typically consists of a single 256-bit-wide data transfer at the internal SDRAM core, and sixteen corresponding 16-bit wide, one half-WCK-clock-cycle data transfers at the I/O pins.

Read and Write accesses to LPDDR5 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command. Prior to issuing a Read, Write, or Mask Write command, WCK must be synchronized to CK by issuing a CAS command with (WS_RD, WS_WR or WS_FS) followed by a Read, Write, or Mask Write command.

The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

2.2.1 Pad Definition and Description

Table 1 — Pad Definition and Description

Symbol	Type	Description	Note
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c).	
CS	Input	Chip Select: CS is part of the command code and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.	
CA[6:0]	Input	Command/Address Inputs: CA signals provide the Command and Address input according to the Command Truth Table	
DQ[15:0]	I/O	Data Input/Output: Bi-direction data bus.	
WCK[1:0]_t WCK[1:0]_c	Input	Data Clocks: WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.	
RDQS [1:0]_t, RDQS[1:0]_c	RDQS_t :I/O, RDQS_c :Output	Read Data Strobe: RDQS_t and RDQS_c are the differential output clock signals used to strobe data during a READ operation. And RDQS_t is also used as a Parity pin at Write with Link Protection enabled.	1
DMI[1:0]	I/O	Data Mask Inversion: DMI achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and DMI is a bi-directional signal, and each byte of data has a DMI signal.	1
ZQ	Reference	ZQ: ZQ is used to calibrate the output drive strength and the termination resistance as calibration reference. There is one ZQ pad per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.	
VDDQ, VDD1, VDD2H, VDD2L	Supply	Power Supplies: Isolated on the die for improved noise immunity.	
VSS	GND	Ground Reference: Power supply ground reference	
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets the die. RESET_n is an asynchronous signal.	
NOTE 1 See Table 2 and Table 3, Per-Byte Signal List/Description, for multi-function definition for these pins.			

2.2.2 Pin per Byte

Table 2 — Pins Per-Byte Signal List/Description for Link Protection Disabled

Pin Name	DBI Enable	SE RDQS		SE RDQS		Diff RDQS	
		Link Protection disabled					
		(MR20 OP[1:0]=01		(MR20 OP[1:0]=11		(MR20 OP[1:0]=10	
		Write	Read	Write	Read	Write	Read
#11 DMI	No	DM	N/A	DM	N/A	DM	N/A
	Yes	DMI	DBI	DMI	DBI	DMI	DBI
#12 RDQS_t	No	N/A	RDQS_t	N/A	N/A	N/A	RDQS_t
	Yes	N/A	RDQS_t	N/A	N/A	N/A	RDQS_t
#13 RDQS_c	No	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c
	Yes	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c

Table 3 — Pins Per-Byte Signal List/Description for Link Protection Enabled

Pin Name	DBI Enable	SE RDQS		SE RDQS		Diff RDQS	
		Link Protection enabled					
		(MR20 OP[1:0]=01		(MR20 OP[1:0]=11		(MR20 OP[1:0]=10	
		Write	Read	Write	Read	Write	Read
#11 DMI	No	DM	parity	DM	parity	DM	parity
	Yes	DMI	parity	DMI	parity	DMI	parity
#12 RDQS_t	No	parity	RDQS_t	parity	N/A	parity	RDQS_t
	Yes	parity	RDQS_t	parity	N/A	parity	RDQS_t
#13 RDQS_c	No	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c
	Yes	N/A	N/A	N/A	RDQS_c	N/A	RDQS_c

2.2.3 LPDDR5/LPDDR5X Bank Architecture

LPDDR5/LPDDR5X SDRAM supports multiple bank architectures to provide optimal access methods for varied system configurations. The native burst length determined by data prefetch size depends on which bank architecture is enabled. MR8 OP[1:0] indicates the SDRAM type, and LPDDR5 SDRAM (MR8 OP[1:0]=00B) supports all three bank architectures, BG Mode, 8B Mode, and 16B Mode. LPDDR5X SDRAM (MR8 OP[1:0]=01B), supports only two bank architectures, BG Mode (4 banks, 4Bank groups) and 16B Mode (16banks, no bank groups).

Note that the contents of this standard related to 8B Mode apply only to LPDDR5 SDRAM and do not apply to LPDDR5X SDRAM.

Each architecture name is abbreviated as follows:

BG Mode = 4 banks, 4 bank groups.

8B Mode = 8 banks, no bank groups.

16B Mode = 16 banks, no bank groups.

The supported operation data rate for each Bank/Bank Group Organization is as follows:

BG Mode for more than 3200 Mbps (>3200 Mbps).

8B Mode for all data rate range.

16B Mode for equal or less than 3200 Mbps (≤3200 Mbps).

The bank architecture is selected by MR3 OP[4:3]. This mode register is replicated for each frequency set point.

The BG and 16B modes support burst lengths of 16 or 32, while 8B mode supports only burst length 32.

2.2.3.1 Block Diagram of Bank Configuration and Read Operation Outline

Figure 1, Figure 2, and Figure 3 provide the block diagrams of each architecture.

2.2.3.1.1 4Banks / 4Bank Groups Configuration

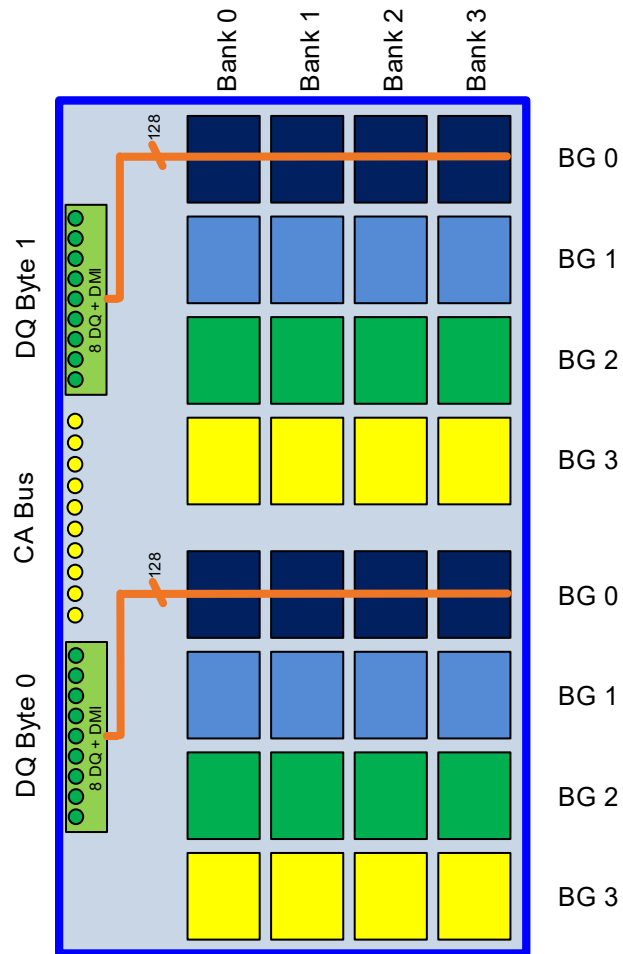


Figure 1 — BG Mode Configuration Example (One Channel Shown)

2.2.3.1.2 8Banks Mode Configuration (Does not Apply to LPDDR5X SDRAM)

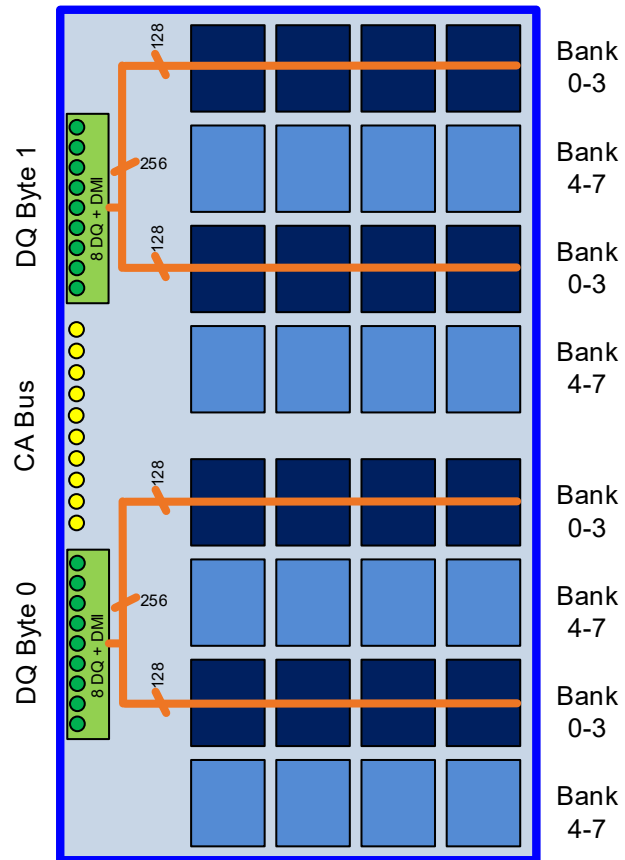


Figure 2 — 8B Mode Configuration Example (One Channel Shown)

2.2.3.1.3 16Banks Mode Configuration

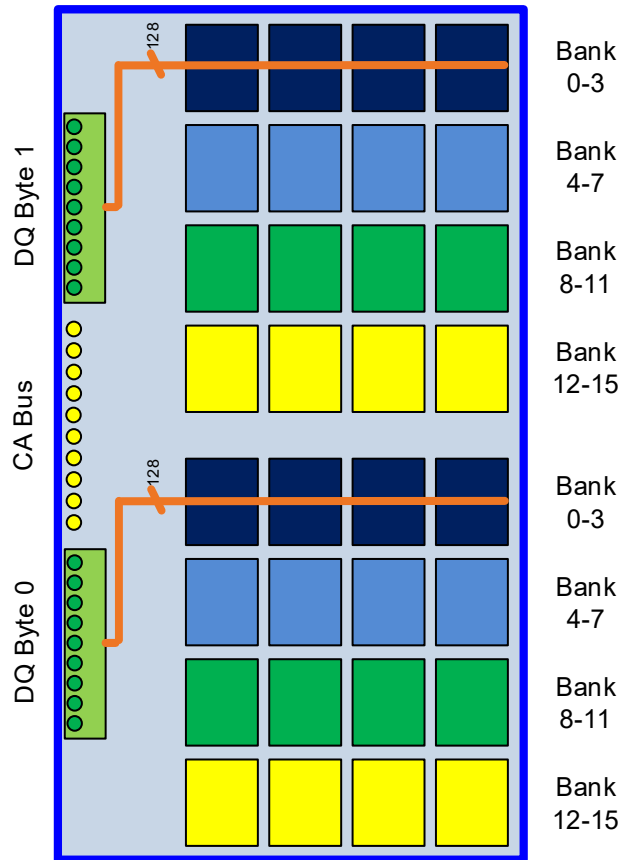


Figure 3 — 16B Mode Configuration Example (One Channel Shown)

2.2.3.2 LPDDR5/LPDDR5X Address Translation Table

The LPDDR5 SDRAM Address translation table in these three modes is shown in Table 4. Refer to Table 201 for details.

Table 4 — LPDDR5 Address Translation Table^{1,2,3}

Bank Architecture Mode	CA0	CA1	CA2	CA3
BG	BA0	BA1	BG0	BG1
8B	BA0	BA1	BA2	B4 / V
16B	BA0	BA1	BA2	BA3
NOTE 1 BA0-3: Bank Address, BG0-1: Bank Group address, B4: Burst Starting Address				
NOTE 2 In 8B mode, CA3 is B4 for READ and is V for ACT-1, PRE, MWR and WR.				
NOTE 3 Bank address (BA) and Bank Group address (BG) in column CA0 to CA2 are physically identical. However, BA3, BG1 and Burst Starting Address(B4) in column CA3 are not physically identical since the page size is different between BG/16B mode and 8B mode.				

Table 5 — LPDDR5X Address Translation Table^{1,2}

Bank Architecture Mode	CA0	CA1	CA2	CA3
BG	BA0	BA1	BG0	BG1
16B	BA0	BA1	BA2	BA3
NOTE 1 BA0-3: Bank Address, BG0-1: Bank Group address.				
NOTE 2 Bank address (BA) and Bank Group address (BG) in column CA0 to CA2 are physically identical. However, BA3, BG1 are not physically identical.				

2.2.3.3 Bank Architecture Transition

The three (for LPDDR5) or two (for LPDDR5X) bank modes can be selected by Mode Register change.

The default Bank architecture is 16B mode. To select another mode, change BK/BG ORG:MR3 OP[4:3] during Power-up, Initialization sequence.

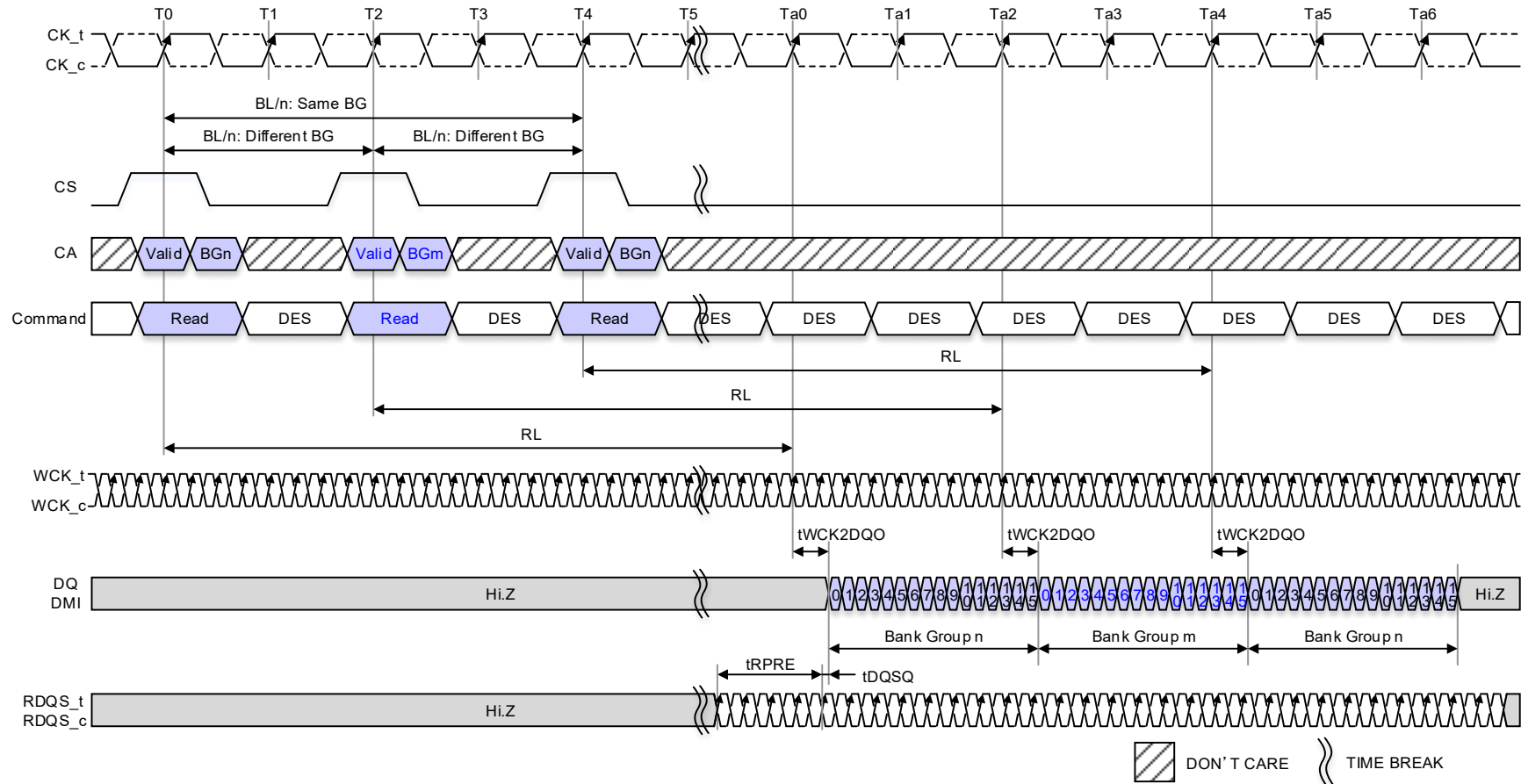
16 mode and BG mode, which are the same page size, can be switched with an FSP procedure. However, it is necessary to perform a Reset to switch between 16B/BG mode and 8B mode of different page sizes.

The bank mode change procedure between 16B and BG mode by FSP can be executed during an Idle.

2.2.3.4 Burst Operation

The Read/Write command behavior depends on the bank architecture. Read behavior is described in the Figures 4–8. These figures focus on Read data output behavior. Therefore, other behavior, for example CAS command, WCK input, is omitted. Refer to 7.4 for details.

2.2.3.4 Burst Operation (cont'd)



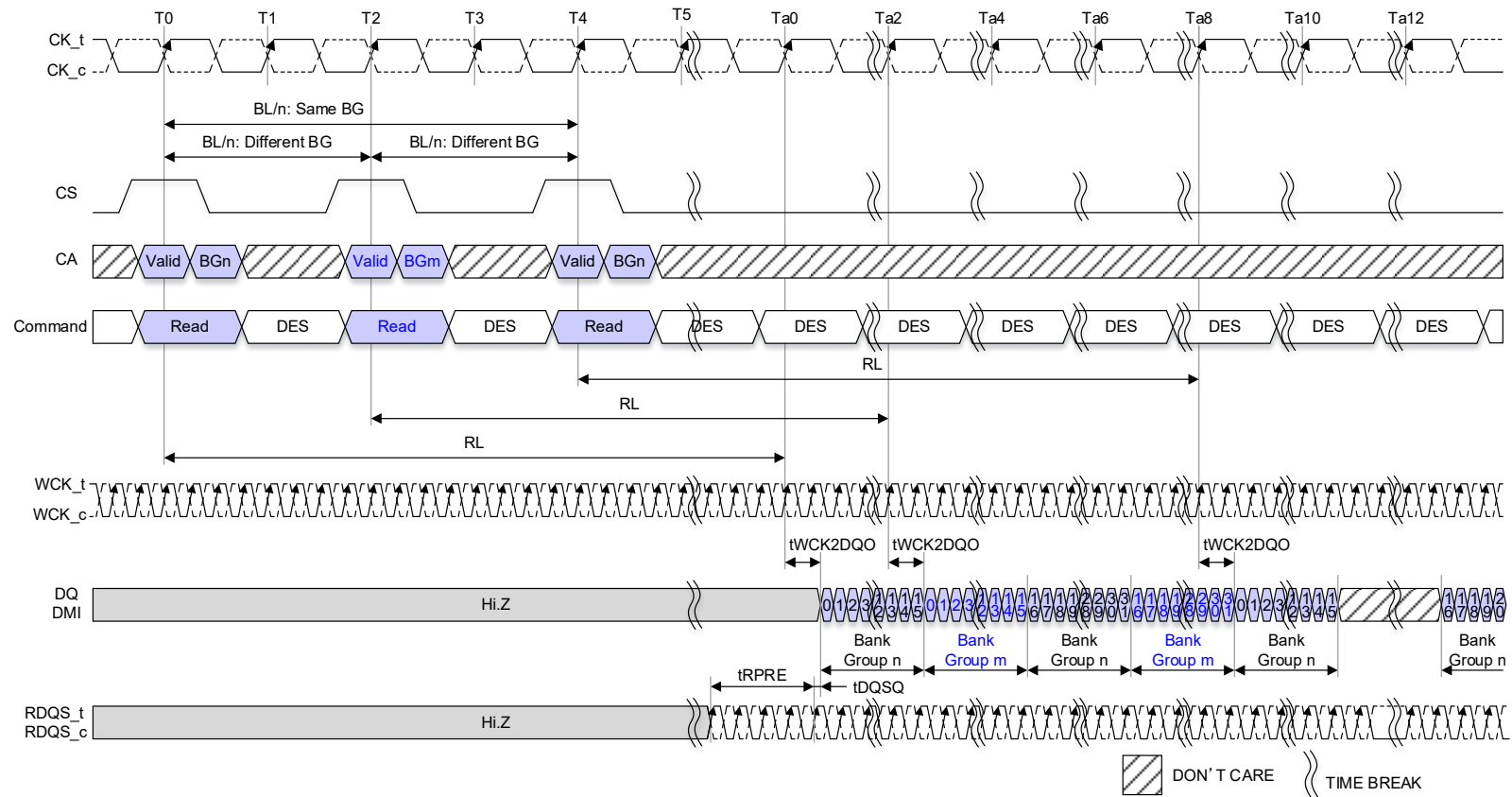
NOTE 1 MR3 OP[4:3]=00_B: BG Mode, MR18 OP[7]=0_B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 4 — Read Operation BG Mode, CKR (WCK vs. CK) = 4:1, BL=16

2.2.3.4 Burst Operation (cont'd)



NOTE 1 MR3 OP[4:3]=00_B: BG mode, MR18 OP[7]=0_B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

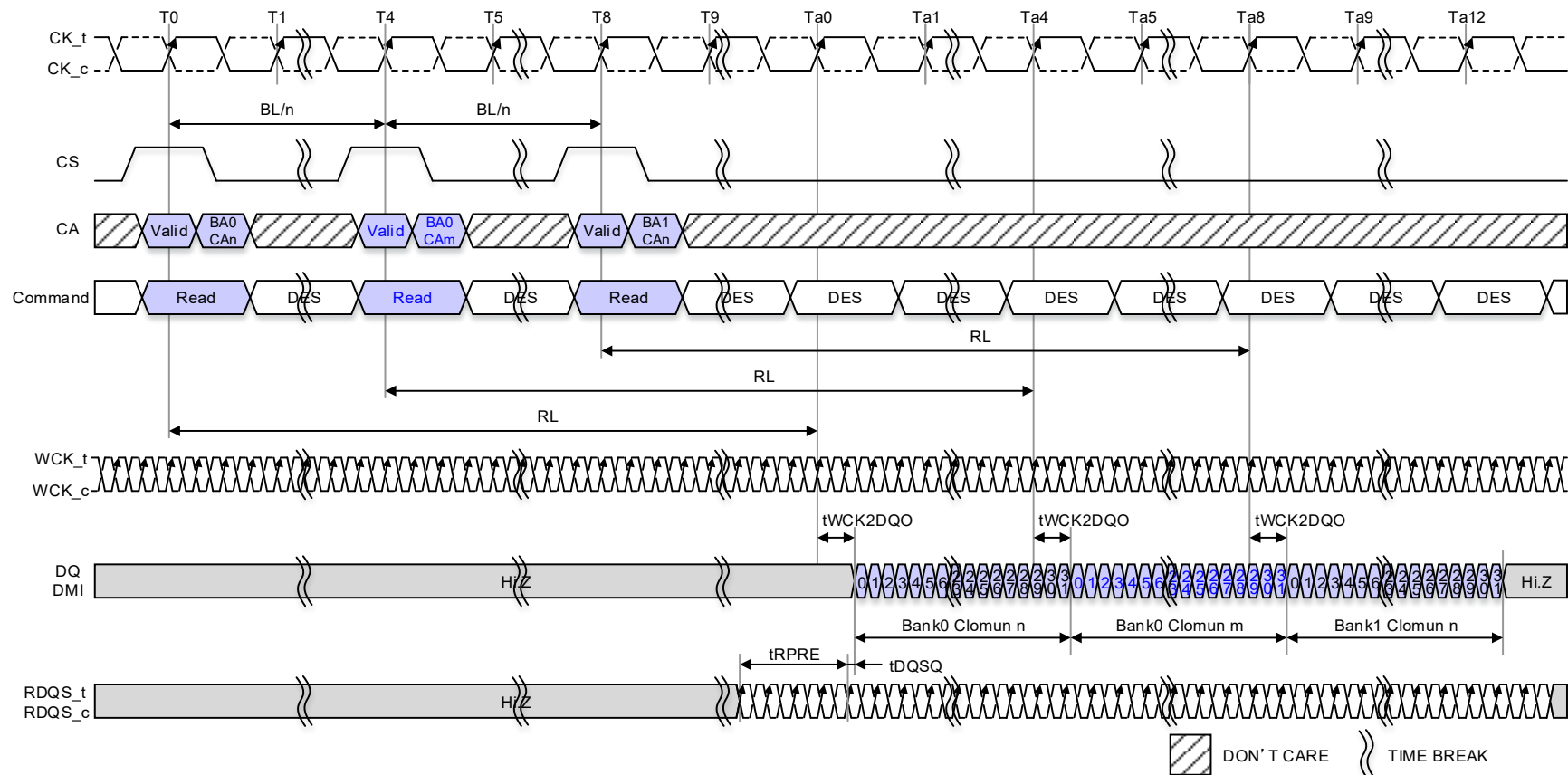
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 5 — Read Operation BG Mode, CKR (WCK vs. CK) = 4:1, BL=32

The BG Mode architecture only supports BL32 in an interleaved fashion when the WCK and CK ratio is 4:1. BL32 interleaved Reads will output the first word of DQ[15:0] after a certain latency from the Read command. The second word, consisting of DQ[31:16], will begin to be driven after an 8tWCK gap from the end of the first word. Figure 5 depicts BG mode Read operations for BL32 including the interleaving between bank groups. If correctly implemented, Read(BL16) command and Read32(BL32) commands can be mixed; however, once a Read32(BL32) command is issued, issuing Read(BL16)/Read32(BL32) command after 3 clocks is prohibited, to avoid read data conflict.

2.2.3.4 Burst Operation (cont'd)

The relationship between preceding Write32(BL32) and Write(BL16)/Write32(BL32) is the same as preceding Read32(BL32) and Read(BL16)/Read32(BL32).



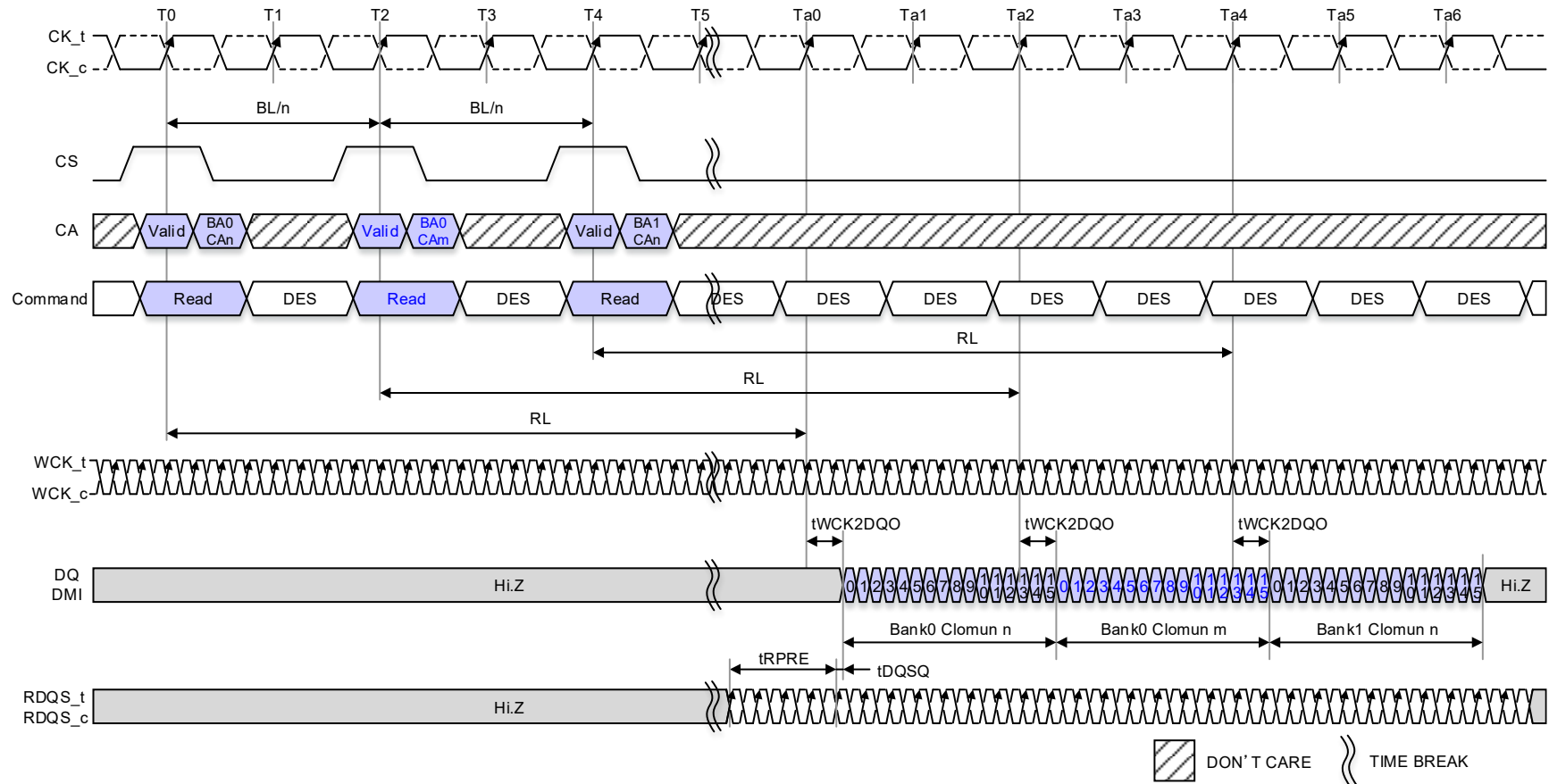
NOTE 1 MR3 OP[4:3]=01_B: 8B mode, MR18 OP[7]=0_B: CKR (WCK vs. CK)= 4:1

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 6 — Read Operation 8B mode, CKR (WCK vs. CK) = 4:1, BL=32 (not Applicable to LPDDR5X SDRAM)

2.2.3.4 Burst Operation (cont'd)



NOTE 1 MR3 OP[4:3]=10B: 16B Mode, MR18 OP[7]=0B: CKR (WCK vs. CK)= 4:1.

NOTE 2 tWCK2CK is 0ps in this instance.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 7 — Read Operation 16B Mode, CKR (WCK vs. CK) = 4:1, BL=16