

JEDEC STANDARD

Low Power Double Data Rate (LPDDR) SDRAM Standard

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Low Power Double Data Rate (LPDDR) SDRAM

(From JEDEC Board Ballot JCB-05-109B, formulated under the cognizance of the JC-42.3C Subcommittee on Parametrics.)

1 Scope

This document defines the Low Power Double Data Rate (LPDDR) SDRAM specification, including features, functionality, AC and DC characteristics, packages, and pin assignments. This scope may be expanded in future to also include other higher density devices.

The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 64 Mb through 2 Gb for x16 and x32 Low Power Double Data Rate SDRAM devices. System designs based on the required aspects of this specification will be supported by all LPDDR SDRAM vendors providing compliant devices.

This specification was created based on the DDR-I specification (JESD79) and some aspects of the DDR2 specification (JESD79-2) where shared technology suggested commonality provided benefits. Each aspect of the changes for low power operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this LPDDR SDRAM specification, replacing whole sections and incorporating the changes into Functional Description and Operation. The applicable ballots are summarized in [Table 1](#).

Table 1 — LPDDR Ballots

Item #	Ballot Number	Subject	Spec Coverage
1418.02	JC-42.3-03-183	LPDDR IO levels	Table 12 and notes
1418.04	JC-42.3-03-114	LPDDR addressing table x16	part of Table 2 except tREFI
1418.05	JC-42.3-03-184	LPDDR IDD test condition	Table 13 and notes except IDD6
1418.07	JC-42.3-03-258	AC timing parameters	Table 14 and notes
1418.08	JC-42.3-03-259	Pin capacitance	Table 11 and notes
1418.09	JC-42.3-04-035	LPDDR clock stop mode	Clock stop, pp 46, Figure 43
1418.10	JC-42.3-04-026	Modification of IDD6 definition	Table 13
1418.11	JC-42.3-04-188	LPDDR addressing table x32	part of Table 2 , x32, except tREFI
1418.12	JC-42.3-04-147	tREFI for x32 LPDDR	part of Table 2 , x32, tREFI only
1452.01	JC-42.3-04-118	LPDDR MRS and EMRS definition	Figure 6 and Figure 7
1452.02	JC-42.3-04-111	LPDDR SDRAM x16 in FBGA-60	Figure 1
1452.03	JC-42.3-04-181	LPDDR SDRAM x32 in FBGA-90	Figure 2
1563.00	JC-42.3-04-037	LPDDR initialization	pp 10; Figure 4 and Figure 5
1563.01	JC-42.3-04-038	LPDDR Deep Power Down mode	pp 45 and Figure 42
1604.01	JC-42.3-04-150A	LPDDR IV Curve	Table 17 , Figure 45 and Figure 47
1625.03	JC-42.3-04-392	LPDDR over/undershoot	Table 16 and Figure 44
1718.05	JC-42.6-07-357	LPDDR400 SDRAM AC Parameters	Table 14
1718.08	JC-42.6-07-358	LPDDR400 SDRAM TQ Pad Proposal	Table 3 , Figure 5 , description page 20, Table 14
1718.13	JC-42.6-07-264	LPDDR SDRAM 60-, 90-Ball BGA Ballouts with A13 ball	Figure 2
1718.14	JC-42.6-07-265	LPDDR SDRAM 60-, 90-Ball BGA Ballouts with additional CS#, CKE	Figure 1 and Figure 2
1718.15	JC-42.6-07-359	LPDDR SDRAM Output Driver Characteristics	Figure 7 , Table 15 , Table 17 , Table 18 , and Figure 46 .
1718.16	JC-42.6-07-360	LPDDR SDRAM address tables	Table 2
1723.02	JC-42.6-08-255	LPDDR SDRAM 1.2V Output Characteristics	LPDDR SDRAM 1.2V I/O Addendum
1718.18	JC-42.6-08-331	LPDDR tRC & tRFC definition	Table 14



2 Low-Power Double Data Rate (LPDDR) SDRAM Devices

64M = 4M x 16 (1M x 16 x 4 banks), 2M x 32 (512K x 32 x 4 banks)
128M = 8M x 16 (2M x 16 x 4 banks), 4M x 32 (1M x 32 x 4 banks)
256M = 16M x 16 (4M x 16 x 4 banks), 8M x 32 (2M x 32 x 4 banks)
512M = 32M x 16 (8M x 16 x 4 banks), 16M x 32 (4M x 32 x 4 banks)
1G = 64M x 16 (16M x 16 x 4 banks), 32M x 32 (8M x 32 x 4 banks)
2G = 128M x 16 (32M x 16 x 4 banks), 64M x 32 (16M x 32 x 4 banks)

2.1 Features

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 2, 4 or 8 (16 is optional)
- Burst Type: Sequential or Interleave
- CAS latency: 3 (2 & 4 are optional)
- Clock Stop capability during idle periods
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh and Temperature Compensated Self Refresh
- Deep Power Down Mode
- LV-CMOS compatible inputs
- VDD and VDDQ: 1.8 +/- 0.1 V

2.2 General Description

The LPDDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits
2 Gb has 2,147,483,648 bits

The LPDDR SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the LPDDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center aligned with data for WRITEs.

The LPDDR SDRAM operates from a differential clock (CK and $\overline{\text{CK}}$: the crossing of the CK going high and $\overline{\text{CK}}$ going low will be referred to as the positive edge of CK). Commands (address and control signals) are registered at every positive edge of CK. Input data is registered at both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.2 General Description (cont'd)

Read and write accesses to the LPDDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The LPDDR SDRAM provides for programmable read or write bursts of 2, 4 or 8 locations. Some vendors may offer an optional burst length of 16. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAMs, the pipelined, multibank architecture of LPDDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

An Auto Refresh mode is provided, along with a power saving Power-down mode. Self Refresh mode may have Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR) options, which allow users to achieve additional power saving. The TCSR and PASR options can be programmed via the extended mode register.

All inputs are LV-CMOS compatible. Devices will have a VDD and VDDQ supply of 1.8 V (nominal).

This datasheet includes all features and functionality required for JEDEC LPDDR SDRAM devices. Certain vendors may elect to offer a superset of this specification by offering improved timings and/or including optional features. Users benefit from knowing that any system design based on the required aspects of the specification are supported by all LPDDR SDRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

Table 2 — LPDDR SDRAM Addressing Table

Item		64 Mb	128 Mb	256 Mb	512 Mb	1 Gb		2 Gb
Number of banks		4	4	4	4	4		4
Bank Address Pins		BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1	BA0, BA1		BA0, BA1
Autoprecharge Pin		A10/AP	A10/AP	A10/AP	A10/AP	A10/AP		A10/AP
x16	Row Addresses	A0-A11	A0-A11	A0-A12	A0-A12	A0-A13		A0-A13
	Column Addresses	A0-A7	A0-A8	A0-A8	A0-A9	A0-A9		A0-A9, A11
	t_{REFI} (μs)	15.6	15.6	7.8	7.8	7.8		7.8
x32	Row Addresses	A0-A10	A0-A11	A0-A11	A0-A12	A0-A12	A0-A13	A0-A13
	Column Addresses	A0-A7	A0-A7	A0-A8	A0-A8	A0-A9	A0-A8	A0-A9
	t_{REFI} (μs)	15.6	15.6	15.6	7.8	7.8		7.8

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)
2.2 General Description (cont'd)

2.2.1 Packages

Single-die, one CS# and one CKE:

In the 60-ball x16 package, a maximum SDRAM density of 2Gb can be achieved only with 2-KByte page size and most significant address bit A13.

In the 90-ball x32 package, a maximum SDRAM density of 2Gb can be achieved either with 2-KByte page size and most significant address bit A13, or with 4-KByte page size and most significant address bit A12.

Dual-die, two CS# and two CKE:

In the 60-ball x16 package, a maximum SDRAM density of 1Gb can be achieved with most significant address bit A12.

In the 90-ball x32 package, a maximum SDRAM density of 2Gb can be achieved with most significant address bit A12.

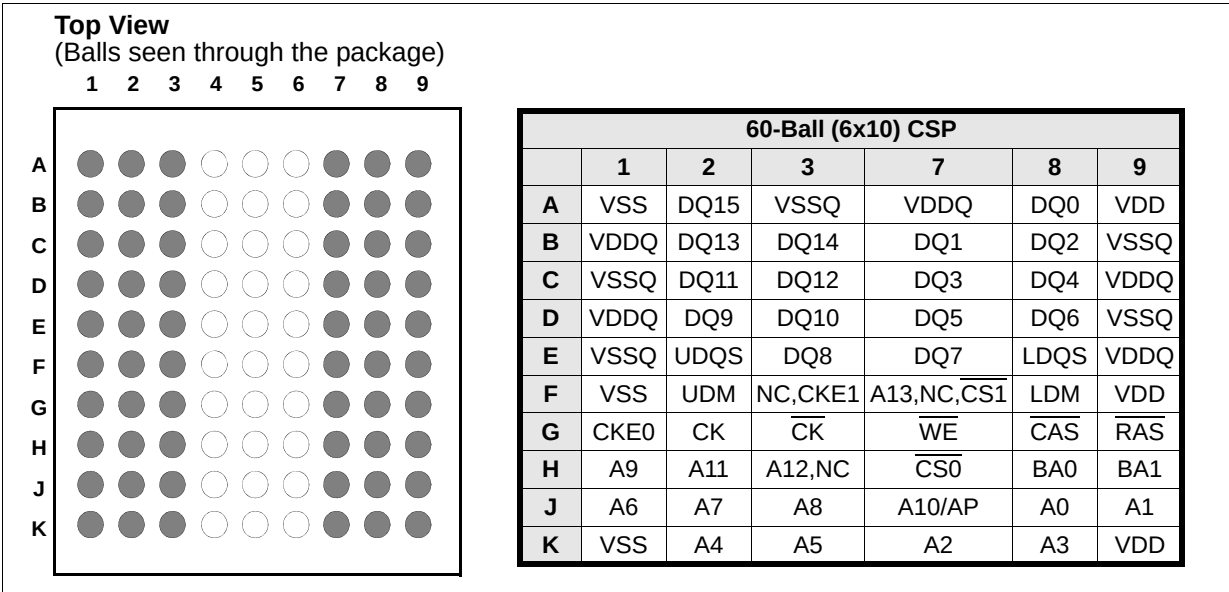


Figure 1 — Pin Configuration of x16 LPDDR SDRAM IN BGA

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.2 General Description (cont'd)

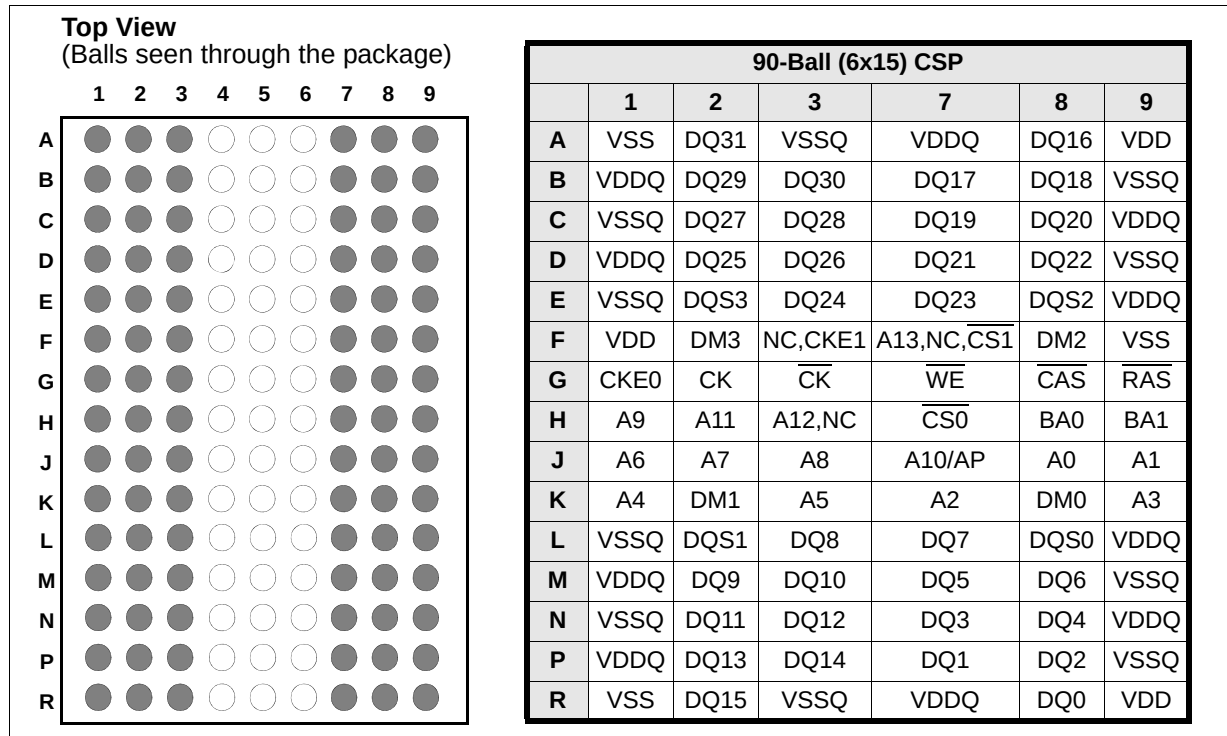


Figure 2 — Pin Configuration of x32 LPDDR SDRAM IN BGA

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)**2.2 General Description (cont'd)****Table 3 — Pin Descriptions**

Symbol	Type	Description
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Input and output data is referenced to the crossing of CK and $\overline{\text{CK}}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{\text{CK}}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, $\overline{\text{CK}}$ and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{\text{CS}}$	Input	Chip Select: $\overline{\text{CS}}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{CS}}$ is considered part of the command code.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM for x16: LDM, UDM for x32: DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ for x16: DQ0-DQ15 for x32: DQ0-DQ31	I/O	Data Bus: Input / Output
DQS for x16: LDQS, UDQS for x32: DQS0-DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
NC	—	No Connect: No internal electrical connection is present
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground
VDD	Supply	Power Supply
VSS	Supply	Ground

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)**2.2 General Description (cont'd)****Table 3 — Pin Descriptions**

Symbol	Type	Description
TPD (Test Power Down)	Input	Optional pad, Test Power Down or TPD, for test purposes only. TPD LOW is normal operation. Taking TPD HIGH asynchronously will place the die in deep power down mode. The assertion of TPD HIGH must meet all the initialization and sequencing of DPD mode
TQ	Output	Optional. Asynchronous, LVCMOS temperature output. Output logic-HIGH state when device temperature equals or exceeds 85°C. Output logic-LOW state when device temperature is less than 85°C.

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.2 General Description (cont'd)

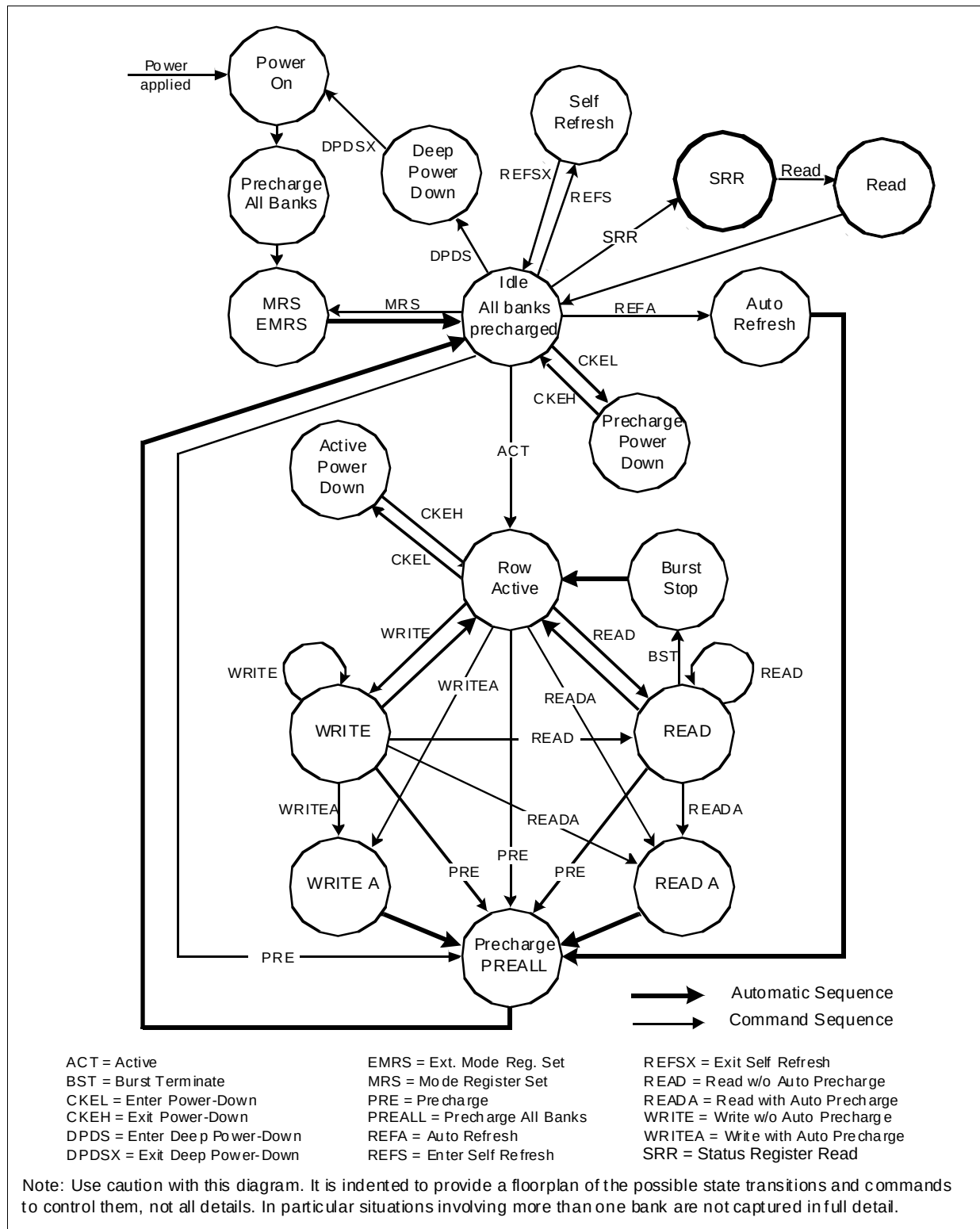


Figure 3 — Simplified State Diagram

2 Low-Power Double Data Rate (LPDDR) SDRAM Devices (cont'd)

2.3 Terminology and Definitions

The following are the definitions of the terms LPDDR200, LPDDR266, LPDDR333, LPDDR370, and LPDDR400 as used in this specification

LPDDR200: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 100 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 100 MHz clock frequency. The corresponding nominal data transfer rate is 200 Million Transfers per Second per pin (MTS).

LPDDR266: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 133 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 133 MHz clock frequency. The corresponding nominal data transfer rate is 266 MTS.

LPDDR333: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 166 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 166 MHz clock frequency. The corresponding nominal data transfer rate is 333 MTS.

LPDDR370: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 185 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 185 MHz clock frequency. The corresponding nominal data transfer rate is 370 MTS.

LPDDR400: A speed grade for LPDDR SDRAM devices. The nominal operating (clock) frequency of such devices is 200 MHz. This means that although the device operates over a range of clock frequencies, the timing specifications included in this speed grade are tailored to a 200 MHz clock frequency. The corresponding nominal data transfer rate is 400 MTS.

3 Functional Description

The LPDDR SDRAM is a high speed CMOS, dynamic random-access memory internally configured as a quad-bank DRAM. These devices contain the following number of bits:

64 Mb has 67,108,864 bits
128 Mb has 134,217,728 bits
256 Mb has 268,435,456 bits
512 Mb has 536,870,912 bits
1 Gb has 1,073,741,824 bits
2 Gb has 1,147,483,648 bits

The LPDDR SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the LPDDR SDRAM effectively consists of a single 2n-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 Initialization

LPDDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below. The Initialization Flow diagram is shown in [Figure 4](#), and the Initialization Flow sequence in [Figure 5](#).

The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Steps 1 through 11.

1. Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level
2. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock
3. There must be at least 200 μ s of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Provide NOPs or DESELECT commands for at least t_{RP} time.
6. Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
7. Using the MRS command, load the base mode register. Set the desired operating modes.
8. Provide NOPs or DESELECT commands for at least t_{MRD} time.
9. Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

3 Functional Description (cont'd)

3.1 Initialization (cont'd)

10. Provide NOP or DESELECT commands for at least t_{MRD} time.
11. The DRAM has been properly initialized and is ready for any valid command.

3 Functional Description (cont'd)

3.1 Initialization (cont'd)

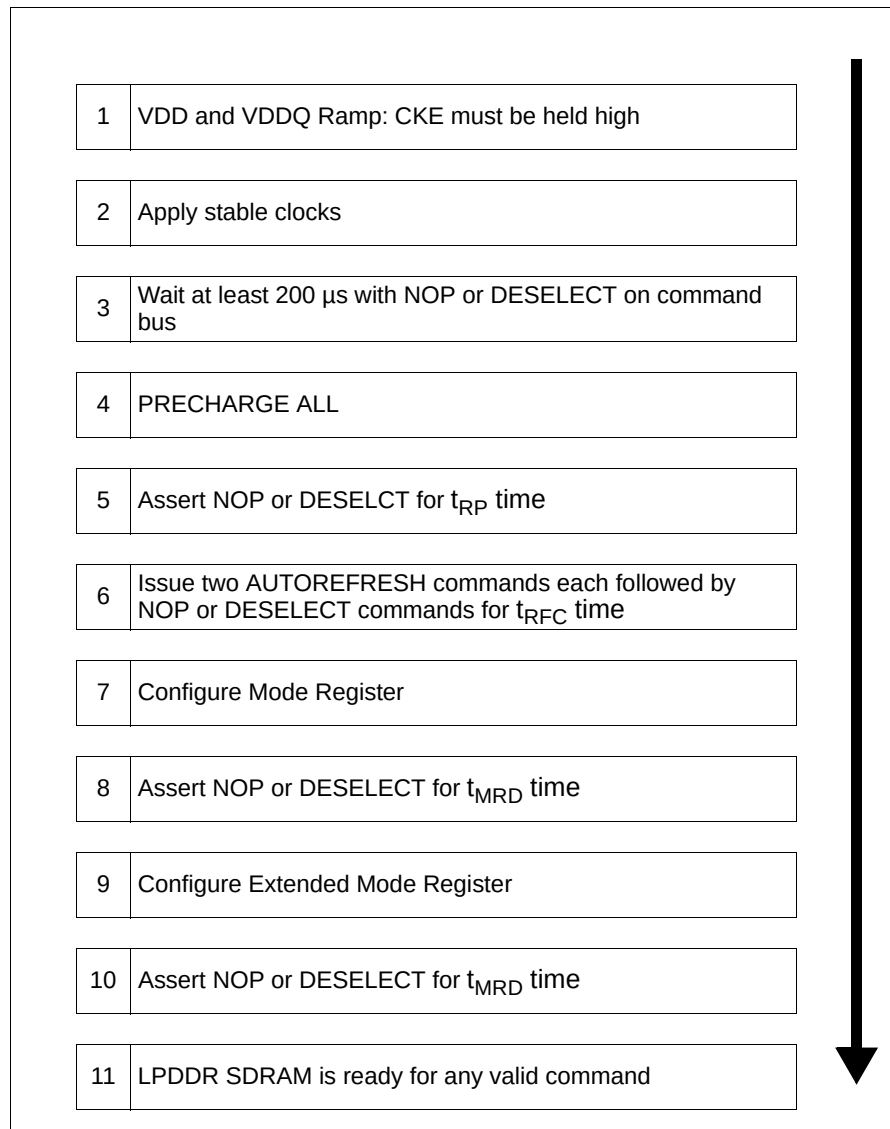
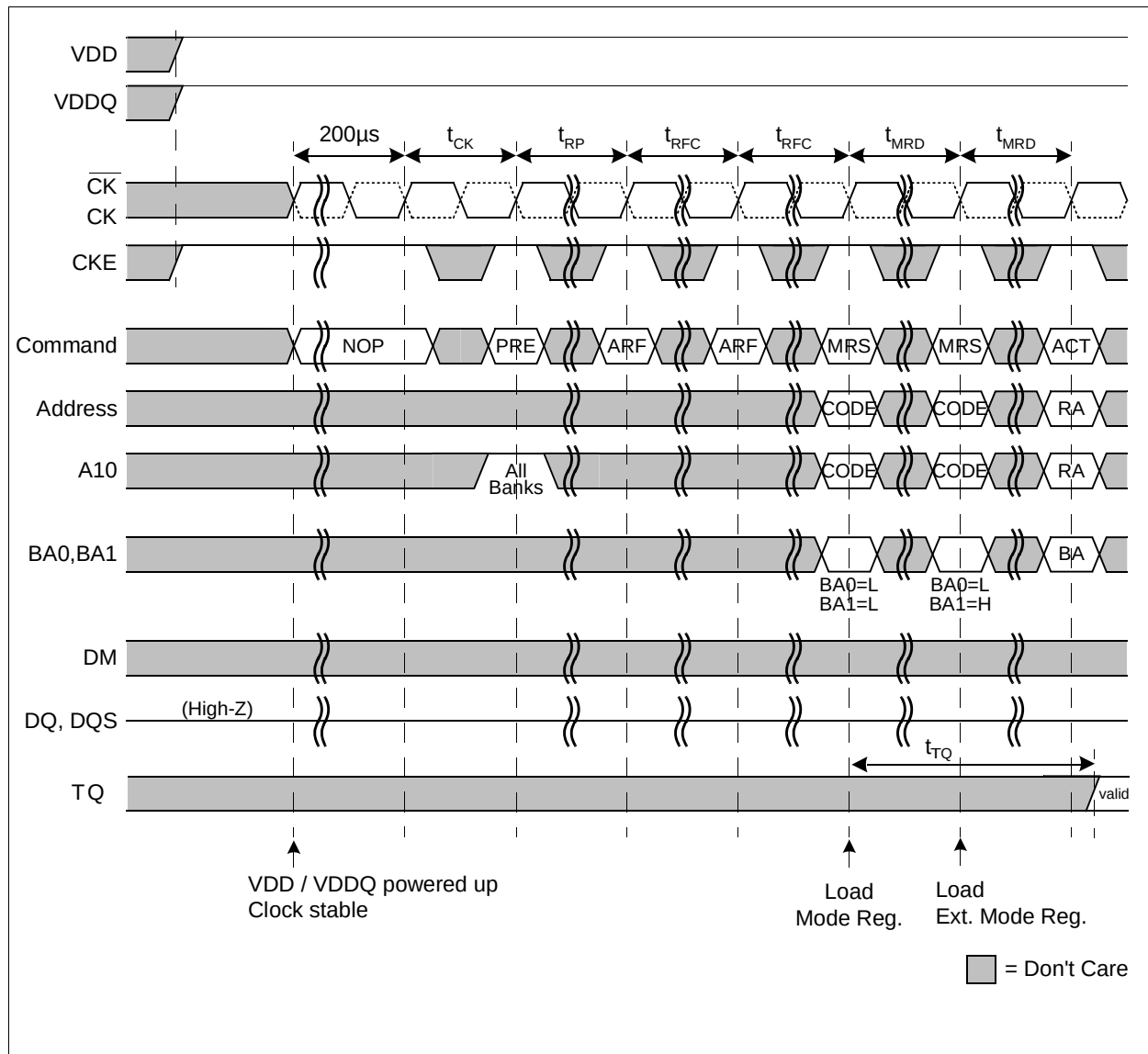


Figure 4 — Initialization Flow Diagram

3 Functional Description (cont'd)

3.1 Initialization (cont'd)



3.1.0.1 TQ Signal Initialization

During device initialization the TQ signal output will be invalid until t_{TQ} after the first MRS command. Following t_{TQ} the TQ signal will output logic-HIGH when the device temperature is greater than, or equal to, 85°C, and logic-LOW when the device temperature is less than 85°C. There is no high-impedance state for this output signal.

3.2 Register Definition

3.2.1 Mode Register

The Mode Register is used to define the specific mode of operation of the LPDDR SDRAM. This definition includes the definition of a burst length, a burst type, a CAS latency as shown in [Figure 6](#).

3 Functional Description (cont'd)

3.2 Register Definition (cont'd)

The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device goes into Deep Power-Down mode, or the device loses power.

Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

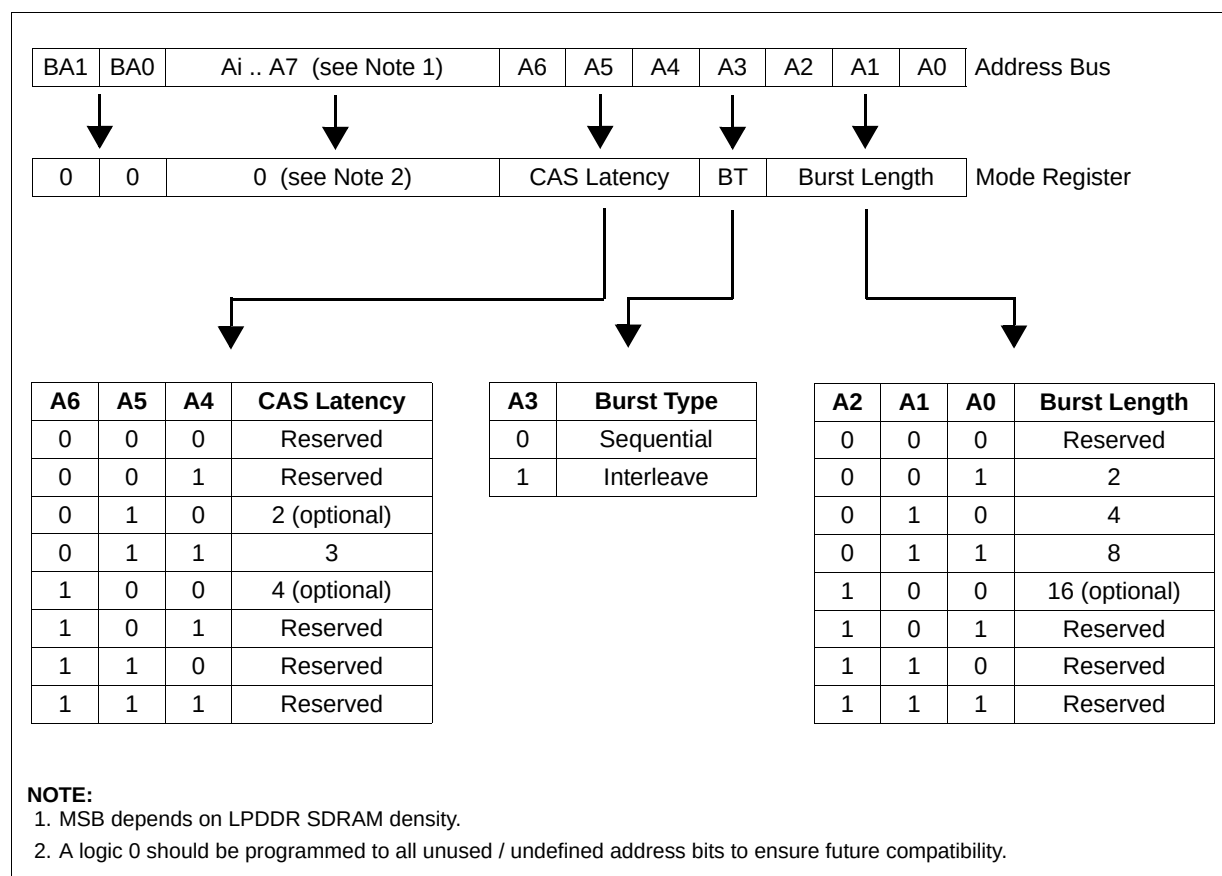


Figure 6 — Mode Register Definition

3.2.1.1 Burst Length

Read and write accesses to the LPDDR SDRAM are burst oriented, with the burst length being set as in [Table 6](#), and the burst order as in [Table 4](#).

The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types. A burst length of 16 is optional and some vendors may choose to implement it.

Table 4 — Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS				ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION)	
	A3	A2	A1	A0	SEQUENTIAL	INTERLEAVED
2	0				0 - 1	0 - 1
	1				1 - 0	1 - 0

3 Functional Description (cont'd)

3.2 Register Definition (cont'd)

Table 4 — Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS				ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION)	
	A3	A2	A1	A0	SEQUENTIAL	INTERLEAVED
4			0	0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
			0	1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
			1	0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
			1	1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8		0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
		0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
		0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
		0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
		1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
		1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
		1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
		1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

NOTES:

1. 16-word burst length is optional.
2. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
3. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
4. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
5. For the optional burst length of sixteen, A4-An selects the sixteen data element block; A0-A3 selects the first access within the block.
6. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8 and A4-An when the burst length is set to 16 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is/are used to select the starting location within the block. The programmed burst length applies to both read and write bursts.