

JEDEC STANDARD

GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD

JESD212C.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD

(From JEDEC Board Ballot JCB-16-53, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 SCOPE

This document defines the Graphics Double Data Rate 5 (GDDR5) Synchronous Graphics Random Access Memory (SGRAM) standard, including features, functionality, package, and pin assignments. This scope may be expanded in future to also include other higher density devices.

The purpose of this Standard is to define the minimum set of requirements for JEDEC standard compatible 512 Mb through 8 Gb x32 GDDR5 SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR5 SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR5 standard such as AC timings and capacitance values were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics.

This standard was created based on the DDR Standard (JESD79) and some aspects of the GDDR4 Standard (JESD21C - 3.11.5.8). Each aspect of the changes for high speed operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this GDDR5 SGRAM document, replacing whole sections and incorporating the changes into Functional Description and Operation.

2 GDDR5 SGRAM STANDARD OVERVIEW

512 Mb	= 16 Mb x 32	(2 Mb x 32 x 8 banks)	/	32 Mb x 16	(4 Mb x 16 x 8 banks)
1 Gb	= 32 Mb x 32	(2 Mb x 32 x 16 banks)	/	64 Mb x 16	(4 Mb x 16 x 16 banks)
2 Gb	= 64 Mb x 32	(4 Mb x 32 x 16 banks)	/	128 Mb x 16	(8 Mb x 16 x 16 banks)
4 Gb	= 128 Mb x 32	(8 Mb x 32 x 16 banks)	/	256 Mb x 16	(16 Mb x 16 x 16 banks)
8 Gb	= 256 Mb x 32	(16 Mb x 32 x 16 banks)	/	512 Mb x 16	(32 Mb x 16 x 16 banks)

2.1 FEATURES

- Single ended interface for data, address and command
- Quarter data-rate differential clock inputs CK_t/CK_c for ADD/CMD
- Two half data-rate differential clock inputs WCK_t/WCK_c, each associated with two data bytes (DQ, DBI_n, EDC)
- Double Data Rate (DDR) data (WCK)
- Single Data Rate (SDR) command (CK)
- Double Data Rate (DDR) addressing (CK)
- 8 or 16 internal banks
- 4 bank groups for t_{CCDL} = 3 t_{CK} and 4 t_{CK}
- 8n prefetch architecture: 128/256 bit per array read or write access
- Burst length: 8 only
- Programmable CAS latency: 5 to 36 t_{CK}
- Programmable WRITE latency: 1 to 7 t_{CK}
- WRITE Data mask function via address bus (single/double byte mask)
- Data bus inversion (DBI) and address bus inversion (ABI)
- Input/output PLL/DLL on/off mode
- Address training: address input monitoring by DQ pins
- WCK2CK clock training with phase information by EDC pins
- Data read and write training via READ FIFO
- READ FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO by WRTR command
- Consecutive read of READ FIFO by RDTR command
- Read/Write data transmission integrity secured by cyclic redundancy check (CRC-8)
- READ/WRITE EDC on/off mode
- Programmable EDC hold pattern for CDR
- Programmable CRC READ latency = 0 to 4 t_{CK}
- Programmable CRC WRITE latency = 7 to 14 t_{CK}
- Low Power modes
- RDQS mode on EDC pin
- Optional on-chip temperature sensor with read-out
- Auto and self refresh modes
- Auto precharge option for each burst access
- 32ms, auto refresh (8k/16k cycles)
- Temperature sensor controlled self refresh rate
- Optional Partial Array Self Refresh (PASR)
- Optional Per-Bank Refresh (REFPB)
- Optional digital t_{RAS} lockout
- On-die termination (ODT); nominal values of 60 ohm and 120 ohm
- Pseudo open drain (POD-15 or POD-135) compatible outputs (40 ohm pulldown, 60 ohm pullup)
- ODT and output drive strength auto-calibration with external resistor ZQ pin (120 ohm)
- Programmable termination and driver strength offsets
- Selectable external or internal VREF for data inputs; programmable offsets for internal VREF
- Separate external VREF for address / command inputs
- Vendor ID, FIFO depth and Density info fields for identification
- x32/x16 mode configuration set at power-up with EDC pin
- Mirror function with MF pin
- Boundary scan function with SEN pin
- 1.5V +/- 0.045V or 1.35V +/- 0.0405V supply for device operation (VDD)
- 1.5V +/- 0.045V or 1.35V +/- 0.0405V supply for I/O interface (VDDQ)
- 170 ball BGA package

2.2 FUNCTIONAL DESCRIPTION

The GDDR5 SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. GDDR5 devices contain the following number of bits:

512 Mb has 536,870,912 bits and eight banks
1 Gb has 1,073,741,824 bits and sixteen banks
2 Gb has 2,147,483,648 bits and sixteen banks
4 Gb has 4,294,967,296 bits and sixteen banks
8 Gb has 8,589,934,592 bits and sixteen banks

The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high-speed operation. The device can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n-prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers at the I/O pins.

The device operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

GDDR5 replaces the pulsed strobes (WDQS and RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK_t/WCK_c) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

Read and write accesses to the device are burst oriented; an access starts at a selected location and consists of a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising CK_c edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK_c edge are used to select the bank and the column location for the burst access.

This specification includes all features and functionality required for JEDEC GDDR5 SGRAM devices. Users benefit from knowing that any system design based on the required aspects of the specification are supported by all GDDR5 SGRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

2.3 DEFINITION OF SIGNAL STATE TERMINOLOGY

The device will be operated in both ODT Enable (terminated) and ODT Disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT Enable mode. ODT Disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT Enable mode can not be guaranteed for a short period of time, i.e., during power up.

Following are four terminologies defined for the state of a device (GDDR5 SGRAM or controller) pin during operation. The state of the bus will be determined by the combination of the device pins connected to the bus in the system. For example in GDDR5 it is possible for the SGRAM pin to be tristated while the controller pin is High or ODT. In both cases the bus would be High if the ODT is enabled. For details on the GDDR5 SGRAM pins and their function see Sections 9.1 and 9.2.

Device pin signal level:

- High: A device pin is driving the Logic "1" state.
- Low: A device pin is driving the Logic "0" state.
- Hi-Z: A device pin is tristate.
- ODT: A device pin terminates with ODT setting, which could be terminating or tristate depending on Mode Register setting.

Bus signal level:

- High: One device on bus is High and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VDDQ
- Low: One device on bus is Low and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VOL(DC) if ODT was enabled, or VSSQ if Hi-Z.
- Hi-Z: All devices on bus are Hi-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: At least one device on bus is ODT and all others are Hi-Z. The voltage level on the bus would be nominally VDDQ.

2.4 CLOCKING

The device operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

GDDR5 uses a DDR data interface and an 8n-prefetch architecture. The data interface uses two differential forwarded clocks (WCK_t/WCK_c). DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c. WCK_t and WCK_c are continuously running and operate at twice the frequency of the command/address clock (CK_t/CK_c).

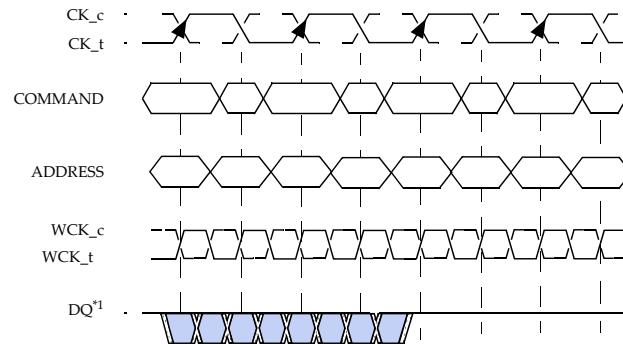


Figure 1 — GDDR5 Clocking and Interface Relationship

NOTE Figure 1 shows the relationship between the data rate of the buses and the clocks and is not a timing diagram.

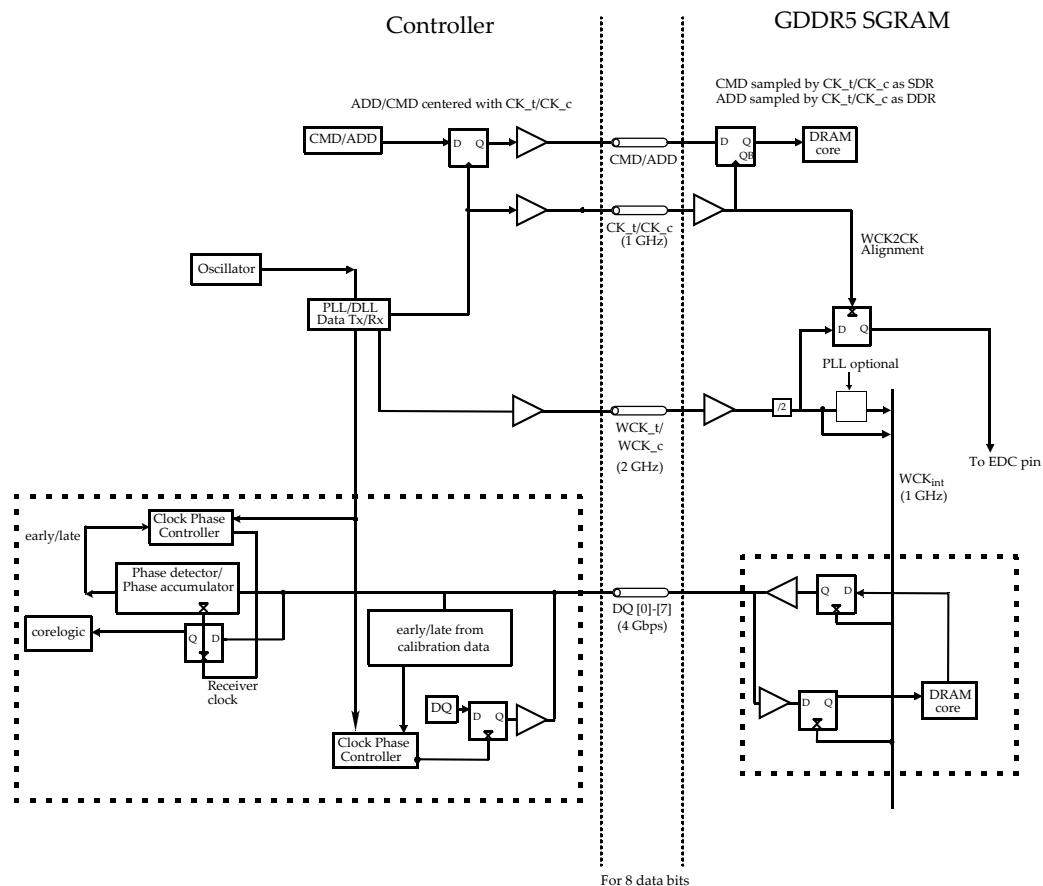


Figure 2 — Block Diagram of an Example Clock System

3 INITIALIZATION

3.1 POWER-UP SEQUENCE

GDDR5 SGRAMs must be powered up and initialized in a predefined manner as shown in Figure 3. Operational procedures other than those specified may result in undefined operation. The Mode Registers do not have RESET default values, except for ABI_n, ADD/CMD termination, and the EDC hold pattern. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

Step	
1	Apply power to VDD
2	Apply power to VDDQ at same time or after power is applied to VDD
3	Apply VREFC and VREFD at same time or after power is applied to VDDQ
4	After power is stable, provide stable clock signals CK _t /CK _c
5	Assert and hold RESET _n low to ensure all drivers are in Hi-Z and all active terminations are off. Assert and hold NOP command.
6	Wait a minimum of 200μs.
7	If boundary scan mode is necessary, SEN can be asserted HIGH to enter boundary scan mode. Boundary scan mode must be entered directly after power-up while RESET _n is low. Once boundary scan is executed, power-up sequence should be followed.
8	Set CKE _n for the desired ADD/CMD ODT settings, then bring RESET _n High to latch in the logic state of CKE _n , t _{ATS} and t _{ATH} must be met during this procedure. See Table 1 for the values and logic states for CKE _n . The rising edge of RESET _n will determine x32 mode or x16 mode depending on the state of EDC1(EDC2 when MF=1). In normal x32 mode, EDC1 has to be sustained HIGH until RESET _n is HIGH. See Table 70 for the values and logic states for EDC1(EDC2 when MF=1).
9	Bring CKE _n Low after t _{ATH} is satisfied
10	Wait at least 200μs referenced from the beginning of t _{ATS}
11	Issue at least 2 NOP commands
12	Issue a PRECHARGE ALL command followed by NOP commands until t _{RP} is satisfied
13	Issue MRS command to MR15. Set the device into address training mode (optional)
14	Complete address training (optional)
15	Issue MRS command to read the Vendor ID
16	Issue MRS command to set WCK01 _t /WCK01 _c and WCK23 _t /WCK23 _c termination values
17	Provide stable clock signals WCK01 _t /WCK01 _c and WCK23 _t /WCK23 _c
18	Issue MRS commands to the mode registers in any order. Issue MRS commands to use PLL/DLL or not and select the position of a WCK/CK phase detector. The use of PLL/DLL and the position of a phase detector must be set before WCK2CK training. t _{MRD} must be met during this procedure. WLMrs, CLMrs, CRCWL and CRCRL must be programmed before WCK2CK training.
19	Issue two REFRESH commands followed by NOP until t _{RFC} is satisfied. GDDR5 SGRAMs may optionally require 500 us before the first REFRESH command may be issued. Vendor datasheets should be consulted for specifics.
20	After any necessary GDDR5 training sequences such as WCK2CK training, READ training (LDFF, RDTR) and WRITE training (WRTR, RDTR), the device is ready for operation.

Figure 3 — GDDR5 Power-up Sequence

3.1 POWER-UP SEQUENCE (cont'd)

Table 1 — Address and Command Termination

CKE_n at RESET_n high transition	VALUE (OHMS)
Low	$ZQ/2 = 60\text{ Ohms}$
High	$ZQ = 120\text{ Ohms}$

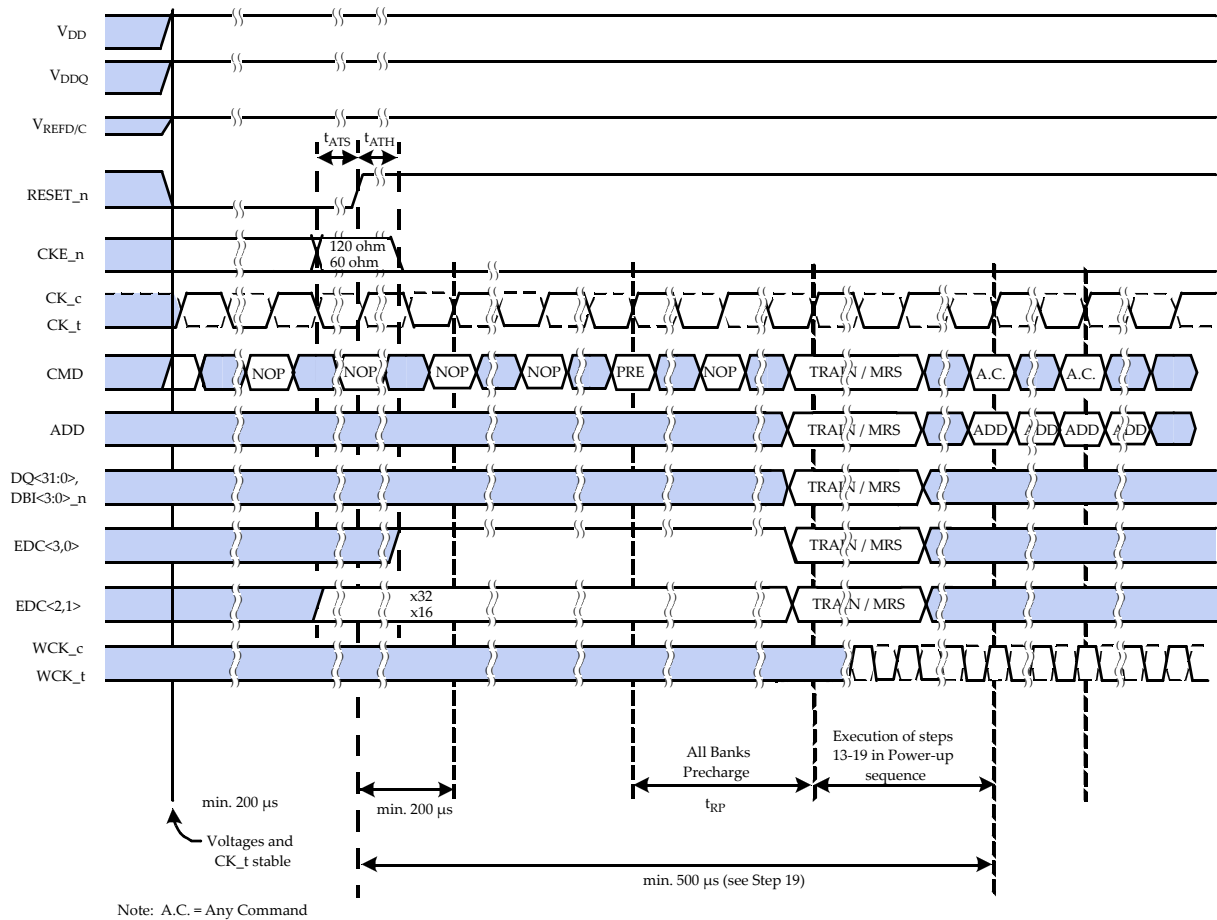
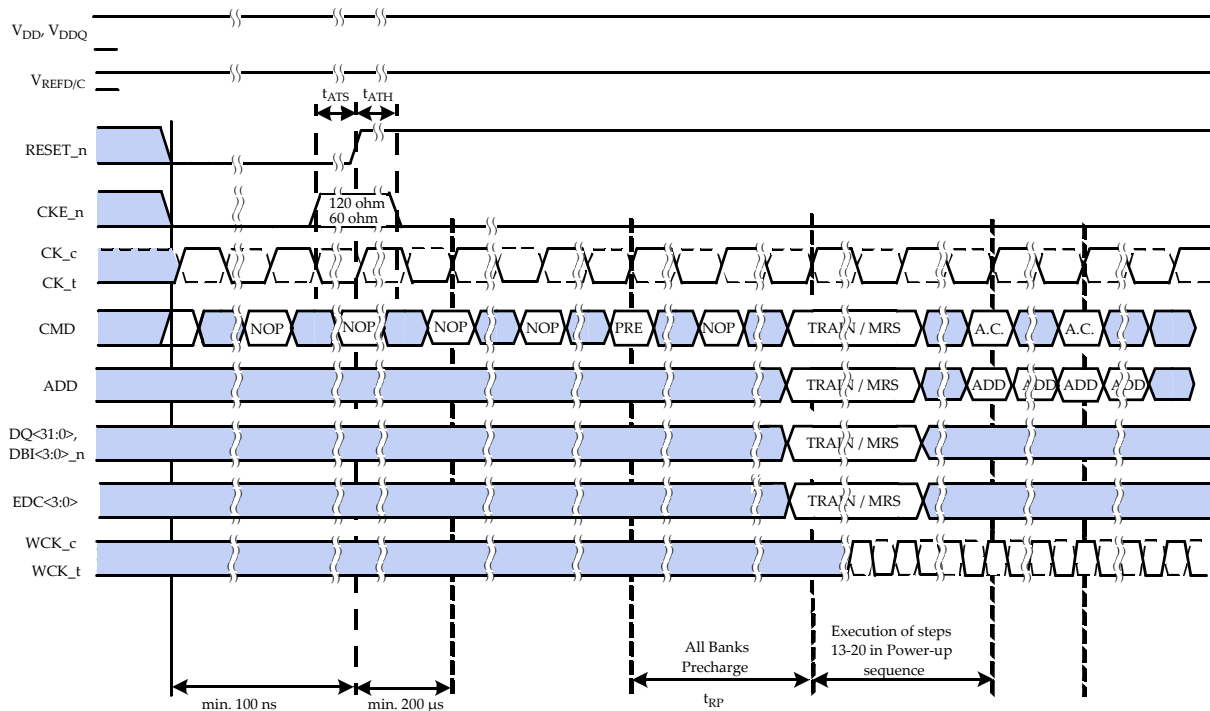


Figure 4 — GDDR5 SGRAM Power-up Initialization

3.2 INITIALIZATION WITH STABLE POWER

The following sequence is required for reset subsequent to power-up initialization. This requires that the power has been stable within the specified VDD and VDDQ ranges since power-up initialization (see Figure 5):

- 1) Assert RESET_n Low anytime when reset is needed.
- 2) Hold RESET_n Low for minimum 100ns. Assert and hold NOP command.
- 3) Set CKE_n for the desired ADD/CMD ODT settings, then bring RESET_n High to latch in the logic state of CKE_n; t_{ATS} and t_{ATH} must be met during this procedure. Keep EDC1 (MF=0) / EDC2 (MF=1) at the same logic level as during power-up initialization as device functionality is not guaranteed if the I/O width has changed.
- 4) Continue with step 9 of the power-up initialization sequence.



Notes: 1. A.C. = Any Command

2. Device functionality is not guaranteed if x32/x16 mode is not the same as during power-up initialization.

Figure 5 — Initialization with Stable Power

3.3 VENDOR ID

GDDR5 SGRAMs are required to include a Vendor ID feature that allows the controller to receive information from the device to differentiate between different vendors and different devices using a software algorithm.

When the Vendor ID function is enabled the device will provide its Manufacturers Vendor Code on bits [3:0] as shown in Table 2; Revision Identification on bits [7:4]; Density for 512 Mb - 4 Gb is provided on the lower density bits [9:8] as shown in Table 3 with bits [13:12] added for 8 Gb density. The FIFO Depth is provided on bits [11:10] as shown in Table 4. Bits [15:14] are RFU.

Vendor ID is part of the INFO field of Mode Register 3 (MR3) and is selected by issuing a MODE REGISTER SET command with MR3 bit A6 set to 1, and bit A7 set to 0. MR3 bits A0-A5 and A8-A11 are set to the desired values. Additional information can optionally be provided by the vendor using the vendor specific settings on the INFO field and will follow the same protocol as vendor ID unless explicitly stated in the vendor data sheet.

The Vendor ID will be driven onto the DQ bus after the MRS command that sets bits A6 to 1 and A7 to 0. The DQ bus will be continuously driven until an MRS command sets MR3 A6 and A7 back to 0 to disable the INFO field or to another valid state for the INFO field if the INFO field includes support for additional vendor specific information. The DQ bus will be in ODT state after $t_{WRIDOFF}$ (max). The code can be sampled by the controller after waiting t_{WRIDON} (max) and before $t_{WRIDOFF}$ (min). DBI is not enabled or ignored during all Vendor ID operations. Table 5 shows the mapping of the Vendor ID info to the physical DQs. The 16 bits of Vendor ID are sent on Byte 0 and 2 when MF=0. When MF=1 the 16 bits are sent on Byte 1 and 3. Optionally the vendor may replicate the data on the other 2 bytes when in x32 mode. Byte 0 would be replicated on Byte 1 and Byte 2 would be replicated on Byte 3 when MF=0. When MF=1, Byte 1 would be replicated on Byte 0 and Byte 3 would be replicated on Byte 2. The EDC hold pattern is continuously driven on the EDC pins provided a stable WCK clock is applied.

Table 2 — Manufacturers Vendor Code

Manufacturers ID	Bit 3	Bit 2	Bit 1	Bit 0	Name of Company
0	0	0	0	0	Reserved
1	0	0	0	1	Samsung
2	0	0	1	0	Qimonda
3	0	0	1	1	Elpida
4	0	1	0	0	Etron
5	0	1	0	1	Nanya
6	0	1	1	0	Hynix
7	0	1	1	1	ProMOS
8	1	0	0	0	Winbond
9	1	0	0	1	ESMT
A	1	0	1	0	Reserved
B	1	0	1	1	Reserved
C	1	1	0	0	Reserved
D	1	1	0	1	Reserved
E	1	1	1	0	Reserved
F	1	1	1	1	Micron

3.3 VENDOR ID (cont'd)

Table 3 — Density

Bit 13	Bit 12	Bit 9	Bit 8	Density
0	0	0	0	512 Mb
0	0	0	1	1 Gb
0	0	1	0	2 Gb
0	0	1	1	4 Gb
0	1	0	0	8 Gb
0	1	0	1	RFU
0	1	1	0	RFU
0	1	1	1	RFU
1	0	0	0	8 Gb
1	0	0	1	RFU
1	0	1	0	RFU
1	0	1	1	RFU
1	1	0	0	512 Mb
1	1	0	1	1 Gb
1	1	1	0	2 Gb
1	1	1	1	4 Gb

NOTE For 512 Mb - 4 Gb densities bits 9 and 8 are the only bits required for proper identification of density, and bits 13 and 12 either driven High or Low. Starting from the 8 Gb density bits 13 and 12 are required for proper identification of density.

Table 4 — FIFO Depth

Bit 11	Bit 10	FIFO Depth
0	0	4
0	1	5
1	0	6
1	1	RFU

Table 5 — Vendor ID to DQ Mapping

Bit								
MF=0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
MF=1	DQ31	DQ30	DQ29	DQ28	DQ27	DQ26	DQ25	DQ24
Feature								
Bit								
MF=0	DQ23	DQ22	DQ21	DQ20	DQ19	DQ18	DQ17	DQ16
MF=1	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8
Feature								

3.3 VENDOR ID (cont'd)

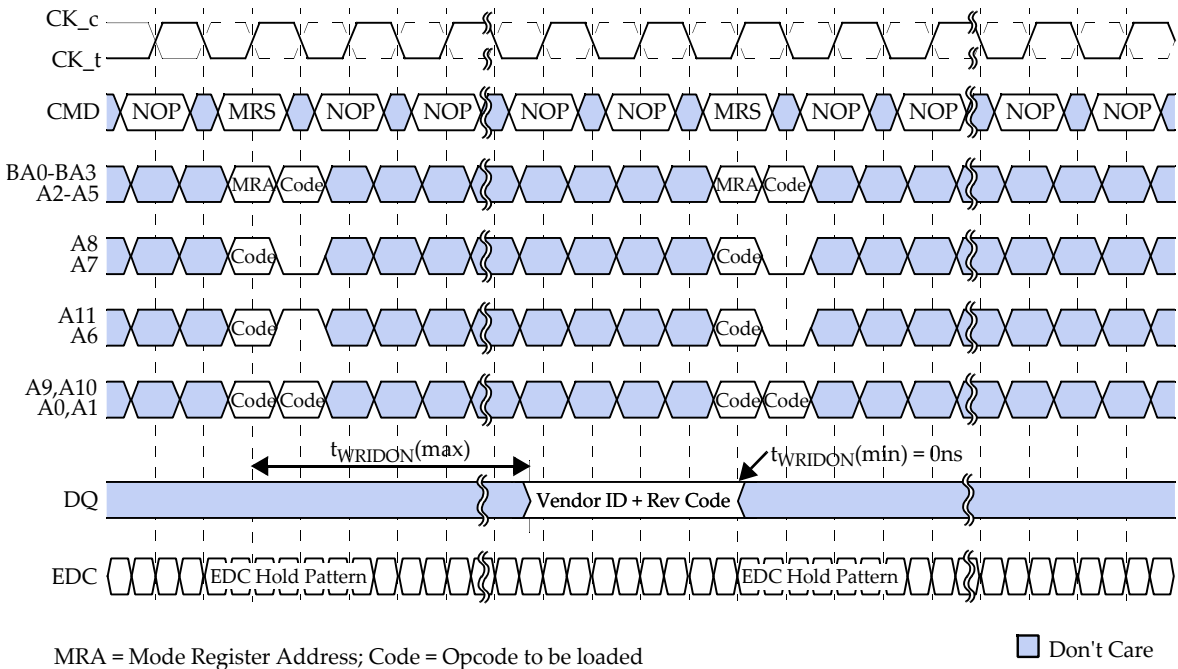


Figure 6 – Vendor ID Timing Diagram

4 ADDRESS

4.1 ADDRESSING

GDDR5 SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 6. The addresses should be provided to the device in two parts; the first half is latched on the rising edge of CK_t along with the command pins such as RAS_n, CAS_n and WE_n; the second half is latched on the next rising edge of CK_c.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 6 — Address Pairs

Clock									
Rising CK _t	BA3	BA2	BA1	BA0	(A12)	A11	A10	A9	A8
Rising CK _c	A3	A4	A5	A2	(A13)	A6	A0	A1	A7
NOTE 1 Address pin A12 is required only for 2 Gb and higher densities. NOTE 2 Address pin A13 is required only for 4 Gb and 8 Gb densities.									

GDDR5 addressing includes support for 512 Mb - 8 Gb densities. For all densities two modes are supported (x32 mode or x16 mode). x32 and x16 modes differ only in the number of valid column addresses, as shown in Table 7.

Table 7 — Addressing Scheme

	512 Mb		1 Gb		2 Gb	
	x32 mode	x16 mode	x32 mode	x16 mode	x32 mode	x16 mode
Row address	A0~A11	A0~A11	A0~A11	A0~A11	A0~A12	A0~A12
Column address	A0~A5	A0~A6	A0~A5	A0~A6	A0~A5	A0~A6
Bank address	BA0~BA2	BA0~BA2	BA0~BA3	BA0~BA3	BA0~BA3	BA0~BA3
Autoprecharge	A8	A8	A8	A8	A8	A8
Page Size	2K	2K	2K	2K	2K	2K
Refresh	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	16K/32ms	16K/32 ms
Refresh period	3.9 μs	3.9 μs	3.9 μs	3.9 μs	1.9 μs	1.9 μs

	4 Gb		8 Gb	
	x32 mode	x16 mode	x32 mode	x16 mode
Row address	A0~A13	A0~A13	A0~A13	A0~A13
Column address	A0~A5	A0~A6	A0~A6	A0~A7
Bank address	BA0~BA3	BA0~BA3	BA0~BA3	BA0~BA3
Autoprecharge	A8	A8	A8	A8
Page Size	2K	2K	4K	4K
Refresh	16K/32 ms	16K/32 ms	16K/32 ms	16 K/32 ms
Refresh period	1.9 μs	1.9 μs	1.9 μs	1.9 μs

NOTE For complete details on refresh refer to the vendor's datasheets for values for refresh interval, refresh period and t_{RFC} as t_{RFC} will scale with density and is vendor specific.

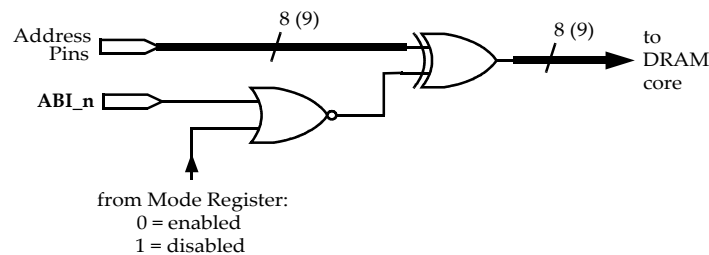
4.2 ADDRESS BUS INVERSION (ABI)

Address Bus Inversion (ABI) reduces the power requirements on address pins, as the no. of address lines driving a low level can be limited to 4 (512 Mb, 1 Gb) or 5 (2 Gb, 4 Gb, 8 Gb).

The Address Bus Inversion function is associated with the electrical signalling on the address lines between a controller and the GDDR5 SGRAM, regardless of whether the information conveyed on the address lines is a row or column address, a mode register op-code, a data mask, or any other pattern.

The ABI_n input is an active Low double data rate (DDR) signal and sampled by the device at the rising edge of CK_t and the rising edge of CK_c along with the address inputs.

Once enabled by the corresponding ABI Mode Register bit, the device will invert the pattern received on the address inputs in case ABI_n was sampled Low, or leave the pattern non-inverted in case ABI_n was sampled High, as shown in Figure 7.



NOTE bus width is 8 when A12/A13 pin is not present, and 9 when A12/A13 pin is present

Figure 7 — Example of Address Bus Inversion Logic

The flow diagram in Figure 8 illustrates the ABI operation. The controller decides whether to invert or not invert the data conveyed on the address lines. The device has to perform the reverse operation based on the level of the ABI_n pin. Address input timing parameters are only valid with ABI being enabled and a maximum of 4 or 5 address inputs driven Low.

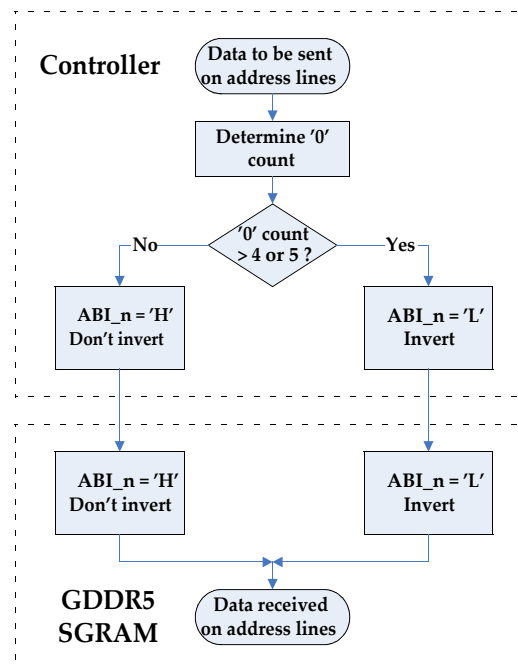


Figure 8 — Address Bus Inversion (ABI) Flow Diagram

4.3 BANK GROUPS

For GDDR5 SGRAM devices operating at frequencies above a certain threshold (f_{CKBG}), the activity within a bank group must be restricted to ensure proper operation of the device. The 8 or 16 banks in the device are divided into four bank groups. The bank groups feature is controlled by bits A10 and A11 in Mode Register 3 (MR3). The assignment of the banks to the bank groups is shown in Table 8.

Table 8 — Bank Groups

Bank	Addressing				512 Mb	1 Gb - 8 Gb
	BA3	BA2	BA1	BA0	8 banks	16 banks
0	0	0	0	0	Group A	Group A
1	0	0	0	1		
2	0	0	1	0	Group B	
3	0	0	1	1		
4	0	1	0	0	Group C	Group B
5	0	1	0	1		
6	0	1	1	0	Group D	
7	0	1	1	1		
8	1	0	0	0		Group C
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		Group D
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

These bank groups allow the specification of different command delay parameters depending on whether back-to-back accesses are to banks within one bank group or across bank groups as shown in Table 9.

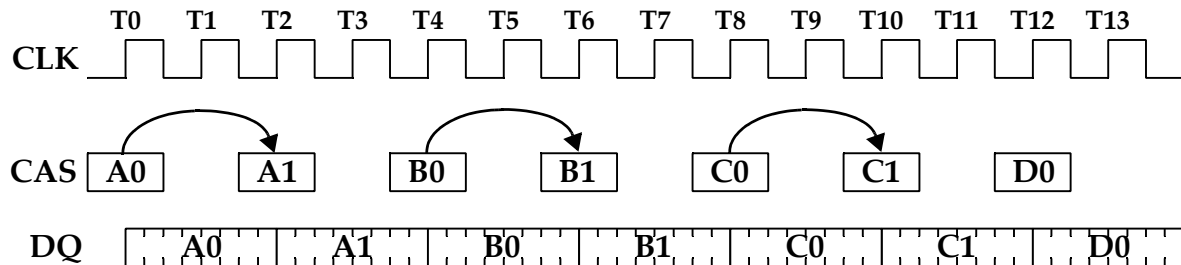
Table 9 — Command Sequences Affected by Bank Groups

Command Sequence	Corresponding AC Timing Parameter			Notes
	Bank Groups Disabled	Bank Groups Enabled		
		Accesses to different bank groups	Accesses within the same bank group	
ACTIVE to ACTIVE	t _{RRDS}	t _{RRDS}	t _{RRDL}	
WRITE to WRITE	t _{CCDS}	t _{CCDS}	t _{CCDL}	
READ to READ	t _{CCDS}	t _{CCDS}	t _{CCDL}	
Internal WRITE to READ	t _{WTRS}	t _{WTRS}	t _{WTRL}	
READ to PRECHARGE	t _{RTPS}	1 t _{ck}	t _{RTPL}	1
NOTE 1 Parameters t _{RTPS} and t _{RTPL} apply only when READ and PRECHARGE go to the same bank; use t _{RTPS} when BG are disabled, and t _{RTPL} when BG are enabled.				

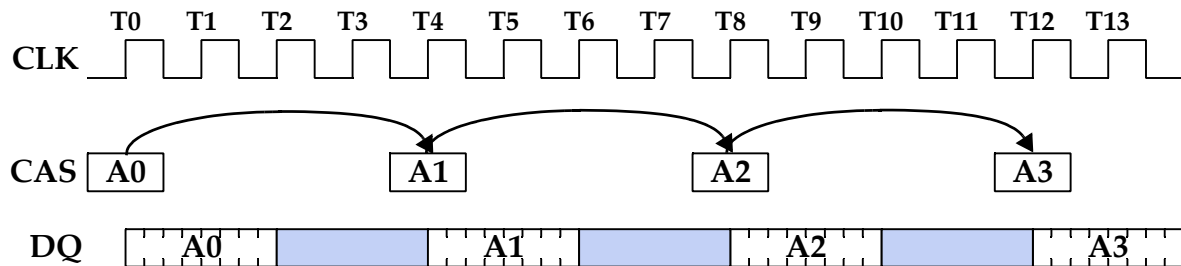
4.3 BANK GROUPS (cont'd)

Figure 9 shows back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters.

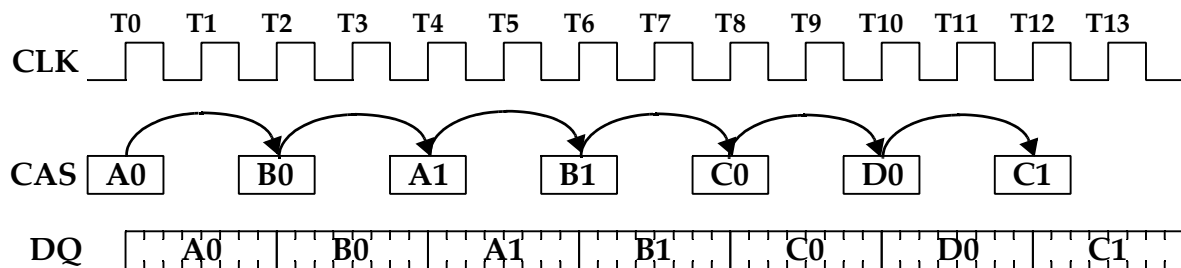
Example 1 (Bank Groups disabled): $t_{CCDS} = 2 * t_{CK}$



Example 2: (Bank Groups enabled): $t_{CCDL} = 4 * t_{CK}$



Example 3: (Bank Groups enabled): $t_{CCDS} = 2 * t_{CK}$



NOTE 1 Column accesses are to open banks, and t_{RCD} has been met.

NOTE 2 CL = 0 assumed

NOTE 3 Ax, Bx, Cx, Dx: accesses to bank groups A, B, C or D, respectively

NOTE 4 With bank groups enabled, t_{CCDL} is $3t_{CK}$ (optional) or $4t_{CK}$, as programmed in MR3.

Figure 9 — t_{CCDS} and t_{CCDL}

5 TRAINING

5.1 INTERFACE TRAINING SEQUENCE

Due to the high data rates of GDDR5, it is recommended that the interfaces be trained to operate with the optimal timings. GDDR5 SGRAM has features defined which allow for complete and efficient training of the I/O interface without the use of the array. The interface trainings are required for normal DRAM functionality unless deemed optional by the DRAM vendor or unless running in lower frequency modes as described in the low frequency section. Interface timings will only be guaranteed after all required trainings have been executed.

A recommended order of training sequences has been chosen based on the following criteria:

The address training must be done first to allow full access to the Mode Registers. (MRS for address training is a special single data rate mode register set guaranteed to work without training). Address input timing shall function without training as long as $t_{AS/H}$ are met at the device.

WCK2CK training should be done before read training because a shift in WCK relative to CK will cause a shift in all READ timings relative to CK.

READ training should be done before WRITE training because optimal WRITE training depends on correct READ data.

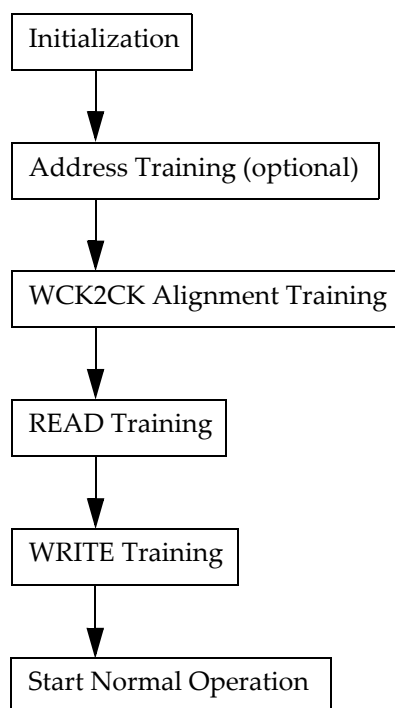


Figure 10 — Interface Training Sequence

5.2 ADDRESS TRAINING

The GDDR5 SGRAM provides means for address bus interface training. The controller may use the address training mode to improve the timing margins on the address bus.

Address training mode is entered and exited via the ADT bit in Mode Register 15 (MR15). Mode Register 15 supports the same setup and hold times on the address pins as for commands to allow a safe entry into address training mode.

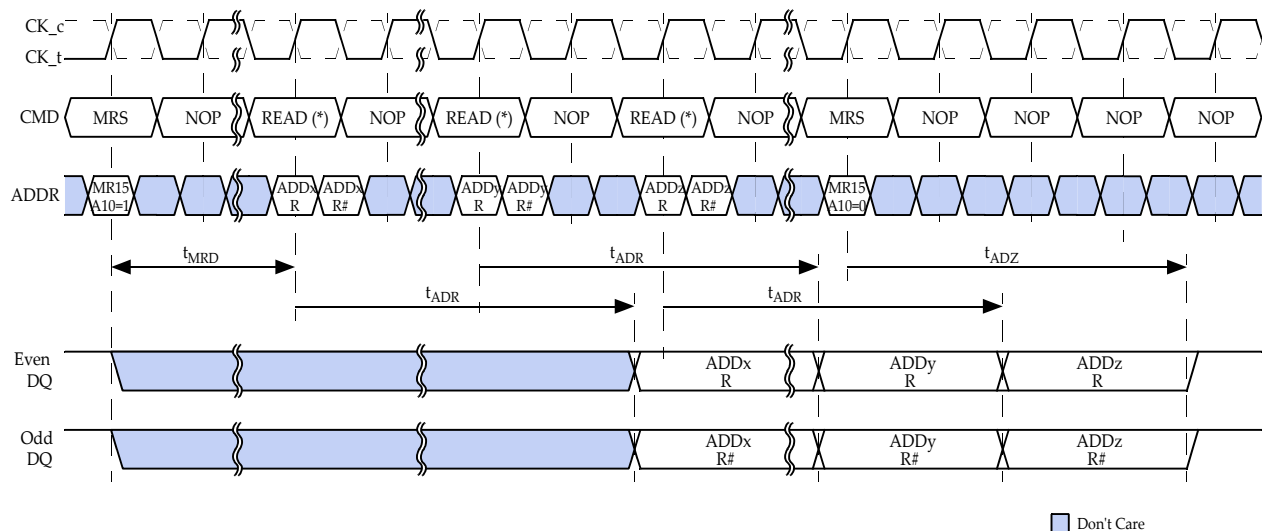
Address training mode uses an internal bridge between the device's address inputs and DQ/DBI_n outputs. It also uses a special READ command for address capture that is encoded using the SDR command pins only (CS_n, RAS_n, CAS_n, WE_n = L, H, L, H). The address values normally used to encode the commands will not be interpreted. Once the address training mode has been entered, the address values registered coincident with this special READ command will be transmitted to the controller on the DQ/DBI_n pins. The controller is then expected to compare the address pattern received to the expected value and to adjust the address transmit timing accordingly. The procedure may be repeated using different address pattern and interface timings.

No WCK clock is required for this special READ command operation during address training mode. The latched addresses are driven out asynchronously.

The only commands allowed during address training mode are this special READ, MRS (e.g., to exit address training mode) and NOP / DESELECT.

When enabled by the ABI bit in Mode Register 1, address bus inversion (ABI) is effective during address training mode. It is suggested to train the ABI_n pin's interface timing together with the other address lines.

The timing diagram in Figure 11 illustrates the typical command sequence in address training mode. The DQ/DBI_n output drivers are enabled as long as the ADT bit is set. The minimum spacing between consecutive special READ commands is $2 t_{CK}$.



NOTE 1 READ command encoding: CS_n = L, RAS_n = H, CAS_n = L, WE_n = H

NOTE 2 ADDxR = 1st half of address x, sampled on rising edge of CK_t;

ADDxR# = 2nd half of address x, sampled on rising edge of CK_c

NOTE 3 Addresses sampled on rising edge of CK_t are returned on even DQ after t_ADR;

addresses sampled on rising edge of CK_c are returned on odd DQ simultaneously with even DQ

NOTE 4 DQs are enabled when ADT bit in Mode Register 15 set to 1 (Enter Address Training Mode)

DQs are disabled after t_ADZ when ADT bit in Mode Register 15 set to 0 (Exit Address Training Mode)

Figure 11 — Address Training Timing

5.2 ADDRESS TRAINING (cont'd)

Table 10 — AC timings in Address Training Mode

Parameter	Symbol	Min	Max	Unit
READ command to data out delay	t_{ADR}	0	vendor specific	ns
ADT off to DQ/DBI_n in ODT state delay	t_{ADZ}	--	vendor specific	ns

Table 11 defines the correspondence between address bits and DQ/DBI_n. Devices configured to x16 mode reflect the address on the two bytes being enabled in that mode, which are bytes 0 and 2 for MF=0 and bytes 1 and 3 for MF=1 configurations. Devices configured to x32 mode reflect the address on the same DQ as in x16 mode; in addition they are allowed but not required to reflect the address on those bytes that are disabled in x16 mode, thus reflecting each address twice.

Devices not supporting an A12/A13 pin shall drive a logic High on the DBI_n pins.

Table 11 — Address to DQ Mapping in Address Training Mode

Output	Address bits registered at rising edge of CK_t								
	A12	A8	A11	BA1	BA2	BA3	BA0	A9	A10
DQ	DBI0_n	DQ22	DQ20	DQ18	DQ16	DQ6	DQ4	DQ2	DQ0
	DBI1_n	DQ30	DQ28	DQ26	DQ24	DQ14	DQ12	DQ10	DQ8
Output	Address bits registered at rising edge of CK_c								
	A13	A7	A6	A5	A4	A3	A2	A1	A0
DQ	DBI2_n	DQ23	DQ21	DQ19	DQ17	DQ7	DQ5	DQ3	DQ1
	DBI3_n	DQ31	DQ29	DQ27	DQ25	DQ15	DQ13	DQ11	DQ9

5.3 WCK2CK TRAINING

The purpose of WCK2CK training is to align the data WCK clock with the command CK clock to aid in the device's internal data synchronization between the logic clocked by CK_t/CK_c and WCK_t/WCK_c. This will help to define both Read and Write latencies between the GDDR5 SGRAM and memory controller. WCK2CK training mode is controlled via MRS.

Before starting WCK2CK training, the following conditions must be met:

- CK_t/CK_c clock is stable and toggling
- The timing of all address and command pins must be guaranteed
- PLL on/off (MR1 bit A7) and PLL delay compensation enable (MR7 bit A2) are set to desired mode before WCK to CK training is started
- The desired WCK2CK alignment point (MR6, bit A0) is selected
- The EDC hold pattern (MR4, bits A0-A3) must be programmed to '1111' as it was required by the first revision of JESD212
- 2 Mode Register bits for internal WCK01 and WCK23 inversion (MR3, bits A2-A3) must be set to a known state
- All banks are idle and no other command execution is in progress

WCK2CK training must be done after any of the following conditions:

- Device initialization
- Any CLmrs, WLMrs, CRCRL or CRCWL latency change
- CK and WCK frequency changes
- PLL on/off (MR1 bit A7) and PLL delay compensation mode (MR7 bit A2) changes
- Change of the WCK2CK alignment point (MR6, bit A0)

At self-refresh exit, at a minimum the device's WCK divide-by-2 circuits must be reset by setting MR3 A4 to HIGH and WCK is restarted in the same way as the initial training value at power up. Alternatively full WCK2CK training can be at done at self-refresh exit. See Self-refresh section for more details on self-refresh. See WCK2CK auto synchronization section for more details on options for WCK2CK alignment for power-down exit.

Figure 12 and Figure 13 show example WCK2CK training sequences. WCK2CK training is entered via MRS by setting bit A4 in MR3. This will initiate the WCK divide-by-2 circuits associated with WCK01 and WCK23 clocks in the device. In case the divide-by-2 circuits are at opposite output phases, which is indicated by opposite "early/late" phases on the EDC pins associated with WCK01 and WCK23 (see below), they may be put in phase by using the WCK01 and WCK23 inversion bits. Alternatively, the WCK clocks may be put into a stable inactive state for this initialization event to aid in resetting all dividers to the same output phase as shown in Figure 13. The challenge of this method is to restart the WCK clocks in a way that even their first clock edges meet the WCK clock input specification. Otherwise, divide-by-2 circuits for both WCK01 and WCK23 might again have opposite phase alignment.

Figure 14 illustrates how the WCK phase information is derived. The phase detectors (PD) sample the internally divided-by-2 WCK clocks. Only one sample point is shown in the figure for clarity. In reality, when WCK2CK training mode is enabled, a sample will occur every t_{CK} and will be translated to the EDC pins accordingly. If the divided-by-2 WCK clock arrives early, then the EDC pin outputs the EDC hold pattern during the time interval specified in Figure 14. If the divided-by-2 WCK clock arrives late, then the EDC pin outputs the inverted EDC hold pattern during the time interval specified in Figure 14. This is shown in Table 12. **Finally, if the divided-by-2 WCK and CK clocks are perfectly aligned at the PD, the EDC pins are indeterminate.**

5.3 WCK2CK TRAINING (cont'd)

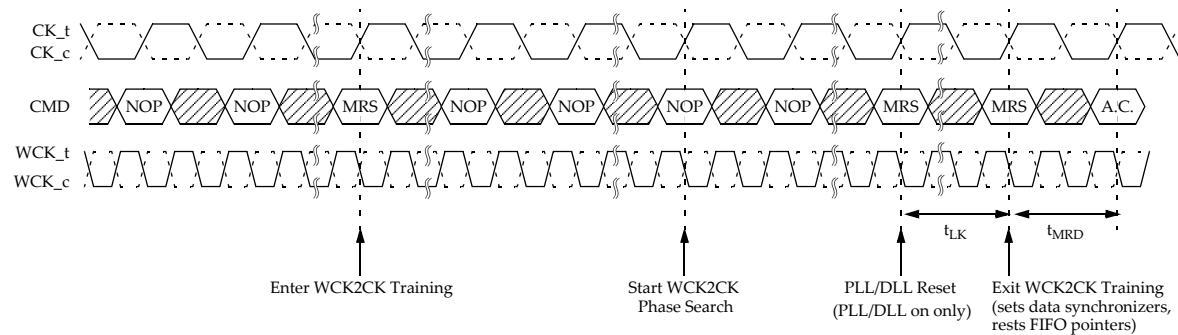


Figure 12 — Example WCK2CK Training Sequence

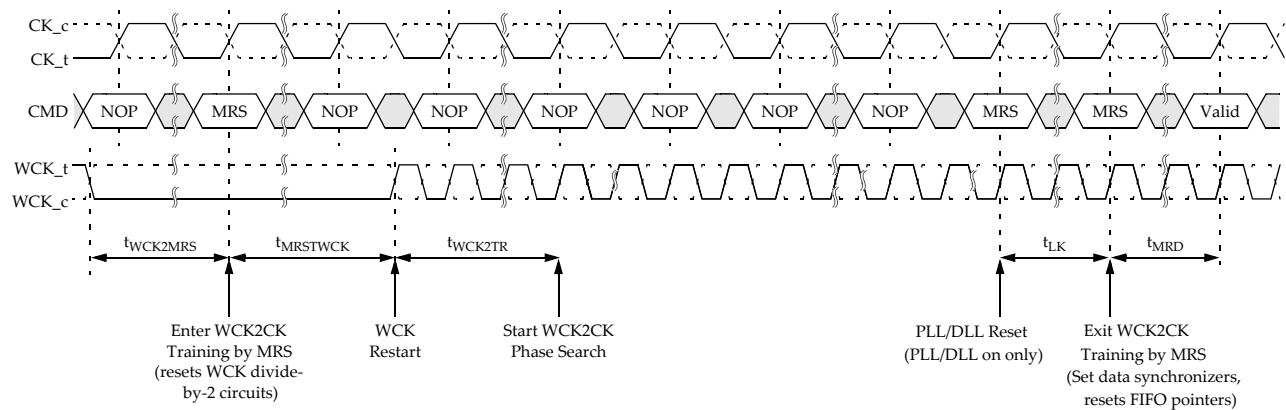


Figure 13 — Example WCK2CK Training Sequence with WCK Stopping

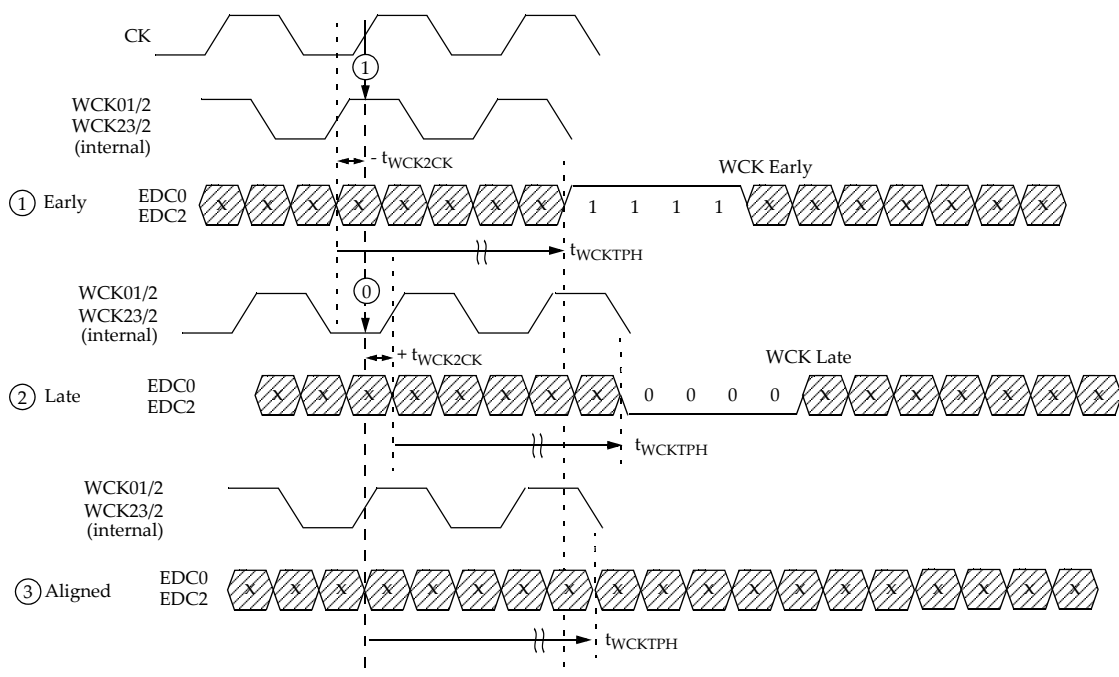


Figure 14 — EDC Pin Behavior for WCK2CK Training (Assumes '1111' as EDC Hold Pattern)

5.3 WCK2CK TRAINING (cont'd)

Table 12 — Phase Detector and EDC Pin Behavior

WCK/2 value sampled by CKt	WCK2CK Phase	Data on EDC Pin	Action
'1'	'Early'	1	Increase Delay on WCK
'0'	'Late'	0	Decrease Delay on WCK

The ideal alignment is indicated by the phase detector output transitioning from “early” to “late” when the delay of the WCK phase is continuously increased. The WCK phase range for ideal alignment is specified by the parameter $t_{WCK2CKPIN}$ in the vendor’s datasheet; the value(s) vary with the PLL/DLL mode (on or off) and the selected alignment point.

If enabled, the PLL/DLL shall not interfere in the behavior of the WCK2CK training. Significantly moving the phase and/or stopping the WCK during training may disturb the PLL/DLL. It is required to perform a PLL/DLL reset after the WCK2CK training has determined and selected the proper alignment between WCK and CK clocks. The PLL/DLL lock time t_{LK} must be met before exiting WCK2CK training to guarantee that the PLL/DLL is in lock such that the device’s data synchronizers are set upon WCK2CK training exit.

WCK2CK training is exited via MRS by resetting bit A4 in MR3. For proper reset of the data synchronizers it is required that the WCK and CK clocks are aligned within $t_{WCK2CKSYNC}$ at the time of the WCK2CK training exit.

After exiting WCK2CK training mode, the WCK phase is allowed to further drift from the ideal alignment point by a maximum of t_{WCK2CK} (e.g., due to voltage and temperature variation). Once this WCK phase drift exceeds $t_{WCK2CK(min)}$ or $t_{WCK2CK(max)}$, it is required to repeat the WCK2CK training and realign the clocks.

WCK2CK alignment at PIN Mode (optional)

The WCK and CK phase alignment point can be changed via MRS by setting bit A0 in MR6. In normal mode, when MR6 A0 is set to ‘0’, the phases of CK and WCK are aligned at the phase detector. On the other hand, when MR6 A0 is set to ‘1’, the phases of CK and WCK are aligned at the pin as shown in Figure 16. PIN mode is supported up to the max CK clock frequency of f_{CKPIN} , and is an option to reduce the time of WCK2CK training at low frequency.

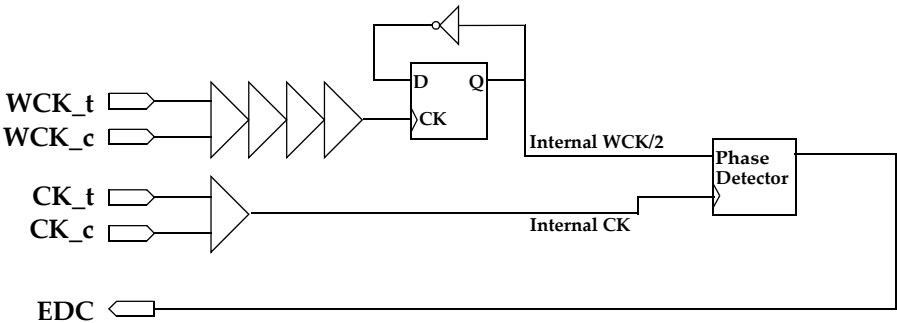


Figure 15 — Normal Mode

5.3 WCK2CK TRAINING (cont'd)

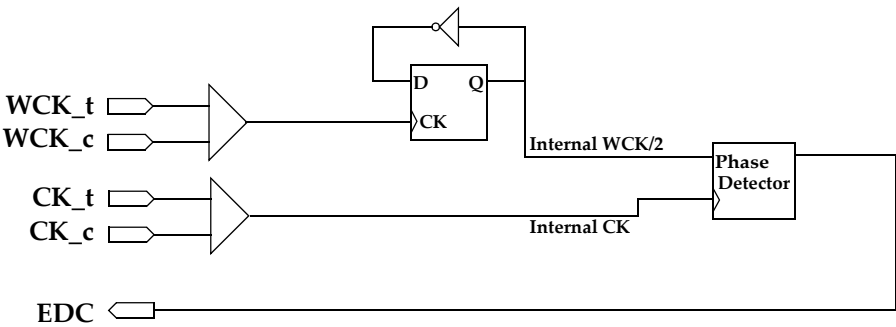


Figure 16 — Pin Mode (Optional)

WCK2CK Auto Synchronization (Optional)

GDDR5 SGRAMs may optionally support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit. This mode is controlled by the autosync bit (MR7, bit A4), and is effective when the LP2 bit (MR5, bit A1) is set and the WCK clocks are stopped during power-down. Also, this mode works for both normal and PIN mode. When WCK2CK automatic synchronization mode is enabled, a full WCK2CK training including Phase search is not required after power-down exit, although WCK2CK MRS must be issued momentarily for setting the data synchronizers. However, WCK and CK clocks must meet the $t_{WCK2CKSYNC}$ specification upon power-down exit. Any allowed command may be issued after t_{XPN} or after t_{LK} in case the PLL/DLL had been enabled upon power-down entry. The PLL/DLL sequence is not affected by this mode. The use of WCK2CK automatic synchronization mode is restricted to lower operating frequencies up to $f_{CKAUTOSYNC}$ as described in vendor’s datasheets.

Table 13 describes WCK2CK training methods for different frequency ranges. Each Frequency range is vendor specific. Normal and PIN mode of WCK2CK training are described in Table 13. Each frequency range is DRAM vendor specific. Divider initialization can be done by training with WCK2CK inversion, WCK2CK stopping, or WCK2CK auto-sync. If the user wants to use WCK2CK stop for divider initialization instead of WCK2CK auto-sync, the user must not set the WCK2CK auto-sync. Below middle frequency, the combined use of PIN and WCK2CK auto-sync modes can minimize WCK2CK training time.

Table 13 — An Example of WCK2CK Training Simplified for Normal Mode and PIN Mode

	High Frequency (i.e., 5 Gbps)		Middle Frequency (i.e., 2 Gbps)		Low Frequency (i.e., 400 Mbps)	
Frequency (Vendor Specific)						
WCK2CK alignment mode	Normal	PIN	Normal	PIN	Normal	PIN
Phase Search	Required	Required	Required	No ¹	No ¹	No ¹
NOTE 1 The divided WCK_t/WCK_c should be aligned CK_t/CK_c by WCK2CK Auto Synchronization or WCK stop mode						

5.3 WCK2CK TRAINING (cont'd)

The following examples describe the WCK2CK training in more detail.

Example 1: outline of a basic WCK2CK training sequence without WCK clock stop:

- 1) Enable training mode via MRS and wait t_{MRD}
- 2) Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case the internal divide-by-2 circuits are at opposite phase use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits
- 3) Adjust the WCK phase independently for WCK01 and WCK23 to the optimal point ("ideal alignment")
- 4) Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)
- 5) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
- 6) Wait t_{MRD} for the reset of data synchronizers

Example 2: outline of a basic WCK2CK training sequence with WCK clock stop:

- 1) Stop WCK clocks with WCK01_t/WCK23_t LOW and WCK01_c/WCK23_c HIGH
- 2) Wait $t_{WCK2MRS}$ for internal WCK clocks to settle
- 3) Enable training mode via MRS and wait $t_{MRSTWCK}$ for divide-by-2 circuits to reset
- 4) Start WCK clocks without glitches (both divide-by-2 circuits remain in sync)
- 5) Wait t_{WCK2TR} for internal WCK clocks to stabilize
- 6) Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; adjust the WCK phase to the optimal point ("ideal alignment")
- 7) Issue a PLL/DLL reset and wait t_{LK} (PLL/DLL on mode only)
- 8) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
- 9) Wait t_{MRD} for the reset of data synchronizers

GDDR5 WCK2CK Training in x16 mode

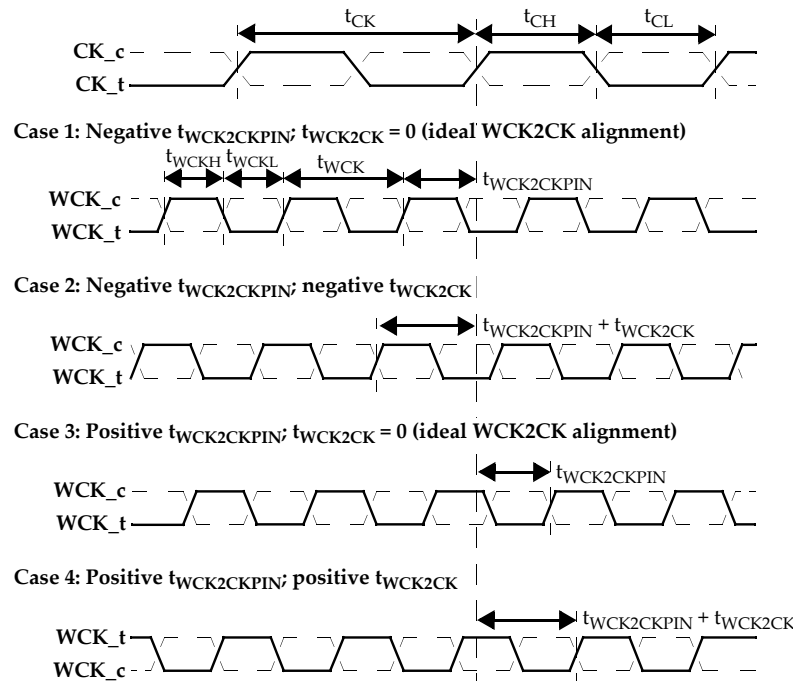
For configurations with WCK clocks not shared between two devices it is suggested to set the WCK phase to the ideal alignment point. However, for configurations where two devices (x16) share their WCK clocks as in a x16 clamshell, an offset given by the midpoint of both DRAM's ideal WCK positions may be required. The maximum allowed offset in this case is specified by parameter $t_{WCK2CKSYNC}$: it defines the WCK offset range from the ideal alignment which still guarantees a device to internally synchronize its WCK and CK clocks upon training exit.

Example: outline of training sequence for x32 and x16 configurations with 2 devices sharing their WCK clocks (e.g., clamshell):

- 1) Enable training mode for both DRAMs via MRS and wait t_{MRD}
- 2) For both DRAMs sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case the internal divide-by-2 circuits are at opposite phases use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits; in case of shared CS_n signals use MREMF0 and MREMF1 bits in MR15 to explicitly direct the MRS command for this phase flipping to either DRAM1 or DRAM2 ("soft chip select");
- 3) Sweep and observe the phase on DRAM1 independently for WCK01 on EDC0 and WCK23 on EDC2; store the setting for the optimal WCK phase
- 4) Sweep and observe the phase on DRAM2 independently for WCK01 on EDC0 and WCK23 on EDC2; store the setting for the optimal WCK phase
- 5) Sweep WCK01 and WCK23 phase to midpoint of DRAM1 and DRAM2 optimal settings
- 6) Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)
- 7) While all WCK and CK are aligned, exit WCK2CK training mode via MRS
- 8) Wait t_{MRD} for the reset of data synchronizers

5.3 WCK2CK TRAINING (cont'd)

READ and WRITE latency timings are defined relative to CK. Any offset in WCK and CK at the pins and/or the phase detector will be reflected in the latency timings. The parameters used to define the relationship between WCK and CK are shown in Figure 17. For more details on the impact on READ and WRITE timings see the OPERATIONS section.



Note: $t_{WCK2CKPIN}$ and t_{WCK2CK} parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK-to-CK phase for stable device operation.

Figure 17 — WCK2CK Timings

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ0-DQ31, DBI0_n-DBI3_n, EDC0-EDC3) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include the DBI_n pins. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC pins.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 18 shows an example of the internal data paths used with LDFF and RDTR. Table 14 lists AC timing parameters associated with Read Training.

Table 14 — LDFF and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVE to LDFF command delay	t_{RCDLTR}		–	ns	
ACTIVE to RDTR command delay	t_{RCDRTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
RDTR to RDTR command delay	t_{CCDS}		–	t_{CK}	2
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF(111) to LDFF command cycle time	t_{LTL7TR}		–	t_{CK}	1
LDFF(111) to RDTR command delay	t_{LTRTR}		–	t_{CK}	
READ or RDTR to LDFF command delay	t_{RDTLT}		–	t_{CK}	
NOTE 1 The min. value is vendor specific and does not exceed 8 t_{CK} .					
NOTE 2 Use t_{CCDS} for gapless consecutive RDTR commands regardless whether Bank Groups is enabled or not.					

5.4 READ TRAINING (cont'd)

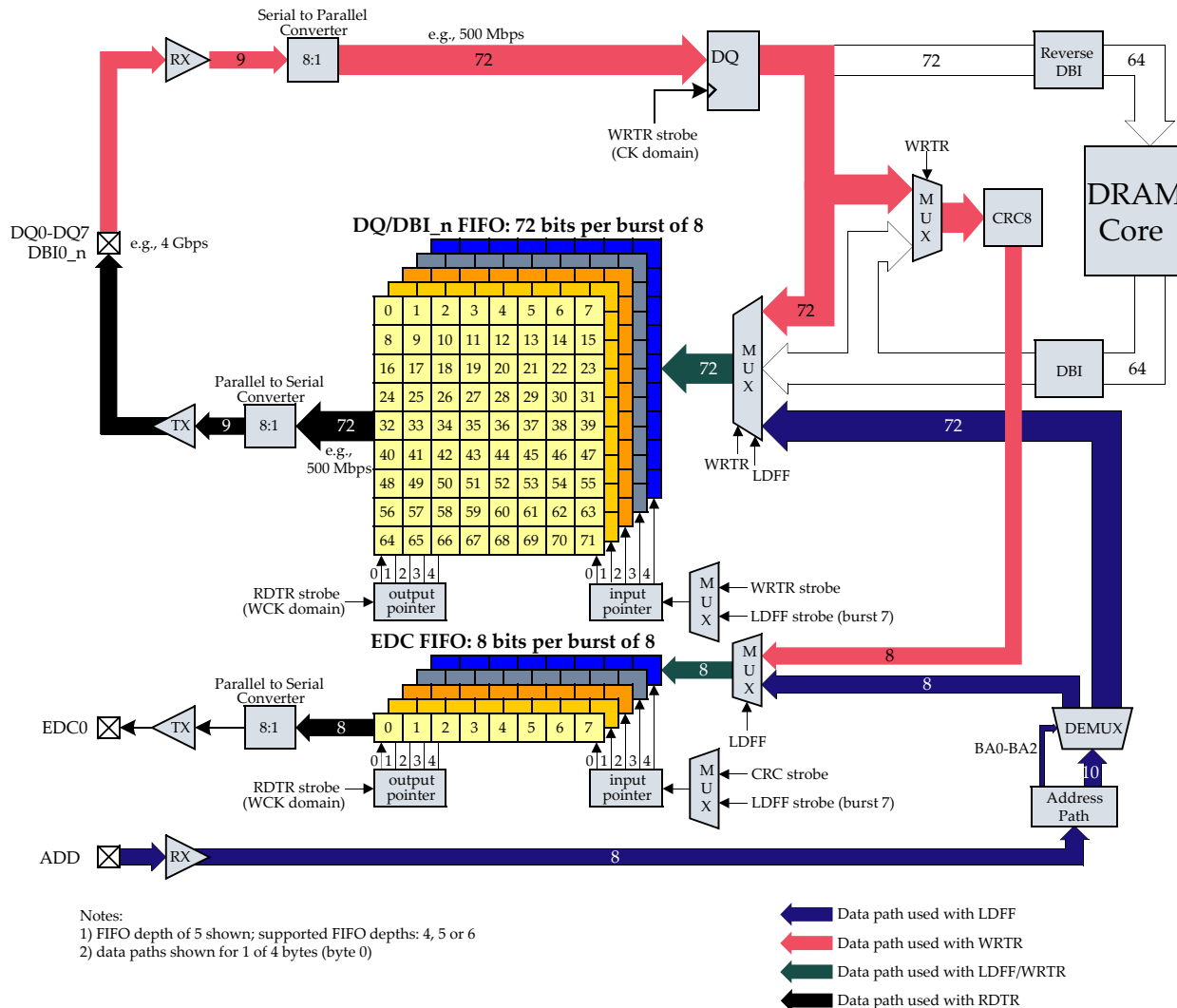


Figure 18 — Data Paths Used for Read and Write Training

LDF Command

The LDF command (Figure 19) is used to securely load data to the device's Read FIFOs via the address bus. Depending on the device's READ FIFO depth nFIFO (4-6), any bit pattern of length 32-48 can be loaded uniquely to every DQ, DBI_n and EDC pin within a byte. The FIFO depth is fixed by design and can be read via the Vendor ID function.

Eight LDF commands are required to fill one FIFO stage; each LDF command loads one burst position, and the bank addresses BA0-BA2 select the burst position from 0 to 7.

The data pattern is conveyed on address pins A0-A7 for DQ0-DQ7, A9 for DBI0_n, and BA3 for EDC0; the data are internally replicated to all 4 bytes, as shown in Figure 20.

LDF loads the DBI FIFO regardless of the WDBI and RDBI Mode Register bits. It also loads the EDC FIFO regardless of the WRCRC and RDCRC Mode Register bits, and no CRC is calculated; however, RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command.

5.4 READ TRAINING (cont'd)

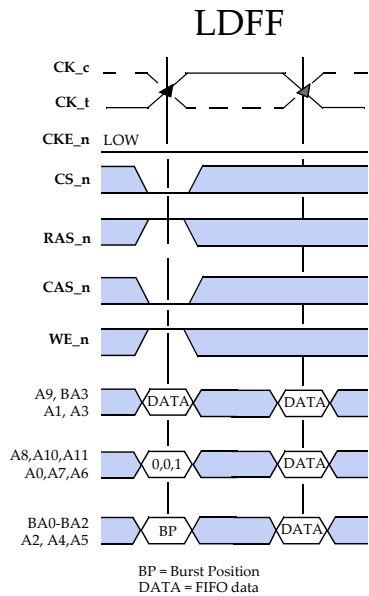


Figure 19 – LDFF Command

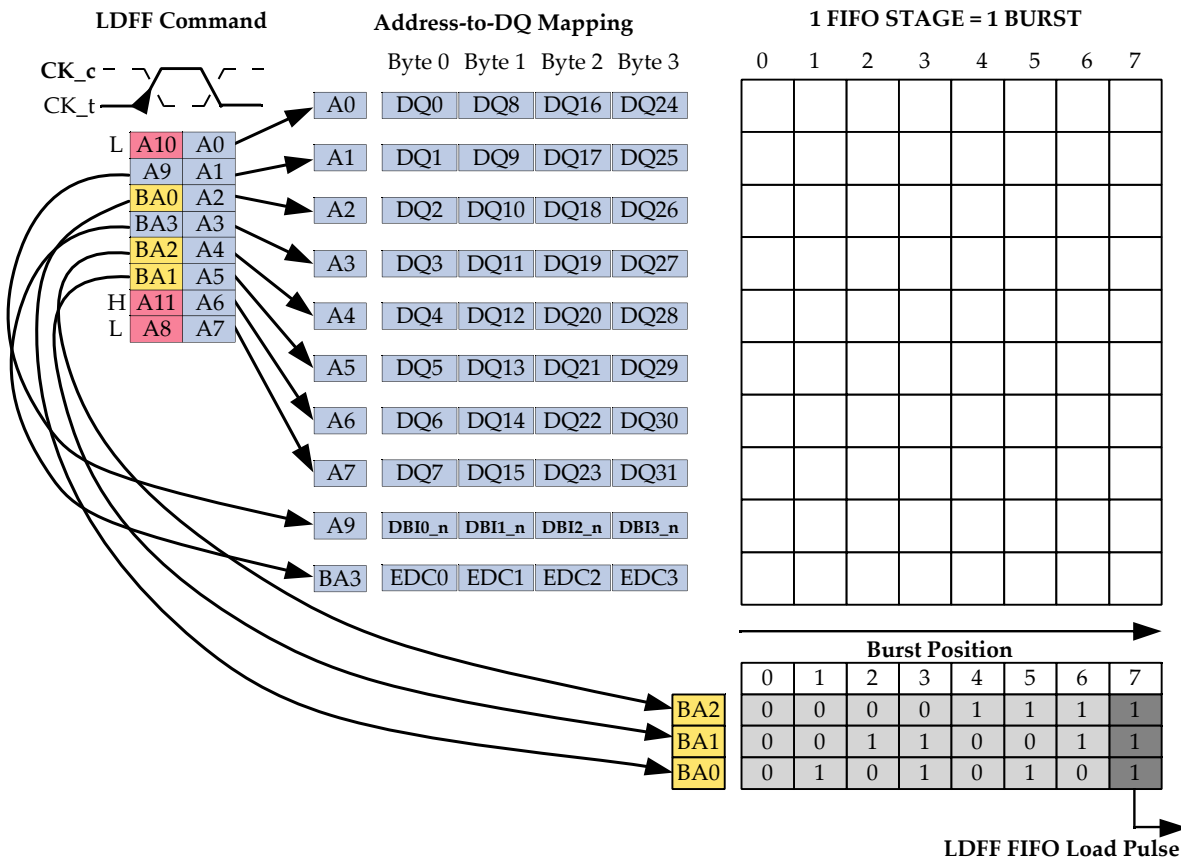


Figure 20 – LDFF Command Address to DQ/DBI_n/EDC Mapping

5.4 READ TRAINING (cont'd)

All burst addresses 0 to 7 must be loaded; LDFF commands to burst address 0 to 6 may be issued in random order; the LDFF command to burst address 7 (LDFF7) must be the last of 8 consecutive LDFF commands, as it effectively loads the data into the FIFO and results in a FIFO pointer increment. Consecutive LDFF commands have to be spaced by at least t_{LTLTR} , and at least t_{LTL7TR} cycles are required after each LDFF command to burst address 7.

LDFF pattern may efficiently be replicated to the next FIFO stages by issuing consecutive LDFF commands to burst address 7 (with identical data pattern). The data pattern in the scratch memory for LDFF will be available until the first RDTR command.

The DQ/DBI_n output buffers remain in ODT state during LDFF.

An amount of LDFF commands to burst address 7 greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input.

The total number of LDFF commands to burst address 7 modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between LDFF and RDTR.

The EDC hold pattern is driven on the EDC pins during LDFF (provided RDQS mode is not enabled).

RDTR Command

A RDTR burst is initiated with a RDTR command as shown in Figure 21. No bank or column addresses are used as the data is read from the internal READ FIFO, not the array. The length of the burst initiated with a RDTR command is eight. There is no interruption nor truncation of RDTR bursts.

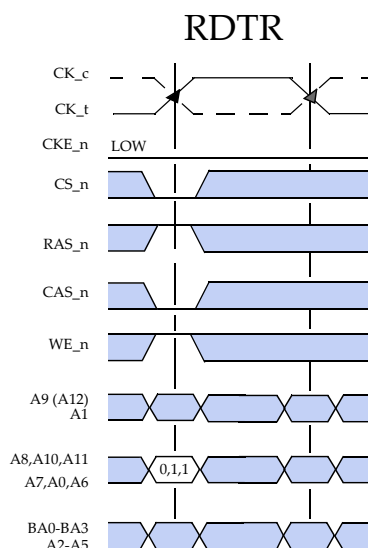


Figure 21 — RDTR Command

5.4 READ TRAINING (cont'd)

A RDTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command. If not set, the DBI_n pins will remain in ODT state, and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. The DBI_n pin behaves like a DQ, and no encoding with DBI is performed.

An amount of RDTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data output. The FIFO depth from which the RDTR data is read must be a number between 4-6 and must be specified by the DRAM vendor. The FIFO depth is read via the Vendor ID function.

During RDTR bursts, the first valid data-out element will be available after the CAS latency (CL). The latency is the same as for READ. The data on the EDC pins comes with additional CRC latency (t_{CRCRD}) after the CL.

Upon completion of a burst, assuming no other RDTR command has been initiated, all DQ and DBI_n pins will drive a value of '1' and the ODT will be enabled at a maximum of $1 t_{CK}$ later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

Data from any RDTR burst may be concatenated with data from a subsequent RDTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new RDTR command should be issued after the first RDTR command according to the t_{CCDS} timing.

A WRTR can be issued any time after a RDTR command as long as the bus turn around time t_{RTW} is met.

The total number of RDTR commands modulo FIFO depth must be equal to total number of WRTR commands modulo FIFO depth when used in conjunction with WRTR. No READ or WRITE commands are allowed between WRTR and RDTR.

The total number of RDTR commands modulo FIFO depth must be equal to the total number of LDFF commands to burst position 7 modulo FIFO depth when used in conjunction with LDFF. No READ or WRITE commands are allowed between LDFF and RDTR.

5.5 WRITE TRAINING

Write training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed input of the device. Each pin (DQ0-DQ31, DBI0_n-DBI3_n) can be individually trained during this sequence.

For Write Training the following conditions must be true:

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- the PLL/DLL must be locked, if enabled.
- WCK2CK training should be complete
- Read training should be complete
- RDBI and WDBI must be enabled prior to and during Write Training if the training shall include the DBI_n pins. RDCRC and WRCRC must be enabled prior to and during Write Training if the training shall include the EDC pins.

The following commands are associated with Write Training:

- WRTR to write a burst of data directly into the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither WRTR nor RDTR access the memory core. No MRS is required to enter Write Training.

Figure 18 shows an example of the internal data paths used with WRTR and RDTR. Figure 23 shows a typical Write training command sequence using WRTR and RDTR. Table 15 lists AC timing parameters associated with WRITE Training.

Table 15 — WRTR and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVE to WRTR command delay	t_{RCDWTR}		—	ns	
ACTIVE to RDTR command delay	t_{RCDRTR}		—	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		—	ns	
RD/WR bank A to RD/WR bank B command delay different bank groups	t_{CCDS}		—	t_{CK}	1
WRTR to RDTR command delay	t_{WTRTR}		—	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}		—	t_{CK}	
READ or RDTR to WRITE or WRTR command delay	t_{RTW}		—	ns	2
NOTE 1 Use t_{CCDS} for gapless consecutive WRTR and RDTR commands regardless whether Bank Groups is enabled or not.					
NOTE 2 t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between t_{WCK2DQO} and t_{WCK2DQI} shall be considered in the calculation of the bus turnaround time.					

5.5 WRITE TRAINING (cont'd)

WRTR Command

A WRTR burst is initiated with a WRTR command as shown in Figure 22. No bank or column addresses are used as the data is written to the internal READ FIFO, not the array. The length of the burst initiated with a WRTR command is eight. There is no interruption nor truncation of WRTR bursts.

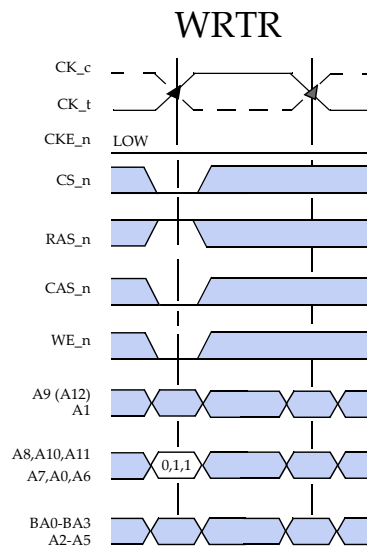


Figure 22 — WRTR Command

A WRTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

WDBI and WRCRC must be enabled to write the DBI and EDC bits, respectively, with the WRTR command. If WDBI is not set, a '1' will be written to the DBI FIFO, and a '1' will be assumed for the DBI_n input in the CRC calculation. In contrast to a normal WRITE, no CRC is returned by the WRTR command and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. Please note that RDCRC must be enabled to read the calculated CRC data with the RDTR command.

An amount of WRTR commands equal to the FIFO depth is required to fully load the FIFO; any number of WRTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input. The FIFO depth to which the WRTR data is written must be a number between 4-6 and must be specified by the DRAM vendor. The FIFO depth is read via the Vendor ID function.

During WRTR bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is the same as for WRITE.

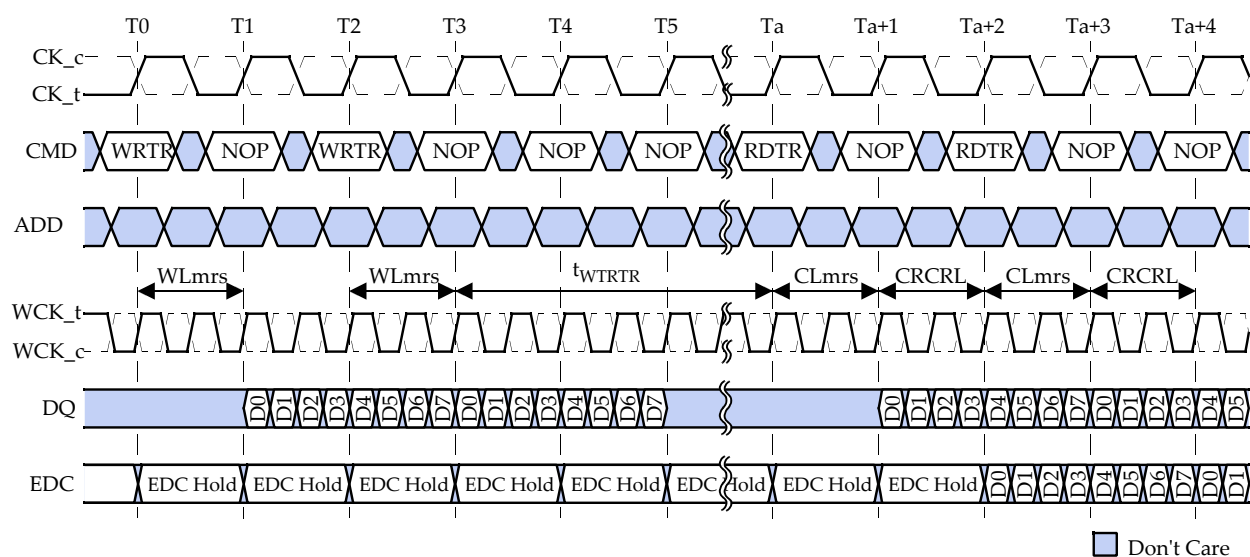
Upon completion of a burst, assuming no other WRTR data is expected on the bus the device's DQ and DBI_n pins will be driven according to the ODT state. Any additional input data will be ignored.

5.5 WRITE TRAINING (cont'd)

Data from any WRTR burst may be concatenated with data from a subsequent WRTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRTR command should be issued after the previous WRTR command according to the t_{CCDS} timing.

A RDTR can be issued any time after a WRTR command as long as the internal bus turn around time t_{RTWTR} is met.

The total number of WRTR commands modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between WRTR and RDTR.



1. $WLmrs$, $CLmrs$ and $CRCRL$ set to 1 for ease of illustration; check Mode Register definition for supported settings

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}=0$, $t_{WCK2CK}=0$) for illustration purposes. WCK2CK training determines the needed offset between WCK_t and CK.

Figure 23 — Write Training Using WRTR and RDTR Commands

6 MODE REGISTERS

GDDR5 specifies 11 Mode Registers to define the specific mode of operation. MR0 to MR8, MR11 and MR15 are defined as shown in the overview in Figure 24. MR9, M10, M12 to MR14 are not defined and may be used by DRAM vendors for vendor specific features. Reprogramming the Mode Registers will not alter the contents of the memory array.

All Mode Registers are programmed via the MODE REGISTER SET (MRS) command and will retain the stored information until they are reprogrammed or the device loses power. Mode Registers must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values e.g., upon power-up.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0. Bit A12/A13 is not used for any mode register programming as this address input is not defined for 512 Mb and 1 Gb densities.

If the user activates bits in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is not implemented).

6 MODE REGISTERS (cont'd)

	BA3	BA2	BA1	BA0	A12-A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0	0	Write Recovery (WR)			TM	CAS Latency (CLmrs)			Write Latency (WLmrs)				
MR1	0	0	0	1	0	PLL Reset	ABI	WDBI	RDBI	PLL DLL	Cal Upd	ADD/CMD Termination	Data Termination	Driver Strength			
MR2	0	0	1	0	0	ADD/CMD Termination Offset		Data and WCK Termination Offset		OCD Pullup Driver Offset		OCD Pulldown Driver Offset					
MR3	0	0	1	1	0	Bank Groups		WCK Termination		Info	RDQS Mode	WCK 2CK	WCK 23Inv	WCK 01Inv	Self Refresh		
MR4	0	1	0	0	0	EDC 13Inv	WR CRC	RD CRC	CRC Read Latency (CRCRL)	CRC Write Latency (CRCWL)		EDC Hold Pattern					
MR5	0	1	0	1	0	RAS						PLL/DLL Bandwidth (PLLBW)		LP3	LP2	LP1	
MR6	0	1	1	0	0	VREFD Offset Bytes in rows A to F			VREFD Offset Bytes in rows M-U			VREFD	Auto VREFD	VREFD Merge	WCK PIN		
MR7	0	1	1	1	0	DCC		VDD Range		Half VREFD	Temp Sense	DQ PreA	Auto Sync	LF Mode	PLL DelC	PLL FLock	PLL StdbY
MR8	1	0	0	0	0	RFU							REF PB	EDC Hi-Z	WR EHF	CL EHF	
MR11	1	0	1	1	0	PASR Row Segment Mask			PASR 2-Bank Mask								
MR15	1	1	1	1	0	RFU	ADT	MRE MF1	MRE MF0								

Figure 24 — Mode Registers Overview

6.1 MODE REGISTER 0 (MR0)

Mode Register 0 controls operating modes such as Write Latency, CAS latency, Write Recovery and Test Mode as shown in Figure 25. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=0 and BA3=0.

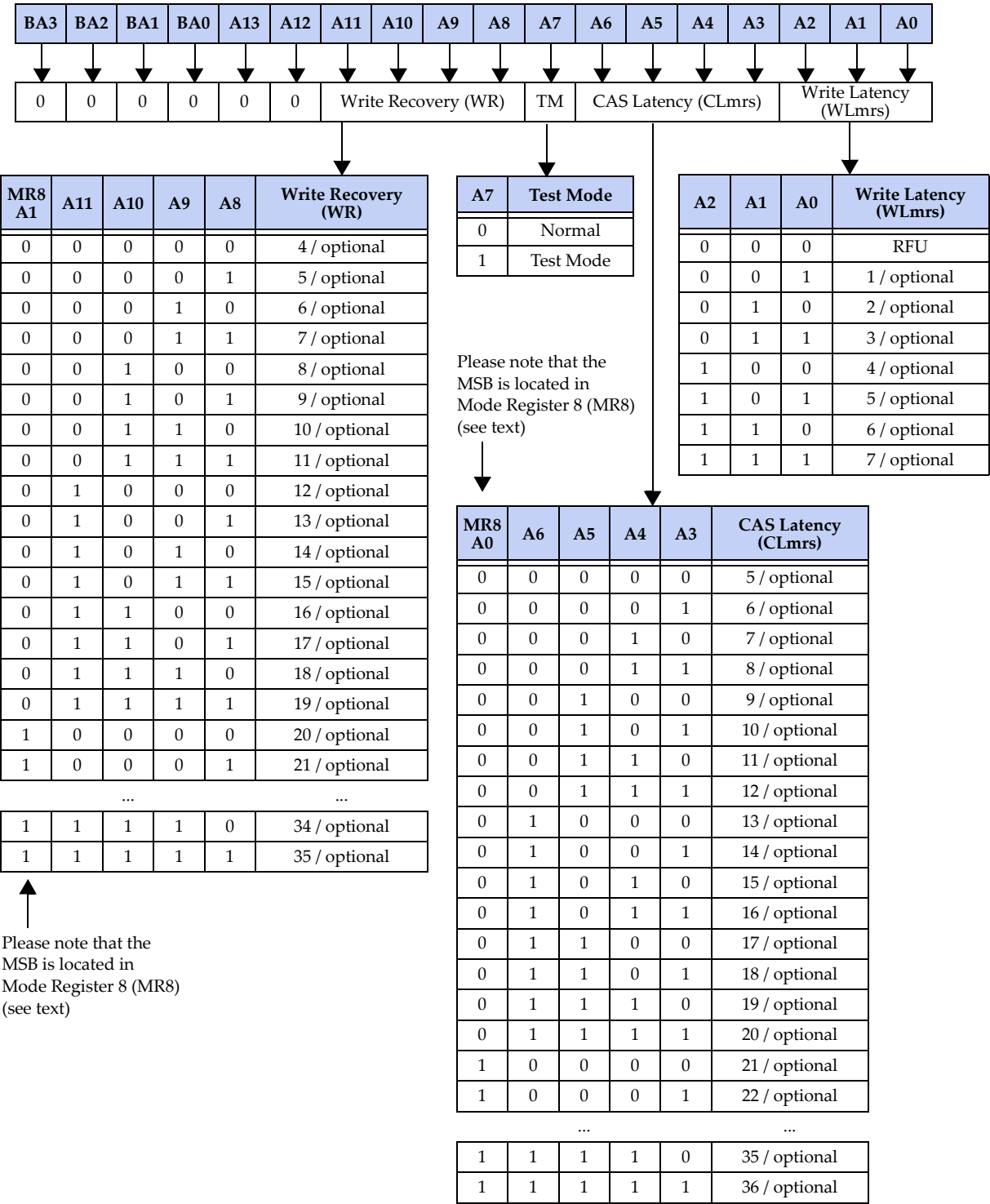


Figure 25 — Mode Register 0 (MR0) Definition

6.1 MODE REGISTER 0 (MR0) (cont'd)

WRITE Latency (WLMrs)

The WRITE latency (WLMrs) is the delay in clock cycles used in the calculation of the total WRITE latency (WL) between the registration of a WRITE or WRTR command and the availability of the first piece of input data. DRAM vendor specifications should be checked for value(s) of WLMrs supported. All WLMrs values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported WLMrs values; the supported WLMrs range must be contiguous. The full WRITE latency definition can be found in the section entitled OPERATION.

When the WRITE latencies are set to small values (i.e., 1,2,... clocks), the input receivers may turn off in bank idle and POWER-DOWN states only, in turn, raising the average operating power. When the WRITE latency is set to higher values (i.e., .. 6, 7 clocks) the input receivers turn on when the WRITE or WRTR command is registered. Refer to vendor datasheets for value(s) of WLMrs where the input receivers are always on or only turn on when the WRITE or WRTR command is registered.

CAS Latency (CLMrs)

The CAS latency (CLMrs) is the delay in clock cycles used in the calculation of the total READ latency (CL) between the registration of a READ or RDTR command and the availability of the first piece of output data.

By default CLMrs is specified by bits A3-A6, defining a CLMrs range of 5 to 20 t_{CK} . All CLMrs values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported CLMrs values; the supported CLMrs range must be contiguous.

For higher frequencies, the CLMrs range may optionally be expanded by the CLEHF bit located in Mode Register 8 (MR8). With the addition of the CLEHF bit a CLMrs range of 5 to 36 t_{CK} is defined. Please note that with the presence of the CLEHF bit a change of the CAS latency may require two MRS commands.

DRAM vendor specifications should be checked for value(s) of CLMrs supported. The full READ latency definition can be found in the section entitled OPERATION.

WRITE Recovery (WR)

The programmed WR value is used for the auto precharge feature along with tRP to determine tDAL. The WR register bits are not a required function and may be implemented at the discretion of the DRAM manufacturer.

WR must be programmed with a value greater than or equal to $RU\{t_{WR}/t_{CK}\}$, where RU stands for round up, t_{WR} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time.

By default WR is specified by bits A8-A11, defining a WR range of 4 to 19 t_{CK} . All WR values are marked as “optional”, allowing the DRAM vendor to define the minimum and maximum supported WR values; the supported WR range must be contiguous.

For higher frequencies, the WR range may optionally be expanded by the WREHF bit located in Mode Register 8 (MR8). With the addition of the WREHF bit a WR range of 4 to 35 t_{CK} is defined. Please note that with the presence of the WREHF bit a change of the WRITE Recovery may require two MRS commands.

Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to '0', and bits A0-A6 and A8-A11 set to the desired values. Programming bit A7 to '1' places the device into a test mode that is only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

6.2 MODE REGISTER 1 (MR1)

Mode Register 1 controls functions like drive strength, data termination, address/command termination, Read DBI, Write DBI, ABI, control of calibration updates and PLL/DLL as shown in Figure 26.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=0 and BA3=0. Bits A0-A1, A4-A6 and A10 of this register are initialized with '0's.

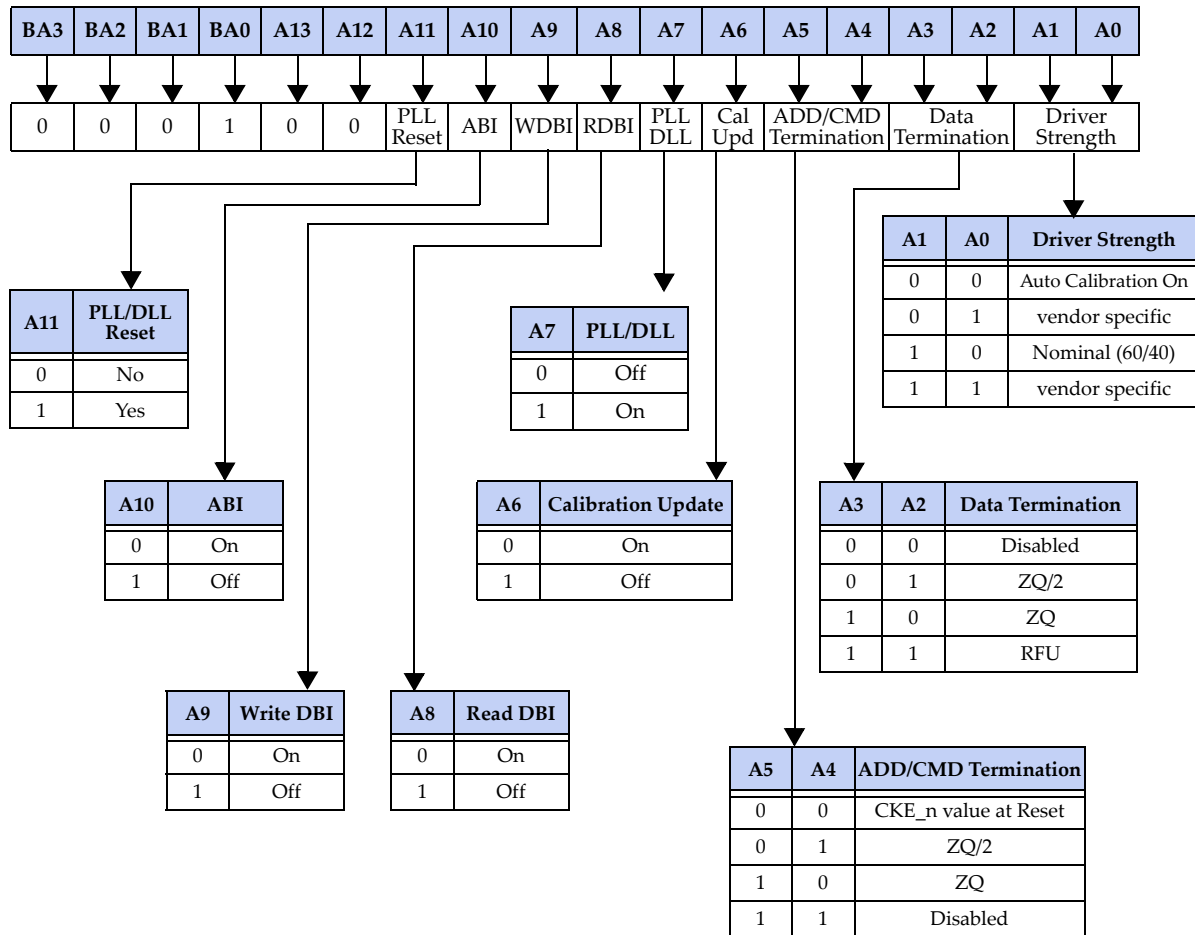


Figure 26 — Mode Register 1 (MR1) Definition

Impedance Autocalibration of Output Buffer and Active Terminator

GDDR5 SGRAMs offer autocalibrating impedance output buffers and on-die terminations. This enables a user to match the driver impedance and terminations to the system within a given range. To adjust the impedance, an external precision resistor is connected between the ZQ pin and VSSQ. A nominal resistor value of 120 Ohms is equivalent to the 40 Ohms Pulldown and 60 Ohms Pullup nominal impedances of GDDR5 SGRAMs. RESET_n, CK_t and CK_c are not internally terminated. CK_t and CK_c shall be terminated on the system using external 1% resistors to VDDQ.

The output driver and on-die termination impedances are updated during all REFRESH commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

6.2 MODE REGISTER 1 (MR1) (cont'd)

Driver Strength

Bits A0 and A1 define the driver strength. The Auto Calibration setting enables the Auto-Calibration functionality for the Pulldown, Pullup and Termination over process, temperature and voltage changes. The design target for the factory setting is 40 Ohm Pulldown, 60 Ohm Pullup driver strength with nominal process, voltage and temperature conditions.

The nominal option enables the factory setting for the Pulldown, Pullup driver strength and termination. With this option enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with Auto Calibration.

Data Termination

Bits A2 and A3 define the data termination value for the on-die termination (ODT) for the DQ and DBI_n pins in combination with the driver strength setting.

The termination can be set to a value of $ZQ/2$ which is intended for a single loaded system, or ZQ which is intended for a weaker termination used in a lower power or frequency applications. The data termination may also be turned off.

ADD/CMD Termination

Bits A4 and A5 define the address/command termination. The default setting ('00') provides that the address/command termination is determined by latching CKE_n on the rising edge of RESET_n.

The address/command termination can also be set to a value of $ZQ/2$ which is intended for a single loaded system, or ZQ which is intended for double loaded configurations with two devices sharing a common address/command bus. The address/command termination may also be turned off.

Calibration Update

The Calibration Update setting enables the calibration value to be updated automatically by the auto calibration engine. The function is enabled upon power-up to reduce update induced jitter. The user may decide to suppress updates from the auto calibration engine by disabling Calibration Update (A6=1).

The calibration updates can occur with any REFRESH command. The update is not complete for a time t_{KO} after the latching of the REFRESH command. During this t_{KO} time, only NOP or DESELECT commands may be issued

PLL/DLL and PLL/DLL Reset

The PLL/DLL is optional on GDDR5 SGRAMs. If a PLL or DLL is to be used, it must be enabled for normal operation by setting bit A7 to '1'.

A PLL/DLL reset is done by turning the PLL/DLL off then on, or by use of the PLL/DLL Reset bit A11. The PLL/DLL Reset bit is self clearing meaning that it returns back to the value '0' after the PLL/DLL reset function has been issued.

RDBI and WDBI

Bit A8 controls Data Bus Inversion (DBI) for READs (RDBI), and bit A9 controls Data Bus Inversion for WRITEs (WDBI). For more details on DBI see READ and WRITE Data Bus Inversion (DBI) in the section entitled OPERATION.

ABI

Address Bus Inversion (ABI) is selected independently from DBI using bit A10. When enabled any data sent over the address bus (whether opcode, addresses, LDFF data or DM) is inverted or not inverted based on the state of ABI_n signal. For more details on ABI see Address Bus Inversion (ABI) in the section entitled OPERATION.

6.3 MODE REGISTER 2 (MR2)

Mode Register 2 defines the output driver (OCD) and termination offsets as shown in Figure 27.

Mode Register 2 is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=0 and BA3=0.

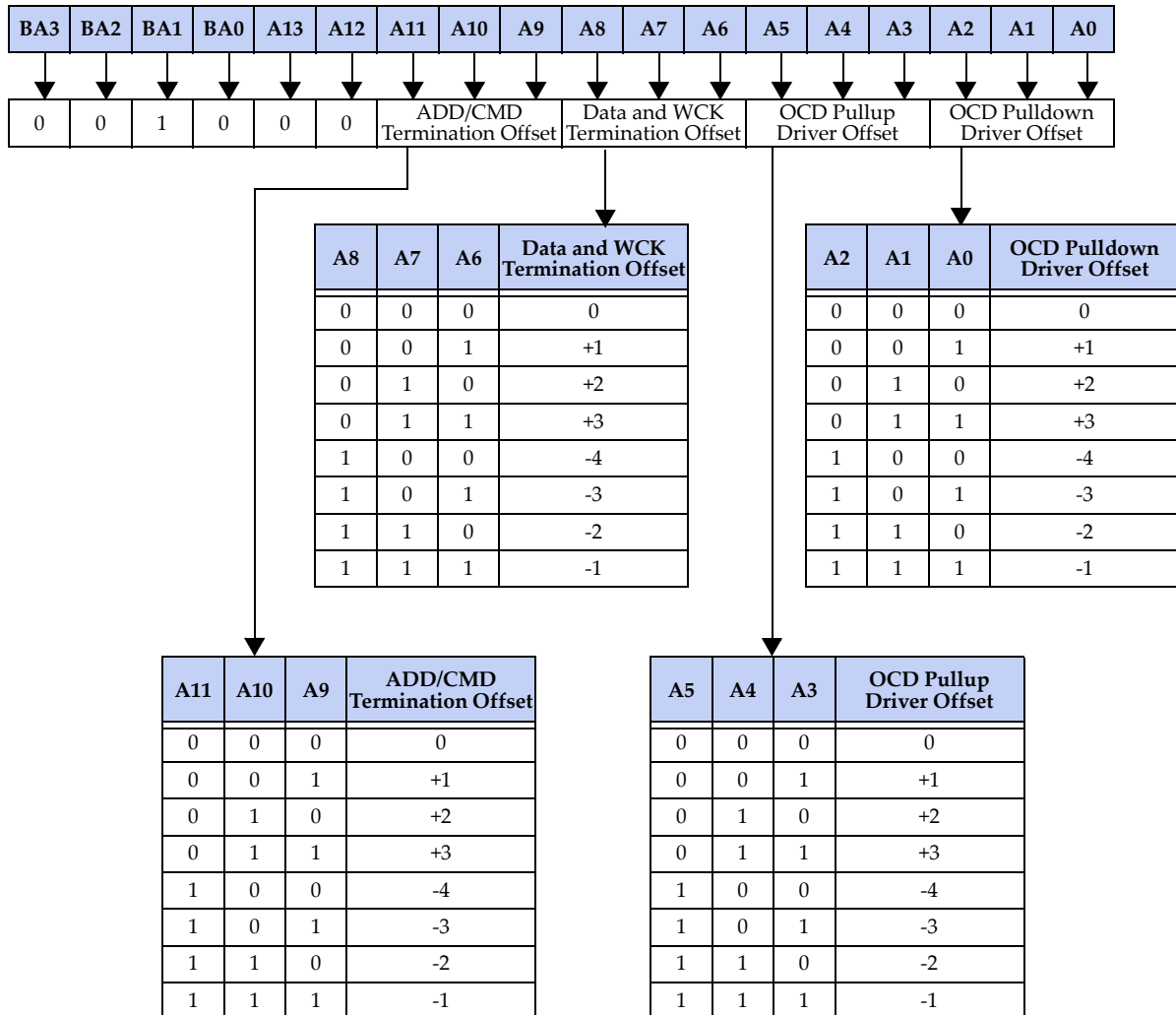


Figure 27 — Mode Register 2 (MR2) Definition

Impedance Offsets

The driver and termination impedances may be offset individually for PD driver, PU driver, DQ/DBI_n/ WCK termination and address/command termination. The offset impedance step values may be non-linear and will vary across DRAM vendors and across PVT. With negative offset steps the drive strengths will be decreased and Ron will be increased. With positive offset steps the drive strengths will be increased and Ron will be decreased. With negative offset steps the termination value will be increased. With positive offset steps the termination value will be decreased.

IV curves and AC timings are only guaranteed with zero offset.

6.3 MODE REGISTER 2 (MR2) (cont'd)

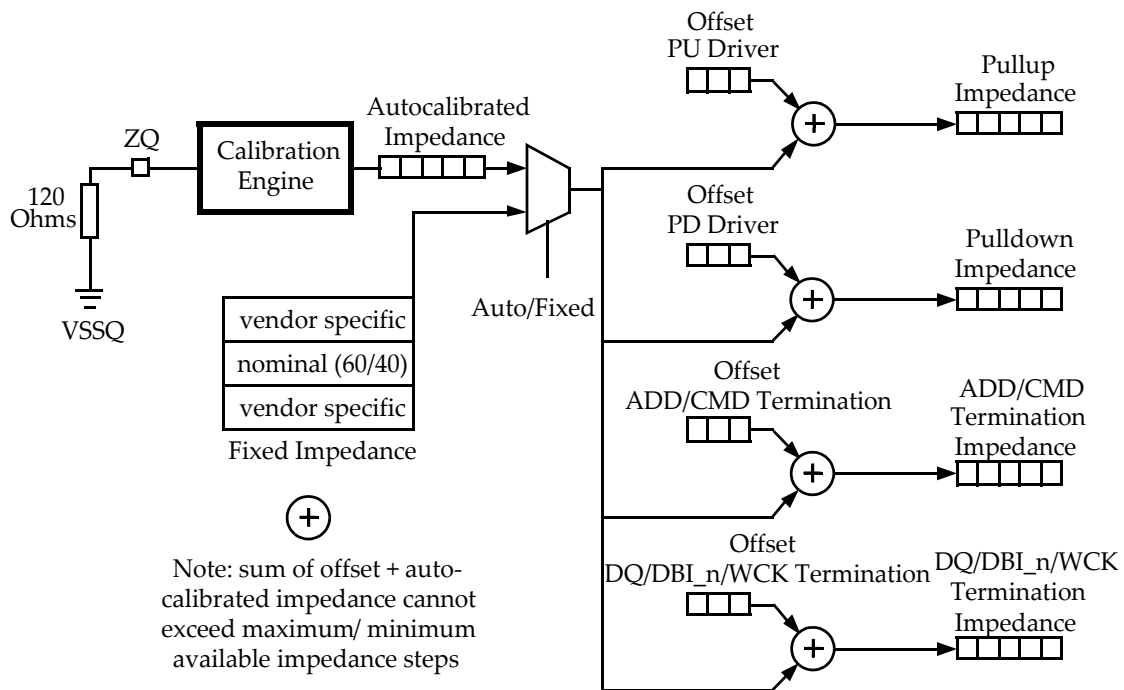


Figure 28 — Impedance Offsets

6.4 MODE REGISTER 3 (MR3)

Mode Register 3 controls functions including Bank Groups, WCK termination, self refresh, RDQS mode, DRAM Info and WCK2CK training as shown in Figure 29.

Mode Register 3 is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=0 and BA3=0.

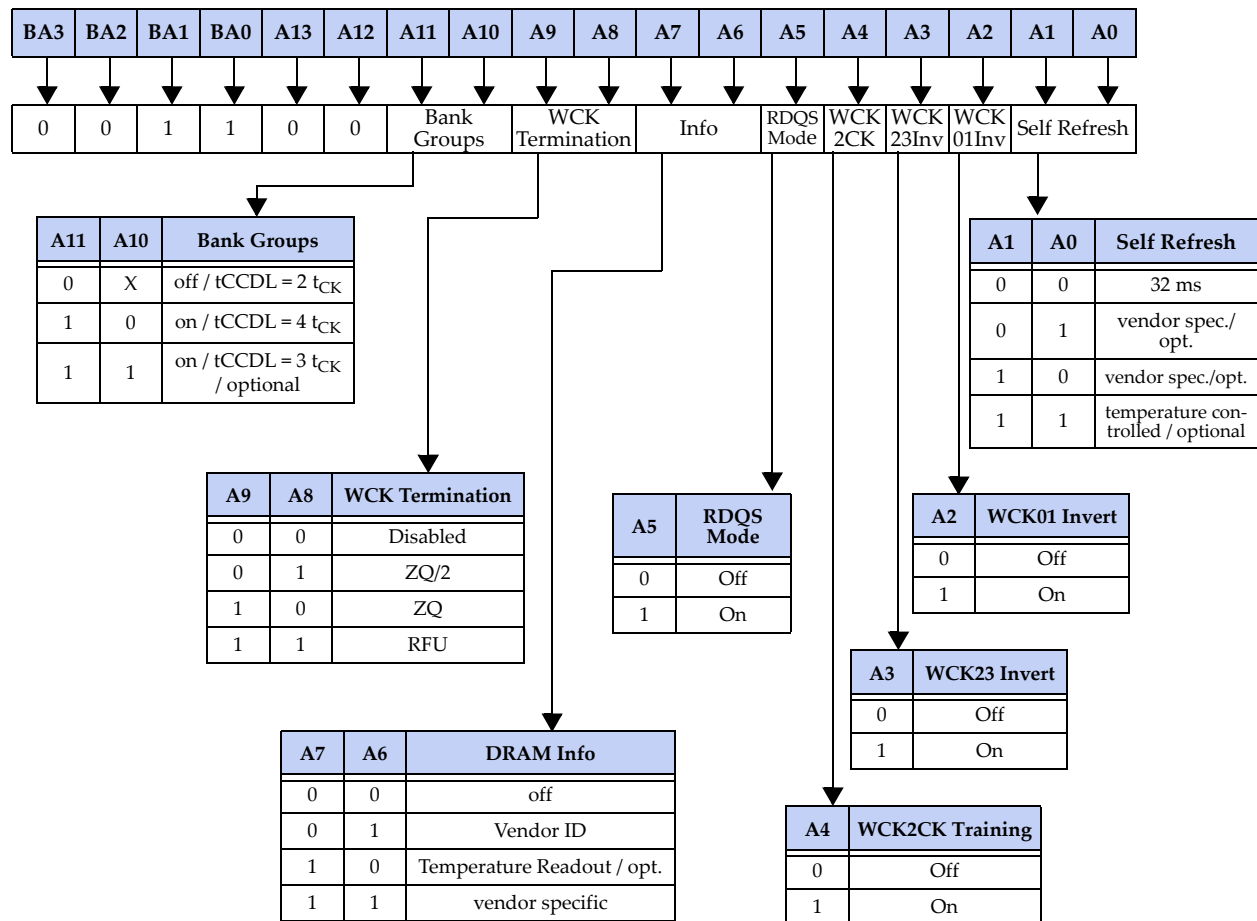


Figure 29 — Mode Register 3 (MR3) Definition

Self Refresh

The refresh interval in self refresh mode may be set to 32ms, or being controlled by an optional integrated temperature sensor. DRAM vendors may support additional settings related to other temperatures.

WCK2CK

Bit A4 (WCK2CK) enables and disables the WCK2CK alignment training. For details on this training sequence, see the section on TRAINING.

WCK01 / WCK23 Inversion

Bits A2 and A3 control whether the internal phase of the WCK01 and WCK23 clock inputs after internal divide-by-2 shall be inverted, corresponding to a 2 U.I. phase shift. The bits are used in conjunction with WCK2CK training mode.

6.4 MODE REGISTER 3 (MR3) (cont'd)

RDQS Mode

Bit A5 enables the RDQS mode of the device. In this mode the EDC pins will act as a READ strobe (RDQS). No CRC is supported in RDQS mode, and all related bits in MR4 will be ignored. A detailed description of the RDQS mode can be found in the section entitled OPERATION.

DRAM Info

Bits A6 and A7 enable the DRAM Info mode which is provided to output the Vendor ID, or optionally the current junction temperature or other vendor specific device info.

The Vendor ID identifies the manufacturer of the device, and provides the die revision, memory density and FIFO depth.

The Temperature Readout provides the SGRAM's junction temperature. Vendors may require that the related on-chip temperature sensor being enabled in advance by bit A6 in MR7.

WCK Termination

Bits A8 and A9 define the termination value for the on-die termination (ODT) for the WCK01_t, WCK01_c, WCK23_t and WCK23_c pins in combination with the driver strength setting.

The termination can be set to a value of $ZQ/2$ which is intended for a single loaded system, or ZQ which is intended for double load configurations with two devices sharing the WCK clocks. The WCK termination may also be turned off.

Bank Groups

Bit A11 enables the bank groups feature, and bit A10 specifies the min column-to-column command delay (t_{CCDL}). With A11 set to '1', back-to-back column accesses within a bank group have to be spaced by 3 or 4 clocks as defined by bit A10, with $3 t_{CK}$ being optional for the DRAM vendor. With A11 set to '0', the bank groups feature is disabled and t_{CCDL} equals t_{CCDS} .

The DRAM vendor's datasheet specifies the operating frequency limit below which the user may run the device without activating the bank groups feature (f_{CKBG}).