

JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP)

JESD216B

(Revision of JESD216A, July 2013)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman. It was derived from prior work done by Intel on their ‘Serial Flash Discoverable Parameters Guidelines’ document.

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members were volunteers from AMD, ASPEED, Emulex, HP, Intel, Macronix, Micron, Microchip, Sanyo, Spansion, and Winbond.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Special Function parameter tables for erase sector address map and 4-byte address instructions are added in this revision of this standard. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

(From JEDEC Board Ballot JCB-14-08, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory.)

1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, Standard Manufacturers Identification Code (contact jedec.org for the latest revision of this document)
2. NIST SP800-147, BIOS Protection Guidelines (<http://csrc.nist.gov/publications/nistpubs/>)

3 Terms and definitions

For the purposes of this standard, the following terms and definitions apply:

00b: The ‘b’ suffix indicates the ‘00’ digits are a binary representation of the number.

00h: The ‘h’ suffix indicates the ‘00’ digits are a hexadecimal representation of the number.

0x00: The ‘0x’ prefix indicates the ‘00’ digits are a hexadecimal representation of the number. This form is used in the ‘C’ sample code in Annexes.

Address: The three or four byte value following some instructions that is used to select a location within an address space of the flash memory.

3 Terms and definitions (cont'd)

Basic Parameter Table: The table pointed to by Parameter ID FF00h. Contains general information about the flash device's capabilities.

Block: A group of contiguous sectors.

Command: The combination of the instruction, address, optional mode bits, wait states, and data cycles used to initiate functions or transfer information between the controller and the serial flash.

Controller: The serial bus master

Double Transfer Rate (DTR): Instruction, address, and/or data may be input or output on both the rising and falling edges of the clock.

Dummy Cycles: Clock cycles during which no data is transferred to or from a memory.

DWORD: Four consecutive 8-bit bytes used as the basic 32-bit building block for headers and parameter tables.

Instruction: The one byte code used to initiate a function in the serial flash or identify the type of information transfer between the controller and the serial flash.

Mode Bits: Optional control bits that follow the address bits. These bits are driven by the controller if they are specified.

Wait States: Required clock cycles between the address bits or optional mode bits and the start of data when reading from the flash device. Some device data sheets describe these as dummy cycles because no information is transferred between the controller and memory during these cycles. Neither controller nor memory are required to drive the data lines during these cycles.

Read Latency: On flash read instructions, the total number of clocks between end of address and the start of data. The sum of clocks for mode bits and clocks for wait states equals the Read Latency.

Sector: The minimum granularity - size and alignment - of an area that can be erased in the data array of a flash memory device. Different areas within the address range of the data array may have a different minimum erase granularity (sector size).

(x-y-z): Command mode nomenclature used to indicate the number of active pins used for the instruction (x), address (y), and data (z). At the present time, the only valid Read SFDP command modes are: (1-1-1), (2-2-2), and (4-4-4)

4 Read SFDP Command Protocol

4.1 Instruction

The Read SFDP instruction code is 5Ah.

4.2 Address

Indicates the starting byte address in the SFDP area and is always expressed as a three byte field.

4.3 Wait States

Following the address, eight clocks are required before valid data is clocked out.

4.4 Clock Rate

SFDP compliant devices must support 50 MHz operation for the Read SFDP command (instruction 5Ah). Devices may support a wider frequency range, but a controller can always run SFDP cycles at 50 MHz or less and get valid results.

4.5 Command Modes

The Read SFDP command can be used with device supported modes of (1-1-1), (2-2-2), or (4-4-4), but the instruction (5Ah), address (24 bits), eight wait states, and 50 MHz requirements remain the same. Support for SFDP does not imply or require that the flash device support 2-2-2 or 4-4-4 mode. If the controller knows a priori the mode in which the flash device is configured, then it can issue the Read SFDP command in that mode. If the controller does not know, then a suggested algorithm is to try to read the SFDP signature (see 6.1) in 4-4-4 mode, if that fails try 2-2-2 mode, and if that fails try 1-1-1 mode.

Timing Diagram Signal Definitions:

- S# = Select, low active. Memory device selection signal also often referred to as Chip Select or Chip Enable
- C = Clock. Serial clock to the memory also often referred to as SCLK.
- DQ0 = Data input or output zero. The least significant memory data input or output also often referred to as IO0 or Serial Input (SI) when not used for two or four bit data I/O.
- DQ1 = Data input or output one. The next most significant memory data input or output above DQ0, also often referred to as IO1 or Serial Output (SO) when not used for two or four bit data I/O.
- DQ2 = Data input or output two. The next most significant memory data input or output above DQ1, also often referred to as IO2 or Write Protect, low active (WP#) when not used for four bit data I/O.
- DQ3 = Data input or output three. The most significant memory data input or output, also often referred to as IO3 or Hold, low active (HOLD#) when not used for four bit data I/O.

4.5.1 Read SFDP (1-1-1) Mode

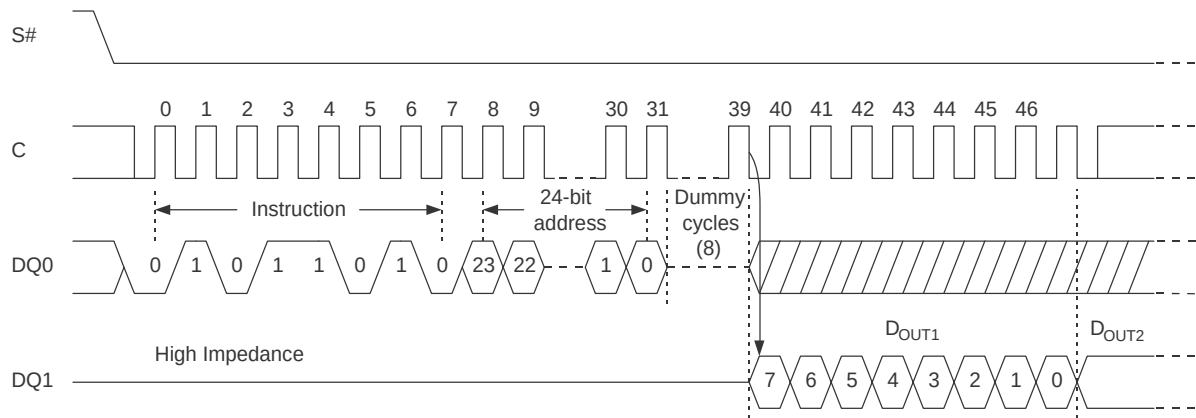


Figure 1 — Read SFDP (1-1-1) Mode Timing Diagram

4.5.2 Read SFDP (2-2-2) Mode

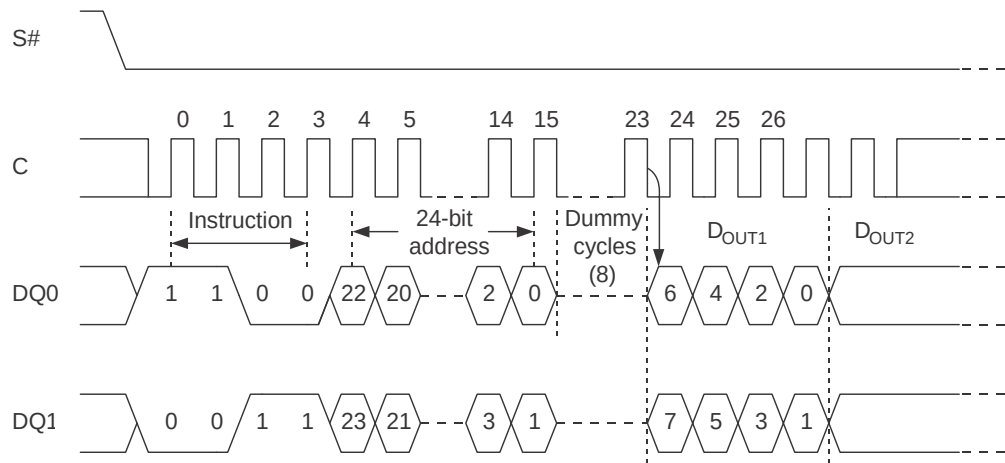


Figure 2 — Read SFDP (2-2-2) Mode Timing Diagram

4.5.3 Read SFDP (4-4-4) Mode

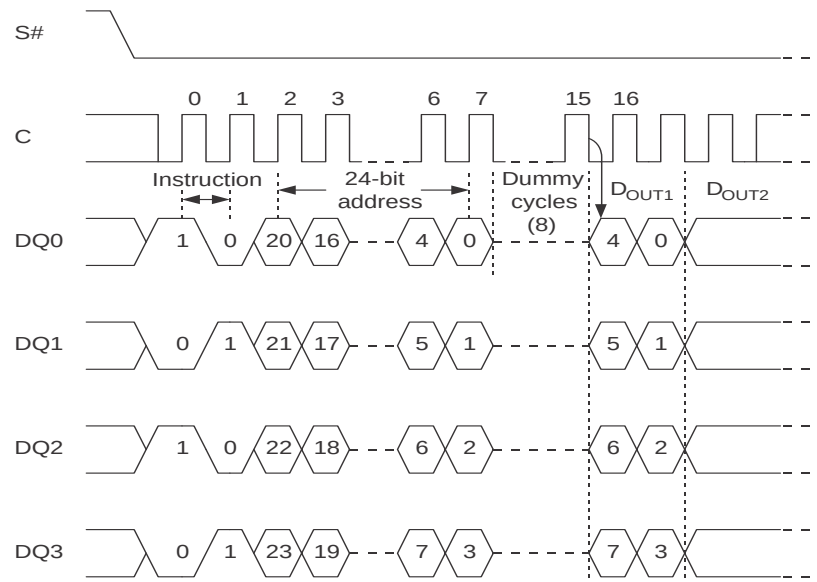


Figure 3 — Read SFDP (4-4-4) Mode Timing Diagram

5 Read SFDP Behavior

5.1 Security

The SFDP and flash memory address ranges must never overlap. This ensures that address range checking the controller may perform to prevent access to security keys or other sensitive information stored in flash cannot be bypassed. Also, for PC BIOS applications non-overlap is required to comply with NIST SP800-147.

Addresses beyond the end of the SFDP tables must not alias into the flash memory. Regardless of the implementation, writes to SFDP tables must be permanently disabled before the memory device is released to a customer by the memory vendor factory.

5.2 Reset and Hold Functions

Reset and Hold functionality will be available during the Read SFDP command if the memory device command mode supports these features.

5.3 Read Wrap

Not supported with the Read SFDP command—even when a memory device defaults to Read Wrap-around mode for other read commands. Only continuous (sequential) read is supported with the Read SFDP command.

5.4 SFDP Address Boundary Wrap

Device behavior when the Read SFDP command crosses the SFDP structure boundary is not defined except for the security restriction specified in 5.1. There is no requirement for the address counter to wrap back to the beginning of the structure and the data read after that point is not specified.

5.5 Reserved SFDP Locations

The content of reserved SFDP locations (memory within the SFDP address space that has not yet been defined or used) is not specified, but recommended to be all FFh.

6 SFDP Database

6.1 SFDP Header Structure

The format of the SFDP header is shown in Figure 4.

	[31:24]	[23:16]	[15:8]	[7:0]	Hex byte location
SFDP Header	Serial Flash Discoverable Parameters (SFDP) Signature = 50444653h				[3h:0h]
	Byte 3 = "P"	Byte 2 = "D"	Byte 1 = "F"	Byte 0 = "S"	
	Unused (set to FFh)	Number of Parameter Headers (NPH)	SFDP Major Revision	SFDP Minor Revision	[7h:4h]
1 st Parameter Header	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB JEDEC ID (00h)	[Bh:8h]
	Parameter ID MSB JEDEC ID (FFh)	Parameter Table Pointer (byte address)			[Fh:Ch]
2 nd Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	[13h:10h]
	Parameter ID MSB	Parameter Table Pointer (byte address)			[17h:14h]
...					
Nth Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	
	Parameter ID MSB	Parameter Table Pointer (byte address)			

Figure 4 — Overall Header Structure

6.2 SFDP Header

The SFDP Header is located at address 000000h of the SFDP data structure. It identifies the SFDP Signature, the number of parameter headers, and the SFDP revision numbers.

Both the SFDP header and the individual parameter table headers include Major and Minor revision numbers.

Major revisions require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. For example, changes that reorganize previously defined fields.

Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields.

JESD216B maintains backwards compatibility with JESD216A, defines previously reserved bits in DWORD 15 of the Basic Flash Parameter Table and adds optional Function Specific table definitions.

The revision numbers of vendor-defined and Function Specific tables follow the same guidelines as the Basic Parameter Table.

Major vs. Minor Revisions

Major revisions indicate that the table structure has changed and may not be backwards compatible with software written for an earlier revision of SFDP.

Increments of minor revisions indicate that fields or DWORDS have been added but the definition of existing fields is unchanged. Software should accept any minor revision number and read only the number of parameter table fields that the software requires. Users should accept any minor revision greater than or equal to the current revision. All fields in current tables will be unchanged in subsequent minor revisions.

6.2.1 SFDP Header: 1st DWORD

Bits	Description
31:0	SFDP Signature Allows a user to know that the information is valid. Signature[31:0]: 50444653h

6.2 SFDP Header (cont'd)

6.2.2 SFDP Header: 2nd DWORD

Bits	Description
31:24	Unused Contains FFh and can never be changed.
23:16	Number of Parameter Headers (NPH) Specifies the number of parameter headers in the SFDP data structure. This number is 0-based. Therefore, 0 indicates 1 parameter header. The value of this field is not defined by this standard. It is dependent on the number of tables a vendor implements.
15:8	SFDP Major Revision Number This 8-bit field indicates the major revision number of this standard. The value in this field is 1 for devices which implement the JESD216B revision. NOTE The value of this field may only be changed by an update to the JESD216 standard.
7:0	SFDP Minor Revision Number This 8-bit field indicates the minor revision number of this standard. The value in this field is 6 for devices which implement the JESD216B revision. NOTE The value of this field may only be changed by an update to the JESD216 standard.

6.3 Parameter Headers

Each Parameter Header identifies the size, location, revision, ownership and function of their associated parameter tables. Parameter table ownership will be either JEDEC (via this standard) or an individual vendor (via vendor specific documentation).

Multiple parameter headers can be specified with each parameter header being 2 DWORDs (64-bits). The first parameter header is mandatory, is defined by this standard, and starts at byte offset 08h. If a vendor chooses to include multiple revisions of the Basic Parameter Table they may do so provided the table headers are in order starting with the oldest version. The total number of parameter headers is specified in the NPH field of the SFDP header, see 6.2. All subsequent parameter headers need to be contiguous and may be specified by JEDEC or by vendors using the same structure (shown in Figure 4). Minor revisions may overlap earlier revisions by starting at the same address as an earlier revision but have additional length for parameters added in the later revision. This allows the use of legacy parameters without the need to repeat them in each new minor revision.

6.3 Parameter Headers (cont'd)

6.3.1 Parameter Header: 1st DWORD

Bits	Description
31:24	Parameter Table Length This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	Parameter Table Major Revision Number* This 8-bit field indicates the major revision number of the associated parameter table. NOTE Major Revision starts at 01h. The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard. The Major Revision of a vendor-specified table is controlled by that vendor.
15:8	Parameter Table Minor Revision Number* This 8-bit field indicates the minor revision number of the associated parameter table. NOTE Minor Revision starts at 00h. The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard. The Minor Revision of a vendor-specified table is controlled by that vendor.
7:0	Parameter ID LSB: Refer to Definition of Parameter ID Field in 6.3.3.
* See "Major vs. Minor Revisions" in 6.2	

6.3.2 Parameter Header: 2nd DWORD

Bits	Description
31:24	Parameter ID MSB Refer to Definition of Parameter ID Field in 6.3.3.
23:0	Parameter Table Pointer (PTP) This address specifies the start of this header's Parameter Table in the SFDP structure. This is a byte address and must be DWORD-aligned.

6.3.3 Definition of Parameter ID Field

The Parameter ID indicates the parameter table ownership and type.

Parameter ID MSB	Parameter ID LSB	type	owner
01h – 7Fh	odd parity	Vendor specific	Vendor
01h – 7Fh	even parity	Function specific	Vendor
80h – FFh	even parity	Function specific	JEDEC JC42.4
FFh	00h	Basic Parameter Table	JEDEC JC42.4

Function Specific tables may be defined by the JC-42.4 Committee or a manufacturer (vendor). The purpose of the Function Specific tables is to allow development of features and associated parameter tables common to multiple manufacturers, prior to the parameter tables being incorporated into the next revision of JESD216. Allocation of IDs for Function Specific tables is requested through the JEDEC office, see Annex C.

6.3.3 Definition of Parameter ID Field (cont'd)

Vendor Specific table structure is defined by the identified device vendor. The parameter table ID field identifies the vendor that owns the table definition.

The original JESD216 specification used only a one byte ID field to identify the parameter table owner. JESD216 revision A expanded the ID field to two bytes, MSB and LSB, because a single byte is insufficient to uniquely identify all manufacturers (vendors). The original single byte parameter ID is now referred to as the parameter ID LSB.

The Parameter ID LSB value of 00h is reserved for the Basic Parameter Table defined by this standard. For backwards compatibility the MSB is FFh when the LSB is 00h and LSB 00h shall not be used when the MSB is any value other than FFh. This is because some legacy systems using the original JESD216 may ignore the MSB and assume any parameter ID with LSB of 00h is the Basic Parameter Table.

Parameter IDs with:

- An MSB of 01h through 7Fh indicates a Vendor Owned table and provides the bank number of a JEDEC JEP106 assigned Manufacturer ID.
 - 00h is reserved because JEP106 bank numbering begins at 01h
 - The JEP106 Manufacturer's Identification Code LSB is an eight (8) bit field, consisting of seven (7) data bits plus one (1) odd parity bit in the most significant bit position. A Parameter ID LSB with odd parity signifies a Manufacturer's Identification Code and a Parameter ID LSB with even parity signifies a Function Specific table.
- An MSB of 80h through FFh indicates a Function Specific or Basic Parameter Table defined by the JEDEC 42.4 committee. The LSB is used to identify the Function Specific table type.
 - Any parameter ID with LSB 00h identifies the SPI protocol Basic Parameter Table.
 - LSB values with even parity are Function Specific tables that are defined by the JC-42.4 committee.
 - LSB values with odd parity are illegal to prevent any confusion with JEP106 Manufacturer ID values.

6.3.3.1 Function Specific parameter table ID assignments:

Description	ID (Hex)
Basic SPI protocol	FF00
Sector map	FF81
Replay Protected Monotonic Counters	FF03
4-byte Address Instruction Table	FF84
Reserved for next Function Specific Table assignment	FF05

6.3.4 Example SFDP Headers (Note the definition and discussion of Parameter Headers in 6.3)

Figure 5 shows an example of a basic SFDP Header (major revision 1, minor revision 6): one Parameter Header, Parameter Table length of 16 DWORDs, 1st Parameter Header Revision 1.6, JEDEC ID of FF00h, and the Parameter Table Pointer pointing to location 000010h. This header is backwards compatible with previous generations of this standard, therefore devices are not required to contain headers with prior revision numbers.

6.3.4 Example SFDP Headers (cont'd)

In Figure 6, the first parameter header points to a version 1.0 format Basic Parameter Table of 9 DWORDs starting at location 100h and the second parameter headers both points to a separate version 1.6 format Basic Parameter Table of 16 DWORDs starting at location 200h.

Figure 7 adds one of the Optional Function Specific headers introduced in JESD216B. This third header indicates that this device supports 4-byte address instructions functionality.

In Figure 6 and Figure 7, devices that do not have the functionality of these features may not contain these additional parameters.

Example calculation using the Parameter Table Pointer (PTP):

- The PTP is a byte address. The fields within this document are defined in terms of DWORDS.
- To calculate the byte address of a particular field, given a PTP of 100h:
- The SFDP byte address of DWORD 3 = $100h + ((3-1) * 4) = 100h + 2 * 4 = 100h + 8 = 108h$

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	00h	01h	06h	< [7h:4h]
1st Parameter Header	10h	01h	06h	00h	< [Bh:8h]
	FFh	00h	00h	10h	< [Fh:Ch]

Figure 5 — Example SFDP Header with single Basic Parameter Table

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	01h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]

Figure 6 — Example SFDP Header with two Basic parameter Tables

6.3.4 Example SFDP Headers (cont'd)

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	02h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]
3rd Parameter Header	02h	01h	00h	84h	< [1Bh:18h]
	FFh	00h	02h	80h	< [1Fh:1Ch]

Figure 7 — Example SFDP Header with two basic Parameter Tables and one optional (4-Byte Address) Function Specific Table

6.4 JEDEC Basic Flash Parameter Header and Table

Parameter tables contain coded information describing the features and capabilities of the serial flash. The first parameter table as defined by JEDEC is mandatory and its starting address is specified by the PTP field of the 1st Parameter Header. This table identifies some of the basic features of SPI protocol flash memory devices.

6.4.1 JEDEC Basic Flash Parameter Header: 1st DWORD

Bits	Description
31:24	Parameter Table Length This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	Parameter Table Major Revision Number This 8-bit field indicates the major revision number of the parameter table. The value in this field is 1 for this table defined by JESD216B revision. NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.
15:8	Parameter Table Minor Revision Number This 8-bit field indicates the minor revision number of the Sector Map parameter table. The value in this field is 6 for this table defined by JESD216B revision. NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	Parameter ID LSB The JEDEC Basic Flash Parameter Table is assigned the ID LSB of 00h.