

JEDEC STANDARD

Serial Flash Discoverable Parameters (SFDP)

JESD216F.02

(Editorial Revision of JESD216F.01, February 2022)

JUNE 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Foreword

This standard was prepared by the JEDEC SFDP Task Group authorized by the JC-42.4 Committee Chairman.

The intended audience is serial flash vendors and engineers writing device drivers for SFDP compliant serial flash devices.

The participating SFDP TG members included volunteers from Adesto, Infineon, Giga Device, Intel, ISSI, Macronix, Micron, Microchip, NXP, Sanyo, and Winbond.

Introduction

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors.

The SFDP standard defines a common parameter table describing important device characteristics and serial access methods used to read the parameter table data. Optional Special Function parameter tables for erase sector address map and 4-byte address instructions are included. In the JESD216D revision are optional Special Function parameter tables for the JEDEC x4 (Quad) eXtended Serial Peripheral Interface (x4 xSPI). New in the JESD216E revision is a description of the Replay Protected Monotonic Counter (RPMC) functionality and also descriptions of the Secure Read and Secure Write packet transfer transactions. Additional parameter headers and tables can be specified by future revisions of this standard or by flash vendors and are optional.

SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP) STANDARD

From JEDEC Board Ballot JCB-21-49, formulated under the cognizance of the JC-42.4 Committee on Nonvolatile Memory, item 1775.73.

1 Scope

The SFDP standard defines the structure of the SFDP database within the memory device and methods used to read its data.

The JEDEC-defined header with Parameter ID FF00h and the related Basic Parameter Table is mandatory. This header and table provide basic information for a Serial Peripheral Interface (SPI) protocol memory. Additional headers and tables are optional.

The read command protocol using various I/O modes and standard clock rate are specified. The device electrical parameters are not specified.

2 Normative Reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents listed. For undated references, the latest edition of the normative document referred to applies.

1. JEP106, *Standard Manufacturers Identification Code* (see www.jedec.org for latest revision)
2. NIST SP800-147, *BIOS Protection Guidelines* (<http://nvlpubs.nist.gov/nistpubs/Legacy/SP/nistspecialpublication800-147.pdf>)
3. JEDEC Standard JESD251, *eXpanded Serial Peripheral Interface (xSPI) for Non Volatile Memory Devices* as approved by JC42.4 committee in the June 2017 meeting.

JEDEC Standard JESDxxx, *SPI Protocol Reset (Serial Peripheral Interface - Flash Hardware Reset Method, Not Requiring a Dedicated Reset Signal Input)*, **This document is in development.**

4. JEDEC Standard JESD230C, *NAND Flash Interface Interoperability*

3 Terms and Definitions

For the purposes of this standard, the following terms and definitions apply.

00b: The ‘b’ suffix indicates the ‘00’ digits are a binary representation of the number.

00h: The ‘h’ suffix indicates the ‘00’ digits are a hexadecimal representation of the number.

address: The three or four byte value following some instructions that is used to select a location within an address space of the flash memory.

basic parameter table: The table pointed to by Parameter ID FF00h. Contains general information about the flash device's capabilities.

block: A group of contiguous sectors.

command: The combination of the instruction, address, optional mode bits, wait states, and data cycles used to initiate functions or transfer information between the controller and the serial flash.

controller: The serial bus initiator

Double Transfer Rate (DTR): Instruction, address, and/or data may be input or output on both the rising and falling edges of the clock. NOTE: The term “Double Data Rate” (DDR) may also be encountered in some documentation.

Data Strobe (DS): Target to initiator strobe signal used to capture data sent by the target.

dummy cycles: Clock cycles during which no data is transferred to or from a memory.

DWORD: Four consecutive 8-bit bytes used as the basic 32-bit building block for headers and parameter tables.

instruction: The one byte code used to initiate a function in the serial flash or identify the type of information transfer between the controller and the serial flash.

mode bits: Optional control bits that follow the address bits. These bits are driven by the controller if they are specified.

wait states: Required clock cycles between the address bits or optional mode bits and the start of data when reading from the flash device. Some device data sheets describe these as dummy cycles because no information is transferred between the controller and memory during these cycles. Neither controller nor memory are required to drive the data lines during these cycles.

read latency: On flash read instructions, the total number of clocks between end of address and the start of data. The sum of clocks for mode bits and clocks for wait states equals the Read Latency.

sector: The minimum granularity - size and alignment - of an area that can be erased in the data array of a flash memory device. Different areas within the address range of the data array may have a different minimum erase granularity (sector size).

3 Terms and Definitions (cont'd)

(x-y-z): Command mode nomenclature used in JESD216A and JESD216B to indicate the number of active pins used for the instruction (x), address (y), and data (z). For new entries in the current standard, this is replaced by the (An-Bn-Cn) nomenclature described below. The (x-y-z) nomenclature is equivalent to (AS-BS-CS) unless otherwise noted. (4-4-4) is therefore equivalent to (4S-4S-4S).

(An-Bn-Cn): Command mode nomenclature used to indicate the number of active pins used for the instruction (A), address (B), and data (C), and the data rate used for each. Data rates(n) can be single (S) and dual (D). At the present time, the only valid Read SFDP command modes are: (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), (4S-4D-4D), and (8D-8D-8D). (4S-4D-4D), and (8D-8D-8D) modes also use a Data Strobe (DS) as part of the communication protocol.

4 Read SFDP Command Protocol

4.1 Instruction

The Read SFDP instruction code is 5Ah.

- The very first SFDP instruction a Device receives from a Host is the READ SFDP (5Ah) instruction during POR discovery phase.

The Fetch SFDP instruction code is 5Bh.

- This instruction is added to support Long Latency NVM Devices. This instruction tells a Device to load all parameter tables, defined in SFDP Header Structure, from device Memory Cell Array to Device Cache Buffer. NAND Flash device is the first Long Latency NVM device supported by SFDP. Host shall wait for 120 μ s tR (Read Latency) then Host can re-issue Read SFDP (5Ah) instruction to access SFDP parameter table and Long Latency NVM device MSPT (Media Specific Parameter Table) table.
- Fetch SFDP (5Bh) instruction shall follow the same mode established between a Host and a Device during POR Read SFDP (5Ah) instruction phase.

NOTE Fetch SFDP instruction is only applicable for POR device discovery process for now. If needed, additional details of normal connected operation description would be available after JEDEC SPI NAND document is available.

4.2 Address

Indicates the starting byte address in the SFDP area and is always expressed as a three byte field for (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), and (4S-4D-4D) modes. For the (8D-8D-8D) mode, 3 or 4 byte addressing may be used.

- Fetch SFDP (5Bh) instruction does not have or require an address field.

4.3 Wait States

Following the address, eight clocks are required before valid data is clocked out for (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), and (4S-4D-4D) modes. For the (8D-8D-8D) mode, a variable number of wait states (dummy cycles) may be used.

- Not applicable for Fetch SFDP (5Bh) instruction since it does not have an address field and does not output data.

4.4 Clock Rate

SFDP compliant devices must support 50 MHz operation for the Read SFDP command (instruction 5Ah). Devices may support a wider frequency range, but a controller can always run SFDP cycles at 50 MHz or less and get valid results.

- Fetch SFDP (5Bh) instruction shall follow the same mode established between a Host and a Device during Read SFDP (5Ah) instruction phase.

4.5 Command Modes

The Read SFDP command can be used with device supported modes of (1S-1S-1S), (2S-2S-2S), (4S-4S-4S), or (4S-4D-4D), but the instruction (5Ah), address (24 bits), eight wait states, and 50 MHz requirements remain the same. For the (8D-8D-8D) mode, the instruction (5Ah) and 50 MHz requirements remain the same, while 24 or 32 address bits, and a variable number of wait states (dummy cycles) may be used. Support for SFDP does not imply or require that the target device supports 2S-2S-2S, 4S-4S-4S, 8S-8S-8S or 8D-8D-8D mode. If the controller knows a priori the mode in which the flash device is configured, then it can issue the Read SFDP command in that mode. If the controller does not know, then a suggested algorithm is to try to read the SFDP signature (see 6.1) in 4S-4S-4S mode, if that fails try 2S-2S-2S mode, and if that fails try 1S-1S-1S mode. For Octal devices, these typically support SFDP read operation in both 1S-1S-1S mode and 8D-8D-8D mode. If the host controller does not know exactly which protocol mode is used for SFDP in 8D-8D-8D mode, this information can be found by reading SFDP in 1S-1S-1S mode first. (To read an unknown device directly in 8D-8D-8D mode, the host controller may read from address 0, and count the number of dummy clocks required before the SFDP signature is received.)

- Fetch SFDP (5Bh) instruction shall follow the same mode established between a Host and a Device during Read SFDP (5Ah) instruction phase.

4.5 Command Modes (cont'd)

Timing Diagram Signal Definitions:

- CS# = Select, low active. Memory device selection signal also often referred to as Chip Select or Chip Enable
- CK = Clock. Serial clock to the memory also often referred to as SCLK.
- IO0 = Data input or output zero. The least significant memory data input or output also often referred to as DQ0 or Serial Input (SI) when not used for two, four or eight bit data I/O.
- IO1 = Data input or output one. The next most significant memory data input or output above IO0, also often referred to as DQ1 or Serial Output (SO) when not used for two, four or eight bit data I/O.
- IO2 = Data input or output two. The next most significant memory data input or output above IO1, also often referred to as DQ2 or Write Protect, low active (WP#) when not used for four or eight bit data I/O.
- IO3 = Data input or output three. The most significant memory data input or output, also often referred to as DQ3 or Hold, low active (HOLD#) when not used for four or eight bit data I/O.
- IO4-7 = Data input or output four to seven. Used for eight bit data I/O (8D-8D-8D). Also often referred to as DQ4-7.
- DS = Data Strobe. Used for (4S-4D-4D) and (8D-8D-8D). The Data Strobe (DS) signal provides a timing reference for information transfer on the IO signals from the target to the initiator. DS is an output signal from the xSPI target device that is aligned with the edges of output data and is used by the host interface to optimize high frequency read data capture. DS may optionally be used as a signal from the target to the initiator, to indicate the duration of initial access latency or, as a signal from the initiator to the target, to indicate write data masking.

4.5.1 Read SFDP (1S-1S-1S) Mode

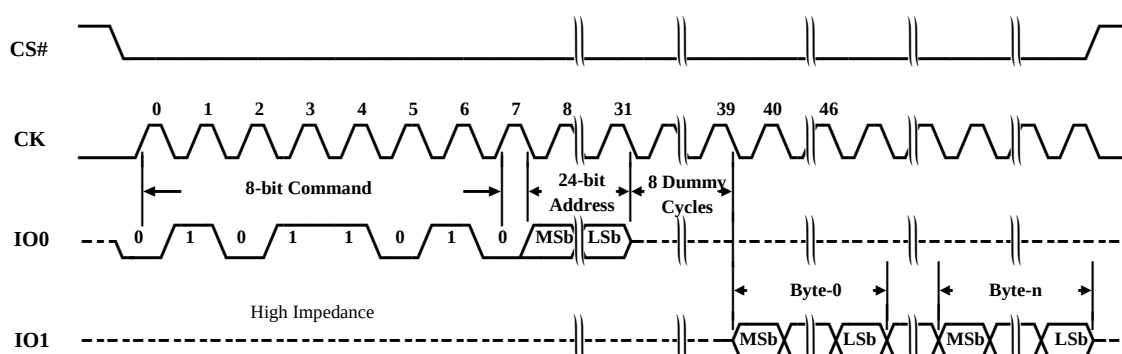


Figure 1 — Read SFDP (1S-1S-1S) Mode Timing Diagram

4.5.2 Read SFDP (2S-2S-2S) Mode

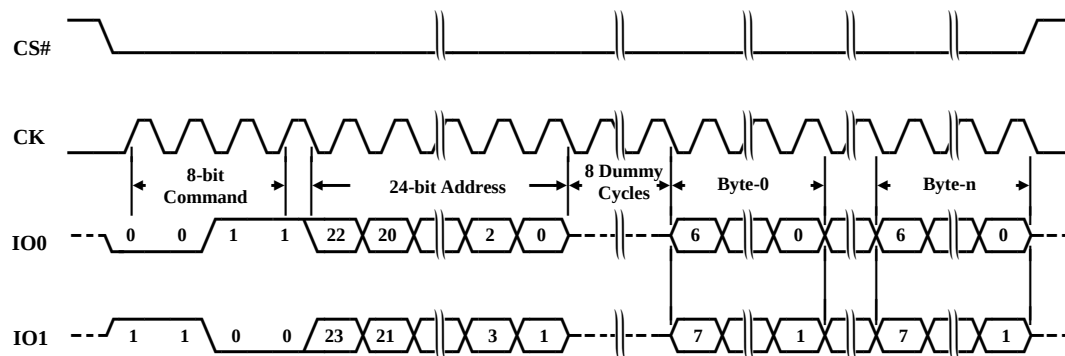


Figure 2 — Read SFDP (2S-2S-2S) Mode Timing Diagram

4.5.3 Read SFDP (4S-4S-4S) Mode

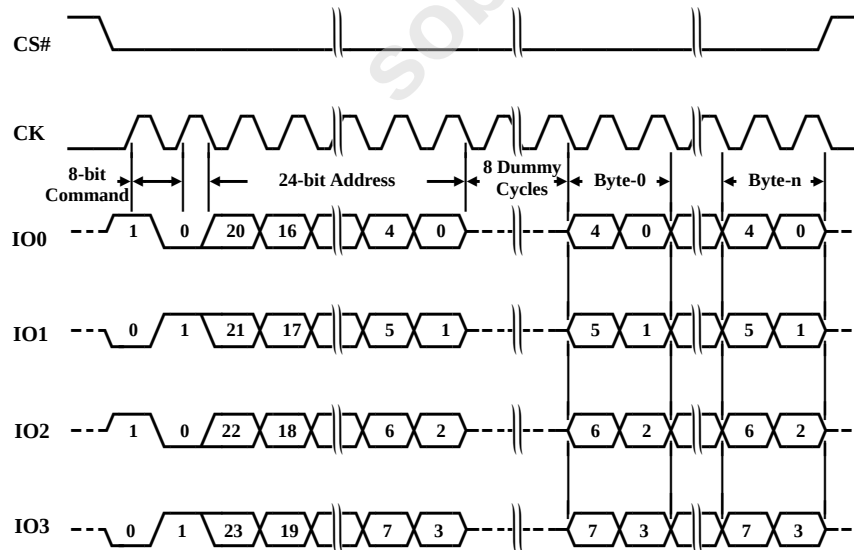
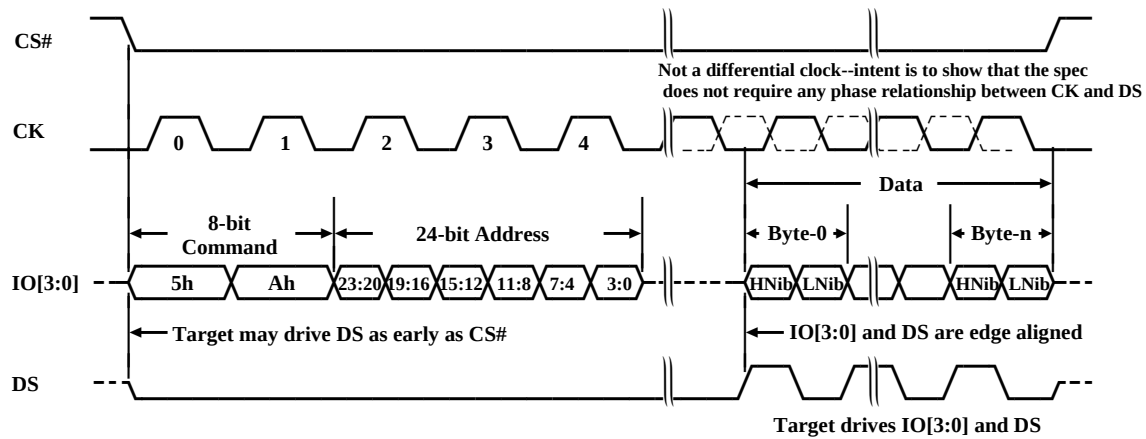


Figure 3 — Read SFDP (4S-4S-4S) Mode Timing Diagram

4.5.4 Read SFDP (4S-4D-4D) Mode



NOTE DS is optional in this mode.

Figure 4 — Read SFDP (4S-4D-4D) Mode Timing Diagram

4.5.5 Read SFDP (8D-8D-8D) Mode

See 6.4.21 for details about the addressing options in this mode.

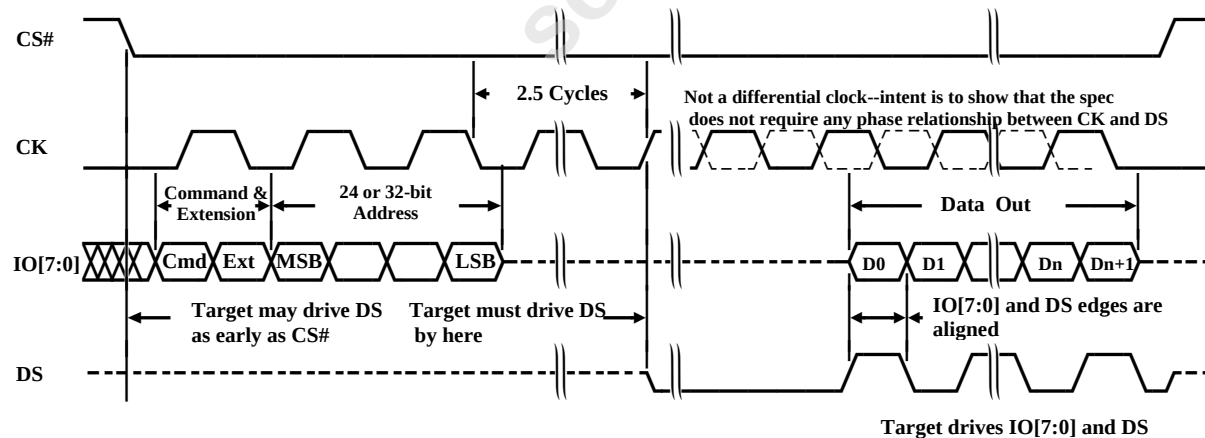


Figure 5 — Read SFDP (8D-8D-8D) Mode Timing Diagram

4.5.6 Fetch SFDP (1S-1S-1S) Mode

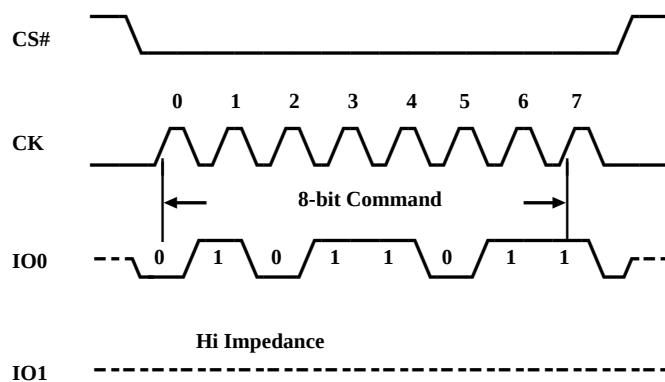


Figure 6 — Fetch SFDP (1S-1S-1S) Mode Timing Diagram

4.5.7 Fetch SFDP (2S-2S-2S) Mode

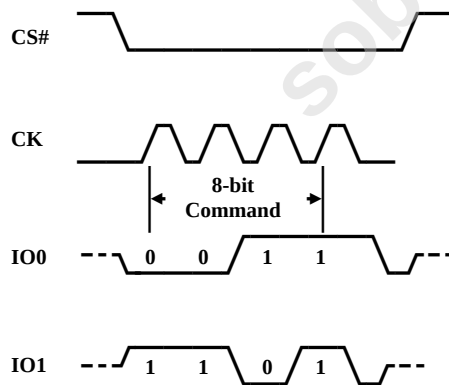


Figure 7 — Fetch SFDP (2S-2S-2S) Mode Timing Diagram

4.5.8 Fetch SFDP (4S-4S-4S and 4S-4D-4D) Mode

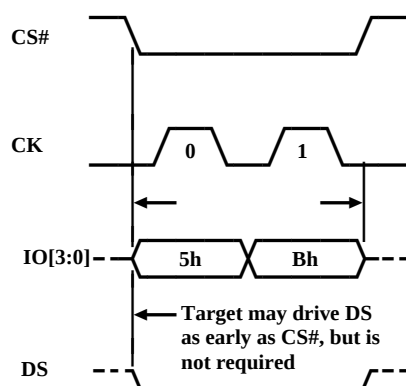


Figure 8 — Fetch SFDP (4S-4S-4S and 4S-4D-4D) Mode Timing Diagram

4.5.9 Fetch SFDP (8D-8D-8D) Mode

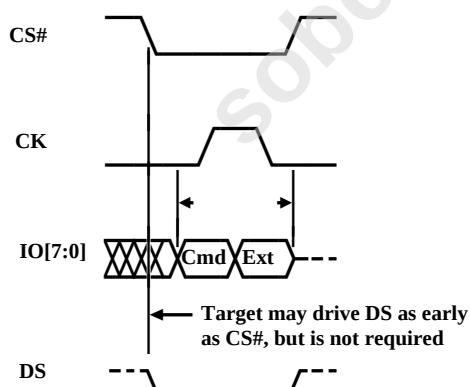


Figure 9 — Fetch SFDP (8D-8D-8D) Mode Timing Diagram

5 Read SFDP Behavior

5.1 Security

The SFDP and flash memory address ranges must never overlap. This ensures that address range checking the controller may perform to prevent access to security keys or other sensitive information stored in flash cannot be bypassed. Also, for PC BIOS applications non-overlap is required to comply with NIST SP800-147.

Addresses beyond the end of the SFDP tables must not alias into the flash memory. Regardless of the implementation, writes to SFDP tables must be permanently disabled before the memory device is released to a customer by the memory vendor factory.

5.2 Reset and Hold Functions

Reset and Hold functionality will be available during the Read SFDP command if the memory device command mode supports these features. Note that these functions may not be available in all modes, as the pins used for Reset or Hold may be reused for I/O pins in Quad and Octal modes.

The JEDEC SPI Protocol Reset is an alternative Reset function that may be used in any mode for devices which support it. See the JEDEC SPI Protocol Reset spec for details.

5.3 Read Wrap

Not supported with the Read SFDP command--even when a memory device defaults to Read Wrap-around mode for other read commands. Only continuous (sequential) read is supported with the Read SFDP command.

5.4 SFDP Address Boundary Wrap

Device behavior when the Read SFDP command crosses the SFDP structure boundary is not defined except for the security restriction specified in 5.1. There is no requirement for the address counter to wrap back to the beginning of the structure and the data read after that point is not specified.

5.5 Reserved SFDP Locations

The content of reserved SFDP locations (memory within the SFDP address space that has not yet been defined or used) is not specified, but recommended to be all FFh.

6 SFDP Database

6.1 SFDP Header Structure

The format of the SFDP header is shown in Figure 10 — Overall Header Structure

	[31:24]	[23:16]	[15:8]	[7:0]	Hex byte location
SFDP Header	Serial Flash Discoverable Parameters (SFDP) Signature = 50444653h Byte 3 = "P" Byte 2 = "D" Byte 1 = "F" Byte 0 = "S"				[3h:0h]
	SFDP Access Protocol	Number of Parameter Headers (NPH)	SFDP Major Revision	SFDP Minor Revision	[7h:4h]
1 st Parameter Header	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB JEDEC ID (00h)	[Bh:8h]
	Parameter ID MSB JEDEC ID (FFh)	Parameter Table Pointer (byte address)			[Fh:Ch]
2 nd Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	[13h:10h]
	Parameter ID MSB	Parameter Table Pointer (byte address)			[17h:14h]
...					
Nth Parameter Header (optional)	Parameter Length (in double words)	Parameter Major Revision	Parameter Minor Revision	Parameter ID LSB	
	Parameter ID MSB	Parameter Table Pointer (byte address)			

Figure 10 — Overall Header Structure

6.2 SFDP Header

The SFDP Header is located at address 000000h of the SFDP data structure. It identifies the SFDP Signature, the number of parameter headers, and the SFDP revision numbers.

Both the SFDP header and the individual parameter table headers include Major and Minor revision numbers.

Major revisions require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. For example, changes that reorganize previously defined fields.

Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields.

JESD216B maintains backwards compatibility with JESD216A, defines previously reserved bits in the 15th DWORD of the Basic Flash Parameter Table and adds optional Function Specific table definitions.

JESD216C maintains backwards compatibility with JESD216B, defines previously reserved bits in the 2nd DWORD of the SFDP Header and adds optional Function Specific table definitions.

JESD216D maintains backwards compatibility with JESD216C.

JESD216E maintains backwards compatibility with JESD216D, defines Secure Read and Secure Write transaction details as well as Replay Protected Monotonic Counter (RPMC) functionality.

The revision numbers of vendor-defined and Function Specific tables follow the same guidelines as the Basic Parameter Table.

Major versus Minor Revisions

Major revisions indicate that the table structure has changed and may not be backwards compatible with software written for an earlier revision of SFDP.

Increments of minor revisions indicate that fields or DWORDS have been added but the definition of existing fields is unchanged. Software should accept any minor revision number and read only the number of parameter table fields that the software requires. Users should accept any minor revision greater than or equal to the current revision. All fields defined in the current tables will be unchanged in subsequent minor revisions. Undefined or reserved fields may be updated.

6.2.1 SFDP Header: 1st DWORD

Bits	Description
31:0	SFDP Signature Allows a user to know that the information is valid. Signature[31:0]: 50444653h

6.2.2 SFDP Header: 2nd DWORD

Bits	Description
31:24	SFDP Access Protocol See 6.2.3
23:16	Number of Parameter Headers (NPH) Specifies the number of parameter headers in the SFDP data structure. This number is 0-based. Therefore, 0 indicates 1 parameter header. The value of this field is not defined by this standard. It is dependent on the number of tables a vendor implements. The value FFh is reserved for future extensions of this standard.
15:8	SFDP Major Revision Number This 8-bit field indicates the major revision number of this standard. The value in this field is 01h for devices which implement the JESD216F revision (unchanged from JESD216D revision). NOTE The value of this field may only be changed by an update to the JESD216 standard.
7:0	SFDP Minor Revision Number This 8-bit field indicates the minor revision number of this standard. The value in this field is 0Ah for devices which implement the JESD216F revision. NOTE The value of this field may only be changed by an update to the JESD216 standard.

6.2.3 Definition of SFDP Access Protocol Field

The purpose of the Access Protocol Field is to provide the host controller necessary information about how to read the SFDP command. In early versions of this spec (up to and including JESD216B) this field was FFh. The value FFh still indicates that the SFDP command structure is backwards compatible with the description given in JESD216B. The device will in this case respond to one or more of the SFDP command options as described in JESD216B. Any other value indicates that the SFDP command will behave differently in one or more aspects.

(8D-8D-8D) devices still use FFh as the parameter value if they boot up in one of the modes that are compatible with the JESD216B revision. (Typically this would be (1S-1S-1S) mode.)

For devices where the boot mode may be changed by the user by setting fuses or similar, the device has to update the value returned in the SFDP Access Protocol Field according to the fuse settings.

SFDP Command Parameter Value		
Decimal	Hex	
0-239	00h-EFh	Reserved for future use
240	F0h	xSPI NAND class-1 device – parameter data is available in device cache buffer. xSPI Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT. Follow Long latency NVM Class-1 device SFDP access behavior for reading SFDP and MSPT data (see Figure 11) SFDP Parameter Table and NVM Media Specific Parameter Table are available in Device's Cache Buffer before Device is ready to process Host commands during POR process, - After POR, Host always first issue READ SFDP (5Ah) with start address '00h' for device discovery - Device returns the SFDP Header with the appropriate parameter value code representing NVM Class-1 Device after received READ SFDP (5Ah) command with start address '00h' - Host issues 2nd (and more if needed) READ SFDP (5Ah) command(s) with a non-zero start address to access SFDP and MSPT table contents Device returns the SFDP/MSPT table data beginning from the start address specified in READ SFDP (5Ah) command.

6.2.3 Definition of SFDP Access Protocol Field Table (cont'd)

SFDP Command Parameter Value		
Decimal	Hex	
241	F1h	xSPI NAND class-2 device – parameter data is not available in device cache buffer. xSPI Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT. Follow Long latency NVM Class-2 device SFDP access behavior for reading SFDP and MSPT data (see Figure 12) Parameter Tables are not available in the device's Cache Buffer before Device is ready to process Host commands during POR process, - After POR, Host always first issue READ SFDP (5Ah) with start address '00h' for device discovery - Device returns SFDP Header with the appropriate parameter value code representing NVM Class-2 Device after received READ SFDP (5Ah) command with '00h' start address - Host issue FETCH SFDP (5Bh) command to Device - Host: wait 120µs; Device: fetches SFDP and MSPT tables from memory cell array to Device's Cache Buffer - Host issues 2nd (and more if needed) READ SFDP (5Ah) command(s) with a non-zero start address to access SFDP and MSPT table contents - Device returns the SFDP/MSPT Table data beginning from the start address specified in READ SFDP (5Ah) command
242	F2h	Reserved for xSPI NAND class-3 device, Combo device includes both NOR Flash and Class-1 Long Latency NVM. -for octal interface to low Latency combo with SFDP table in the cache and can use a 5Ah command
243	F3h	Reserved for xSPI NAND class-3 device – combo device with both NOR Flash device and Class-2 Long Latency NVM device -for octal interface to low Latency combo with SFDP table is not in the cache and requires a 5Bh command before the 5Ah command
244	F4h	SPI NAND class-1 device – parameter data is available in device cache buffer Legacy option: Behavior consistent with JESD216B revision. (1S-1S-1S), (2S-2S-2S) or (4S-4S-4S) operation, 3-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT Follow Long latency NVM Class-1 device SFDP access behavior for reading SFDP and MSPT data (see Figure 11)

6.2.3 Definition of SFDP Access Protocol Field Table (cont'd)

SFDP Command Parameter Value		
Decimal	Hex	
245	F5h	SPI NAND class-2 device – parameter data is not available in device cache buffer Legacy option: Behavior consistent with JESD216B revision. (1S-1S-1S), (2S-2S-2S) or (4S-4S-4S) operation, 3-byte addressing for SFDP command, 8 wait states. NAND Flash devices use JESD230C Parameter Page as MSPT Follow Long latency NVM Class-2 device SFDP access behavior for reading SFDP and MSPT data
246	F6h	Reserved for SPI NAND class-3 device, Combo device includes both NOR Flash and Class-1 Long Latency NVM.
247	F7h	Reserved for SPI NAND class-3 device, Combo device includes both NOR Flash and SPI Class-2 Long Latency NVM.
248:249	F8h:F9h	Reserved for future use
250	FAh	xSPI NOR Profile 2 (8D, 8D, 8D) operation, 5-byte addressing, SFDP command (WREN1 and WREN2), Configurable wait states.
251	FBh	Reserved for future use
252	FCh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 3-byte addressing + 1/2 Cycle for Octal DTR Alignment for SFDP command, 8 wait states.
253	FDh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 20 wait states.
254	FEh	xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 wait states.
255	FFh	Legacy option: Behavior consistent with JESD216B revision. (1S-1S-1S), (2S-2S-2S) or (4S-4S-4S) operation, 3-byte addressing for SFDP command, 8 wait states.

6.2.3 Definition of SFDP Access Protocol Field (cont'd)

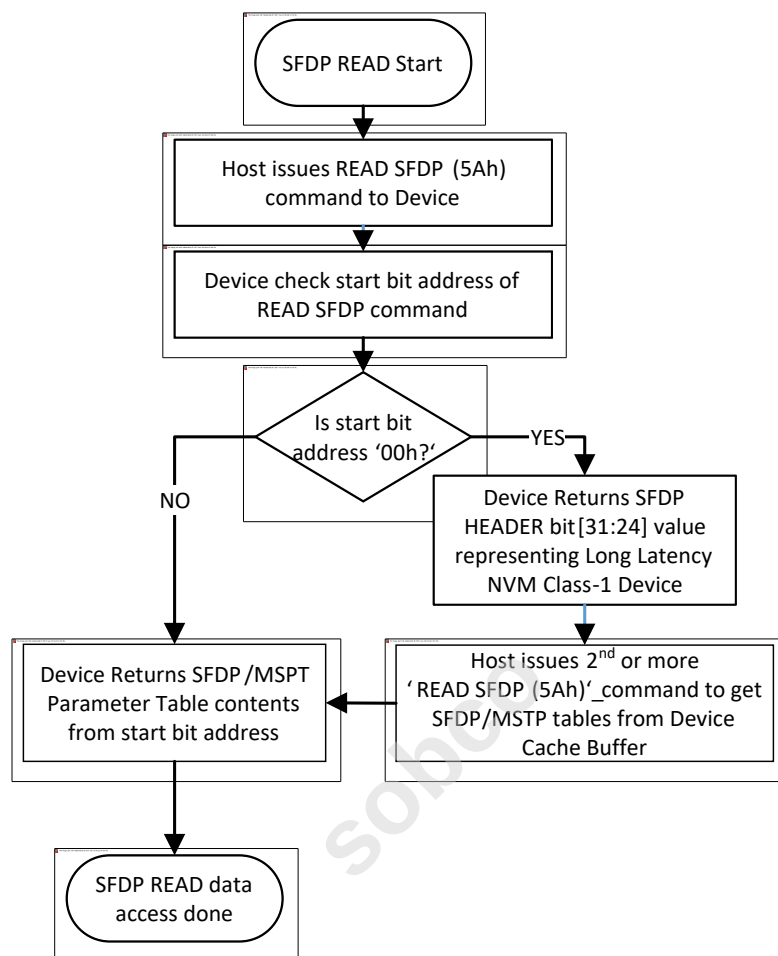


Figure 11 — xSPI NAND Class-1 Device Read SFDP Flow

6.2.3 Definition of SFDP Access Protocol Field (cont'd)

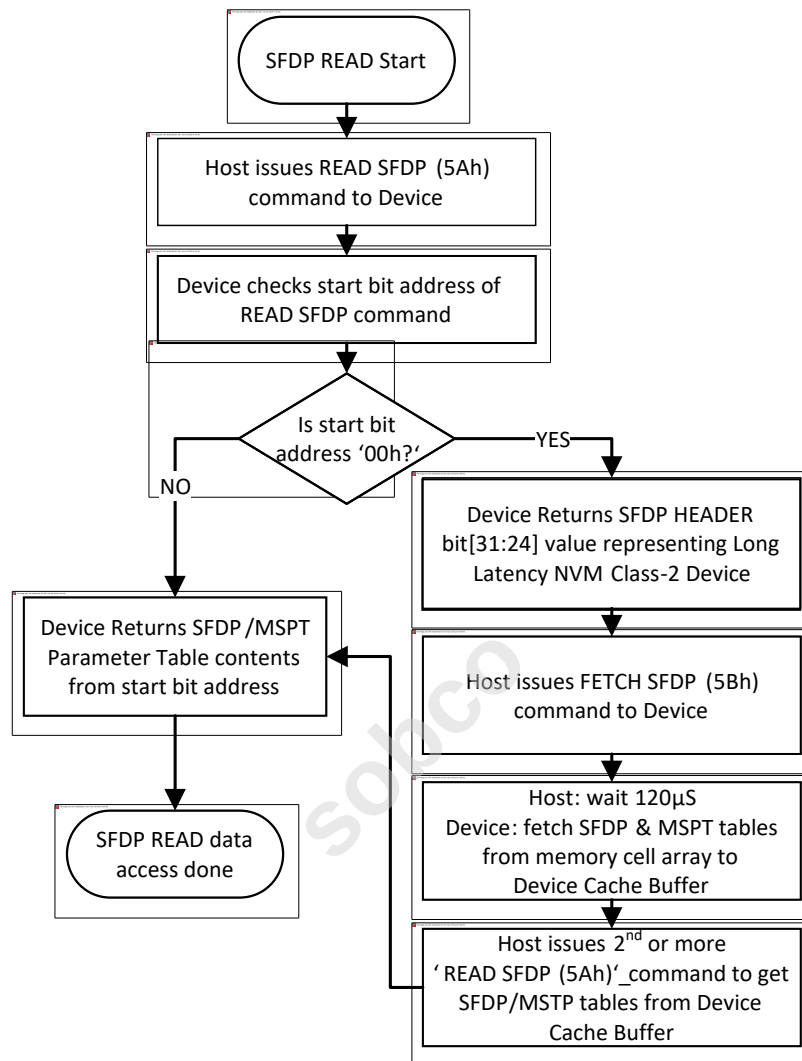


Figure 12 — xSPI NAND Class-2 Device Read SFDP Flow

6.3 Parameter Headers

Each Parameter Header identifies the size, location, revision, ownership, and function of their associated parameter tables. Parameter table ownership will be either JEDEC (via this standard) or an individual vendor (via vendor specific documentation).

Multiple parameter headers can be specified with each parameter header being 2 DWORDs (64-bits). The first parameter header is mandatory, is defined by this standard, and starts at byte offset 08h. If a vendor chooses to include multiple revisions of the Basic Parameter Table, they may do so provided the table headers are in order starting with the oldest version. The total number of parameter headers is specified in the NPH field of the SFDP header, see 6.2.2. All subsequent parameter headers need to be contiguous and may be specified by JEDEC or by vendors using the same structure (shown in Figure 10). Minor revisions may overlap earlier revisions by starting at the same address as an earlier revision but have additional length for parameters added in the later revision. This allows the use of legacy parameters without the need to repeat them in each new minor revision.

6.3.1 Parameter Header: 1st DWORD

Bits	Description
31:24	Parameter Table Length This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD.
23:16	Parameter Table Major Revision Number¹ This 8-bit field indicates the major revision number of the associated parameter table. NOTE Major Revision starts at 01h. The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard. The Major Revision of a vendor-specified table is controlled by that vendor.
15:8	Parameter Table Minor Revision Number¹ This 8-bit field indicates the minor revision number of the associated parameter table. NOTE Minor Revision starts at 00h. The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard. The Minor Revision of a vendor-specified table is controlled by that vendor.
7:0	Parameter ID LSB: Refer to Definition of Parameter ID Field in 6.3.3.
NOTE See "Major vs. Minor Revisions" in 6.2	

6.3.2 Parameter Header: 2nd DWORD

Bits	Description
31:24	Parameter ID MSB Refer to Definition of Parameter ID Field in 6.3.3.
23:0	Parameter Table Pointer (PTP) This address specifies the start of this header's Parameter Table in the SFDP structure. This is a byte address and must be DWORD-aligned.

6.3.3 Definition of Parameter ID Field

The Parameter ID indicates the parameter table ownership and type.

Parameter ID MSB	Parameter ID LSB	Type	Owner
01h – 7Fh	odd parity	Vendor specific	Vendor
01h – 7Fh	even parity	Function specific	Vendor
80h – FFh	even parity	Function specific	JEDEC JC-42.4
FFh	00h	Basic Parameter Table	JEDEC JC-42.4

Function Specific tables may be defined by the JC-42.4 Committee or a manufacturer (vendor). The purpose of the Function Specific tables is to allow development of features and associated parameter tables common to multiple manufacturers, prior to the parameter tables being incorporated into the next revision of JESD216. Allocation of IDs for Function Specific tables is requested through the JEDEC office, see Annex A.

Vendor Specific table structure is defined by the identified device vendor. The parameter table ID field identifies the vendor that owns the table definition.

The original JESD216 standard used only a one byte ID field to identify the parameter table owner. JESD216 revision A expanded the ID field to two bytes, MSB and LSB, because a single byte is insufficient to uniquely identify all manufacturers (vendors). The original single byte parameter ID is now referred to as the parameter ID LSB.

The Parameter ID LSB value of 00h is reserved for the Basic Parameter Table defined by this standard. For backwards compatibility the MSB is FFh when the LSB is 00h and LSB 00h shall not be used when the MSB is any value other than FFh. This is because some legacy systems using the original JESD216 standard may ignore the MSB and assume any parameter ID with LSB of 00h is the Basic Parameter Table.

Parameter IDs with:

- An MSB of 01h through 7Fh indicates a Vendor Owned table and provides the bank number of a JEDEC JEP106 assigned Manufacturer ID.
 - 00h is reserved because JEP106 bank numbering begins at 01h
 - The JEP106 Manufacturer's Identification Code LSB is an eight (8) bit field, consisting of seven (7) data bits plus one (1) odd parity bit in the most significant bit position. A Parameter ID LSB with odd parity signifies a Manufacturer's Identification Code and a Parameter ID LSB with even parity signifies a Function Specific table.

6.3.3 Definition of Parameter ID Field (cont'd)

- An MSB of 80h through FFh indicates a Function Specific or Basic Parameter Table defined by the JEDEC 42.4 committee. The LSB is used to identify the Function Specific table type.
 - Any parameter ID with LSB 00h identifies the SPI protocol Basic Parameter Table.
 - LSB values with even parity are Function Specific tables that are defined by the JC-42.4 committee.
 - LSB values with odd parity are illegal to prevent any confusion with JEP106 manufacturer ID values.

6.3.3.1 Function Specific Parameter Table ID Assignments

Description	ID (Hex)
Basic SPI protocol	FF00
Sector map	FF81
Replay Protected Monotonic Counters (RPMC)	FF03
4-byte Address Instruction Table	FF84
eXtended Serial Peripheral Interface (xSPI) Profile 1.0	FF05
eXtended Serial Peripheral Interface (xSPI) Profile 2.0	FF06
Status, Control and Configuration Register Map	FF87
Status, Control and Configuration Register Map Offsets for Multi-Chip SPI Memory Devices	FF88
Status, Control and Configuration Register Map for xSPI Profile 2.0	FF09
Command Sequences to change to Octal DDR (8D-8D-8D) mode	FF0A
Long Latency NVM Media Specific Parameter Table (MSPT)	FF8B
x4 Quad IO with DS	FF0C
Command Sequences to change to Quad DDR (4S-4D-4D) mode	FF8D
Secure Packet Read / Secure Packet Write	FF8E
Reserved for next Function Specific Table assignment	FF0F

6.3.4 Example SFDP Headers

Note the definition and discussion of Parameter Headers in paragraph 6.3.

Figure 13 shows an example of a basic SFDP Header (major revision 1, minor revision 7): one Parameter Header, Parameter Table length of 16 DWORDs, 1st Parameter Header Revision 1.7, JEDEC ID of FF00h, and the Parameter Table Pointer pointing to location 000010h. This header is backwards compatible with previous generations of this standard, therefore devices are not required to contain headers with prior revision numbers.

Figure 14 shows the same example as in Figure 13 but with Word based addressing (instead of byte) as needed for xSPI Profile 2.0.

In Figure 15, the first parameter header points to a version 1.0 format Basic Parameter Table of 9 DWORDs starting at location 100h and the second parameter headers both points to a separate version 1.6 format Basic Parameter Table of 16 DWORDs starting at location 200h.

6.3.4 Example SFDP Headers (cont'd)

Figure 16 adds one of the Optional Function Specific headers introduced in JESD216B. This third header indicates that this device supports 4-byte address instructions functionality.

In Figure 15 and Figure 16, devices that do not have the functionality of these features may not contain these additional parameters.

Example calculation using the Parameter Table Pointer (PTP):

The PTP is a byte address. The fields within this document are defined in terms of DWORDS.

To calculate the byte address of a particular field, given a PTP of 100h:

The SFDP byte address of the 3rd DWORD = $100h + ((3-1) * 4) = 100h + 2 * 4 = 100h + 8 = 108h$

For xSPI Profile 2.0, the PTP is a word address. The fields within this document are defined in terms of DWORDS.

To calculate the word address of a particular field, given a PTP of 100h:

The SFDP word address of the 3rd DWORD = $100h + ((3-1) * 2) = 100h + 1 * 4 = 100h + 4 = 104h$

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	00h	01h	06h	< [7h:4h]
1st Parameter Header	10h	01h	06h	00h	< [Bh:8h]
	FFh	00h	00h	10h	< [Fh:Ch]

Figure 13 — Example SFDP Header with Single Basic Parameter Table

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Word Location
SFDP Header	50h	44h	46h	53h	< [1h:0h]
	FFh	00h	01h	06h	< [3h:2h]
1st Parameter Header	10h	01h	06h	00h	< [5h:4h]
	FFh	00h	00h	10h	< [7h:6h]

Figure 14 — Example SFDP Header with Single Basic Parameter Table Word Based (xSPI Profile 2.0)

6.3.4 Example SFDP Headers (cont'd)

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	01h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]

Figure 15 — Example SFDP Header with Two Basic Parameter Tables

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	02h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]
3rd Parameter Header	02h	01h	00h	84h	< [1Bh:18h]
	FFh	00h	02h	80h	< [1Fh:1Ch]

Figure 16 — Example SFDP Header with Two Basic Parameter Tables and One Optional (4-Byte Address) Function Specific Tables

6.3.4 Example SFDP Headers (cont'd)

	[31:24]	[23:16]	[15:8]	[7:0]	Hex Byte Location
SFDP Header	50h	44h	46h	53h	< [3h:0h]
	FFh	02h	01h	06h	< [7h:4h]
1st Parameter Header	09h	01h	00h	00h	< [Bh:8h]
	FFh	00h	01h	00h	< [Fh:Ch]
2nd Parameter Header	10h	01h	06h	00h	< [13h:10h]
	FFh	00h	02h	00h	< [17h:14h]
3rd Parameter Header	02h	01h	01h	84h	< [1Bh:18h]
	FFh	00h	02h	80h	< [1Fh:1Ch]
4th Parameter Header	07	01h	00h	06h	< [23h:20h]
	FFh	00h	03h	00h	< [27h:24h]

Figure 17 — Example SFDP Header with Two Basic Parameter Tables and Two Optional (4-Byte Address and Status, Control and Configuration Register Map) Function Specific Tables

6.4 JEDEC Basic Flash Parameter Header and Table

Parameter tables contain coded information describing the features and capabilities of the serial flash. The first parameter table as defined by JEDEC is mandatory and its starting address is specified by the PTP field of the 1st Parameter Header. This table identifies some of the basic features of SPI protocol flash memory devices.

6.4.1 JEDEC Basic Flash Parameter Header: 1st DWORD

Bits	Description
31:24	Parameter Table Length This field specifies how many DWORDs are in the Parameter table. NOTE This field is 1's based. Therefore, 1 indicates 1 DWORD. For the JESD216F revision, this parameter table length is 23 (3 new DWORDs added to JESD216E)
23:16	Parameter Table Major Revision Number This 8-bit field indicates the major revision number of the parameter table. The value in this field is 01h for this table defined by JESD216F revision (unchanged from JESD216D revision). NOTE The Major Revision of JEDEC defined parameter tables can only be modified by updates to this standard.

6.4.1 JEDEC Basic Flash Parameter Header Table: 1st DWORD (cont'd)

15:8	Parameter Table Minor Revision Number This 8-bit field indicates the minor revision number of the JEDEC Basic Flash Parameter table. The value in this field is 08h for this table defined by JESD216F revision (incremented due to 3 new DWORDs added). NOTE The Minor Revision of the JEDEC owned parameter tables can only be modified by updates to this standard.
7:0	Parameter ID LSB The JEDEC Basic Flash Parameter Table is assigned the ID LSB of 00h.

6.4.2 JEDEC Basic Flash Parameter Header: 2nd DWORD

Bits	Description
31:24	Parameter ID MSB The JEDEC Basic Flash Parameter Table is assigned the ID MSB of FFh.
23:0	Parameter Table Pointer (PTP) This address specifies the start of this header's Parameter Table in the SFDP structure. The address is in terms of bytes and must be DWORD-aligned.

6.4.3 JEDEC Basic Flash Parameter Table Overview

DWORD	Description
1	Uniform 4 KB Sectors, Write Buffer Size, Volatile Status Register, Fast Read Support (1S-1S-2S) (1S-2S-2S) (1S-4S-4S) (1S-1S-4S), Number of Address Bytes, DTR Support
2	Memory Density
3	Fast Read (1S-4S-4S) (1S-1S-4S): Wait States, Mode Bit Clocks, Instruction
4	Fast Read (1S-1S-2S) (1S-2S-2S): Wait States, Mode Bit Clocks, Instruction
5	Fast Read (2S-2S-2S) (4S-4S-4S) Support
6	Fast Read (2S-2S-2S): Wait States, Mode Bit Clocks, Instruction
7	Fast Read (4S-4S-4S): Wait States, Mode Bit Clocks, Instruction
8	Erase Type 1 and 2 Size and Instruction
9	Erase Type 3 and 4 Size and Instruction
10	Erase Type (1:4) Typical Erase Times and Multiplier Used To Derive Max Erase Times
11	Chip Erase Typical Time, Byte Program and Page Program Typical Times, Page Size
12	Erase/Program Suspend/Resume Support, Intervals, Latency, Keep Out Area Size
13	Program/Erase Suspend/Resume Instructions
14	Deep Powerdown and Status Register Polling Device Busy
15	Hold and WP Disable Function, Quad Enable Requirements, 4S-4S-4S Mode Enable/Disable Sequences, 0-4-4 Entry/Exit Methods and Support
16	32-bit Address Entry/Exit Methods and Support, Soft Reset and Rescue Sequences, Volatile and Nonvolatile Status Register Support
17	Fast Read (1S-8S-8S) (1S-1S-8S): Wait States, Mode Bit Clocks, Instruction
18	Octal commands, Byte order, Data strobe, JEDEC SPI Protocol Reset
19	Octal Enable Requirements, 8D-8D-8D Mode Enable/Disable Sequences, 0-8-8 Entry/Exit Methods and Support
20	Maximum operating speeds
21	Fast Read (1S-1D-1D), (1S-2D-2D), (1S-4D-4D), and (4S-4D-4D) Support
22	Fast Read (1S-1D-1D) and (1S-2D-2D) Wait States, Mode Bit Clocks, and Instruction
23	Fast Read (1S-4D-4D) and (4S-4D-4D) Wait States, Mode Bit Clocks, and Instruction

6.4.4 JEDEC Basic Flash Parameter Table: 1st DWORD

Bits	Description
31:23	Unused Contains FFh and can never be changed.
22	Supports (1S-1S-4S) Fast Read Device supports single input instruction and address and quad output data Fast Read. 0: (1S-1S-4S) Fast Read NOT supported. 1: (1S-1S-4S) Fast Read supported.
21	Supports (1S-4S-4S) Fast Read Device supports single input instruction, quad input address, and quad output data Fast Read. 0: (1S-4S-4S) Fast Read NOT supported. 1: (1S-4S-4S) Fast Read supported.
20	Supports (1S-2S-2S) Fast Read Device supports single input instruction, dual input address, and dual output data Fast Read. 0: (1S-2S-2S) Fast Read NOT supported. 1: (1S-2S-2S) Fast Read supported.
19	Supports Double Transfer Rate (DTR) Clocking Indicates the device supports some type of double transfer rate clocking. 0: DTR NOT supported 1: DTR Clocking supported
18:17	Address Bytes Number of bytes used in addressing flash array read, write and erase: 00b: 3-Byte only addressing 01b: 3- or 4-Byte addressing (e.g., defaults to 3-Byte mode; enters 4-Byte mode on command) 10b: 4-Byte only addressing 11b: Reserved NOTE This field refers to the number of address bits/bytes that are clocked in for any command requiring an address except for SFDP Header or Table accesses. All SFDP accesses use 3-byte addressing. A device using 4-byte only addressing may still support 03h read using 3-byte addressing. Examples: Read, Fast Read, Write, 4 kilobyte Erase.
16	Supports (1S-1S-2S) Fast Read Device supports single input instruction and address and dual output data Fast Read with 8 wait states. 0: (1S-1S-2S) Fast Read NOT supported. 1: (1S-1S-2S) Fast Read supported.
15:8	4 Kilobyte Erase Instruction NOTE If 4 kilobyte erase is not supported, then enter FFh. This instruction must also be included in one of the Erase Types in 6.4.8 or 0

6.4.4 JEDEC Basic Flash Parameter Table: 1st DWORD (cont'd)

7:5	Unused Contains 111b and can never be changed.
4	Write Enable Instruction Select for Writing to Volatile Status Register This bit only applies if bit 3 is 1. 0: flash device requires instruction 50h as the write enable prior to performing a volatile write to the status register 1: flash device requires instruction 06h as the write enable prior to performing a volatile write to the status register. NOTE If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b. This bit definition is maintained for legacy compatibility only. New system implementations should refer to 0 for a full definition of volatile and non-volatile behavior.
3	Volatile Status Register Block Protect bits 0: Block Protect bits in device's status register are solely non-volatile or may be programmed either as volatile using the 50h instruction for write enable or non-volatile using the 06h instruction for write enable. 1: Block Protect bits in device's status register are solely volatile. NOTE If target flash register is nonvolatile, then bits 3 and 4 must be set to 00b. This bit definition is maintained for legacy compatibility only. New devices should refer to 0 for a full definition of volatile and non-volatile behavior.
2	Write Granularity 0: 1 Byte – Use this setting for single byte programmable devices or buffer programmable devices when the buffer is less than 64 bytes (32 Words). 1: Use this setting for buffer programmable devices when the buffer size is 64 bytes (32 Words) or larger. This bit definition is maintained for legacy compatibility only. New system implementations should refer to 6.4.14 for the buffer (page) size. The legacy minimum write granularity is a single byte within any size programming buffer.
1:0	Block/Sector Erase Sizes Identifies if the device supports uniform 4k erase blocks. This erase size information must also be included one of the Erase Types in 6.4.11 or 6.4.12. 00b: Reserved 01b: 4 kilobyte Erase is supported throughout the device 10b: Reserved 11b: Use this setting only if uniform 4 kilobyte erase is unavailable. NOTE This is a legacy field. Refer to clauses 6.4.8 and 0 for information on what erase sizes are supported.

6.4.5 JEDEC Basic Flash Parameter Table: 2nd DWORD

Bits	Description
31:0	Flash Memory Density For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the size in bits. Example: 00FFFFFFh = 16 megabits For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines 'N' where the density is computed as 2^N bits (N must be ≥ 32). Example: 80000021h = 2^{33} = 8 gigabits

6.4.6 JEDEC Basic Flash Parameter Table: 3rd DWORD

Bits	Description
31:24	(1S-1S-4S) Fast Read Instruction Instruction for single input instruction and address and quad output data Fast Read.
23:21	(1S-1S-4S) Fast Read Number of Mode Clocks This field will be 000b if Mode Bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. Example: If 4 mode bits are needed with a single input address phase command, this field would be 100b.
20:16	(1S-1S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	(1S-4S-4S) Fast Read Instruction Instruction for single input instruction, quad input address, and quad output data Fast Read.
7:5	Quad Input Address Quad Output (1S-4S-4S) Fast Read Number of Mode Clocks This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. Example: If 8 mode bits are needed with a quad input address phase command, this field would be 010b.
4:0	(1S-4S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)

6.4.7 JEDEC Basic Flash Parameter Table: 4th DWORD

Bits	Description
31:24	(1S-2S-2S) Fast Read Instruction Instruction for single input instruction, dual input address, and dual output data Fast Read.
23:21	(1S-2S-2S) Fast Read Number of Mode Clocks This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. Example: If 8 mode bits are needed with a dual input address phase command, this field would be 100b.
20:16	(1S-2S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:8	(1S-1S-2S) Fast Read Instruction Instruction for single input instruction and address and dual output data Fast Read. NOTE The industry standard is 3Bh
7:5	(1S-1S-2S) Fast Read Number of Mode Clocks This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. Example: If 4 mode bits are needed with a single input address phase command, this field would be 100b.
4:0	(1S-1S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output This field should be programmed with 01000b for 8 clocks of dummy cycle. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.) NOTE For legacy reasons, if dummy clocks for this instruction is not 01000b, then bit 16 in 6.4.1 (Supports (1S-1S-2S) Fast Read with 8 wait states) must NOT be set to '1'.

6.4.8 JEDEC Basic Flash Parameter Table: 5th DWORD

Bits	Description
31:5	Reserved. These bits default to all 1's
4	Supports (4S-4S-4S) Fast Read Device supports Quad input instruction and address and quad output data Fast Read. 0: (4S-4S-4S) Fast Read NOT supported. 1: (4S-4S-4S) Fast Read supported.
3:1	Reserved. These bits default to all 1's
0	Supports (2S-2S-2S) Fast Read Device supports dual input instruction and address and dual output data Fast Read. 0: (2S-2S-2S) Fast Read NOT supported. 1: (2S-2S-2S) Fast Read supported.

6.4.9 JEDEC Basic Flash Parameter Table: 6th DWORD

Bits	Description
31:24	(2S-2S-2S) Fast Read Instruction Instruction for dual input instruction and address and dual output data Fast Read.
23:21	(2S-2S-2S) Fast Read Number of Mode Clocks This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. Example: If 4 mode bits are needed with a (2S-2S-2S) Fast Read command, this field would be 010b.
20:16	(2S-2S-2S) Fast Read Number of Wait states (dummy clocks) needed before valid output This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:0	Reserved. These bits default to all 1's

6.4.10 JEDEC Basic Flash Parameter Table: 7th DWORD

Bits	Description
31:24	(4S-4S-4S) Fast Read Instruction Instruction for quad input instruction/address, quad output data Fast Read.
23:21	(4S-4S-4S) Fast Read Number of Mode Clocks This field will be 000b if Mode bits are not supported, NOTE This field should be counted in clocks not number of bits received by the serial flash. The initiator drives the bus during "mode bits" cycles; the initiator tri-states the bus during "dummy" cycles. Example: If 8 mode bits are needed with a (4S-4S-4S) Fast Read phase command, this field would be 010b.
20:16	(4S-4S-4S) Fast Read Number of Wait states (dummy clocks) needed before valid output This field will be 00000b if wait states/dummy clocks are not supported. (The number of dummy clocks should be > 0 to avoid contention on bi-directional pins.)
15:0	Reserved. These bits default to all 1's

6.4.11 JEDEC Basic Flash Parameter Table: 8th DWORD

NOTE If the device uses a 4k subsector size, that size and instruction must be included somewhere in the 8th or 9th DWORD. This allows the user to discover the typical and maximum erase times for the 4k subsector by referencing the 10th DWORD.

Bits	Description
31:24	Erase Type 2 Instruction Instruction used to erase the number of bytes specified by Erase Type 2 Size (bits 23-16).
23:16	Erase Type 2 Size: This field will be 00h if this erase type does not exist. NOTE This field specifies 'N' and is used to calculate erase type size = 2 ^N bytes Example: If the erase type size is 32 kilobytes, this field would 0Fh.
15:8	Erase Type 1 Instruction Instruction used to erase the number of bytes specified by Erase Type 1 Size (bits 7-0).
7:0	Erase Type 1 Size NOTE This field specifies 'N' and is used to calculate erase type size = 2 ^N bytes Example: If the erase type size is 4 kilobytes, this field would 0Ch.

6.4.12 JEDEC Basic Flash Parameter Table: 9th DWORD

Bits	Description
31:24	Erase Type 4 Instruction Instruction used to erase the number of bytes specified by Erase Type 4 Size (bits 23-16).
23:16	Erase Type 4 Size This field will be 00h if this erase type does not exist. NOTE This field specifies 'N' and is used to calculate erase type size = 2^N bytes Example: If the erase type size is 256 kilobytes, this field would 12h.
15:8	Erase Type 3 Instruction Instruction used to erase the number of bytes specified by Erase Type 3 Size (bits 7-0).
7:0	Erase Type 3 Size This field will be 00h if this erase type does not exist. NOTE This field specifies 'N' and is used to calculate erase type size = 2^N bytes Example: If the erase type size is 64 kilobytes, this field would 10h.

6.4.13 JEDEC Basic Flash Parameter Table: 10th DWORD

Bits	Description
31:25	Erase Type 4 Erase, Typical time Time the device <i>typically</i> takes to erase an Erase Type 4 size, see 0. User must poll device busy to determine if the operation has completed. This field has no meaning if the Erase Type 4 size is 00h. 31:30 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 29:25 count Formula: typical time = (count + 1)*units Example: If count=2 and units=10b, then typical time is (2+1)*128ms = 384 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
24:18	Erase Type 3 Erase, Typical time Time the device <i>typically</i> takes to erase an Erase Type 3 size, see 0. User must poll device busy to determine if the operation has completed. This field has no meaning if the Erase Type 3 size is 00h. 24:23 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 22:18 count Formula: typical time = (count + 1)*units Example: If count=1 and units=10b, then typical time is (1+1)*128ms = 256 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s

6.4.13 JEDEC Basic Flash Parameter Table: 10th DWORD (cont'd)

17:11	Erase Type 2 Erase, Typical time Time the device <i>typically</i> takes to erase an Erase Type 2 size, see 6.4.8. User must poll device busy to determine if the operation has completed. This field has no meaning if the corresponding Erase Type size is 00h. 17:16 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 15:11 count Formula: typical time = (count + 1)*units Example: If count=0 and units=10b, then typical time is (0+1)*128ms = 128 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
10:4	Erase Type 1 Erase, Typical time Time the device <i>typically</i> takes to erase an Erase Type 1 size, see 6.4.8. User must poll device busy to determine if the operation has completed. This field has no meaning if the corresponding Erase Type size is 00h. 10:9 units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) 8:4 count Formula: typical time = (count + 1)*units Example: If count=1 and units=10b, then typical time is 1*128ms = 128 ms The range is 1ms to 32 seconds in four groups: 1 ms to 32 ms, 16 ms to 512 ms, 128 ms to 4096 ms, 1 s to 32 s
3:0	Multiplier from typical erase time to maximum erase time 3:0 count Formula: Erase Type n (or Chip) erase maximum time = 2 * (count + 1) * Erase Type n (or Chip) erase typical time Example: If count = 9, then Erase Type n (or Chip) erase maximum time is 20 * Sector Type n (or Chip) erase typical time NOTE 1 'n' = 1, 2, 3, or 4 NOTE 2 This multiplier applies to all erase types and the chip erase. The maximum time is intended to be used as a watchdog timeout for an error or failure condition. Since a common scale factor is used across all erase sizes, any particular maximum time may only approximate the datasheet maximum time.

6.4.14 JEDEC Basic Flash Parameter Table: 11th DWORD

Bits	Description
31	Reserved
30:24	Chip Erase, Typical time Typical time to erase one chip (die). User must poll device busy to determine if the operation has completed. For a device consisting of multiple dies, that are individually accessed, the time is for each die to which a chip erase command is applied. 30:29 units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) 28:24 count Formula: typical time = (count + 1)*units Example: If count=5 and units=10b, then typical time is: 5*4 s = 20 s The range of this field is 16ms to 2048 seconds in four groups: 16 ms to 512 ms, 256 ms to 8192 ms, 4 s to 128 s, 64 s to 2048 s
23:19	Byte Program Typical time, additional byte Time the device <i>typically</i> takes to write each additional byte after the first. User must poll device busy to determine if the operation has completed. 23 units (0: 1 µs, 1: 8 µs) 22:19 count Formula: additional byte time = (count + 1)*units/byte Example: If units = 1 and count =4, then each additional byte typically adds (4+1)*8 µs = 40 µs to the programming time. For 16 bytes, the additional time would be 16 * 40 µs = 640 µs The range is 1 µs to 128 µs in two groups: 1 µs to 16 µs and 8 µs to 128 µs. NOTE The programming time for small numbers of bytes does not scale linearly up to a full page programming time. When the number of bytes being programmed exceeds ½ of a page size, users should base estimates on the Page Program typical time in this DWORD.
18:14	Byte Program Typical time, first byte Time the device <i>typically</i> takes to write the first byte in a sequence. User must poll device busy to determine if the operation has completed. 18 units (0: 1 µs, 1: 8 µs) 17:14 count Formula: first byte typical time = (count + 1)*units Example: If units = 0 and count = 7, then typical time is (7+1)*1 µs = 8 µs The range is 1 µs to 128 µs in two groups: 1 µs to 16 µs and 8 µs to 128 µs

6.4.14 JEDEC Basic Flash Parameter Table: 11th DWORD (cont'd)

13:8	Page Program Typical time Time the device <i>typically</i> takes to write a full page. User must poll device busy to determine if the operation has completed. The user may scale this by $\frac{1}{2}$ or $\frac{1}{4}$ to determine approximate times for $\frac{1}{2}$ and $\frac{1}{4}$ page program operations 13 units (0: 8 μs, 1: 64 μs) 12:8 count Formula: typical page program time = (count + 1)*units The range is 8 μs to 2048 μs in two groups: 8 μs to 256 μs and 64 μs to 2048 μs
7:4	Page Size This field specifies 'N' and is used to calculate page size = 2^N bytes.
3:0	Multiplier from typical time to max time for Page or byte program 3:0 count Formula: maximum time = 2 * (count + 1)*typical time NOTE This multiplier applies to all page or byte typical program times. The maximum time is intended to be used as a watchdog timeout for an error or failure condition. Since a common scale factor is used across all program sizes, any particular maximum time may only approximate the datasheet maximum time.