

# **JEDEC STANDARD**

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## **Test Methods to Characterize Voiding in Pre-SMT Ball Grid Array Packages**

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### **JESD217A.01**

(Revision of JESD217.01, October 2016)

**NOVEMBER 2022**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES

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## **Forward**

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This document has been prepared by the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices.

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## **Introduction**

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As ball grid array device pitch continues to decrease, the need to characterize solder voiding has become more significant. Solder void manifestation (type and/or sizes) has been used to determine process capability as a means of quality assurance during process transfer, and as indicators of process stability from in-line manufacturing monitors. This document describes how to characterize voids in solder spheres in ball grid array packages prior to surface-mount (SMT) reflow soldering.



## TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES

(From Board Ballot JCB-22-35, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

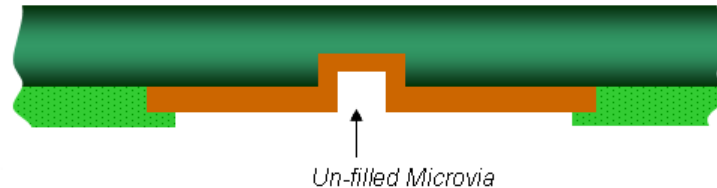
### 1 Scope

This standard provides an overview of solder void types, outlines current metrologies and test methods used for pre-SMPT solder void characterization and potential limitations, and prescribes sampling strategy for data collection, and tolerance guidelines for corrective measures.

Test methods can be applied to several types of ball grid array packages such as FCBGA, PBGA, CBGA, and CCGA with minimum 0.5 mm ball-to-ball pitch and constructed with leaded and lead-free solder alloys.

Guidelines for pre-SMT voids may not be sufficiently robust where ball grid array packages balls are assembled onto unfilled micro-via structures on package substrate land. Hence, the un-filled microvia construction (Figure 1 (a)) is considered out-of-scope for this document, while filled via (Figure 1 (b)) is within scope.

*a) BGA Package Substrate with un-filled Microvia*



*b) BGA Package Substrate with filled Microvia*

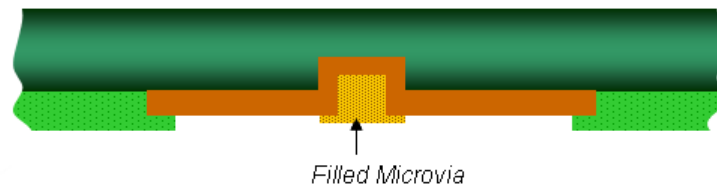


**Figure 1 — Illustration of Unfilled Microvia (a) Out-of-Scope vs. Filled Microvia (b) In-Scope of Document**

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## 2 Terms and Definitions

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**ball grid array (BGA) packages:** A package in which the external connections to the package are made via a rectangular array of ball-type connections, all on a common plane. (Ref. definition per JESD22-B112.)

**CBGA:** Ceramic ball grid array package.

**CCGA:** Ceramic column grid array package.

**field of view:** The area of the test sample under metrology examination.

**flip chip ball grid array (FCBGA) package:** A type of ball grid array (BGA) package which consists of facedown die (flip chip FC) on organic substrate of package.

NOTE FCBGA packages typically have a filled epoxy which is dispensed between the die and the substrate.

**lead solder:** A solder sphere composed primarily of tin (Sn) and lead (Pb) elements.

NOTE 67%/37% (SnPb) and 60%/40% (SnPb) are predominant formulations, and are commonly referred to as eutectic solder.

**Pb-free; lead-free:** Having a maximum lead (Pb) concentration value of 0.1% by weight in PCB surface finishes, device terminal finishes, bump or ball materials, and attachment solders.

NOTE Pb-free SAC alloys: traditional tin/silver/copper alloys that have a melting point in the range of 217°C and 220°C.

NOTE LTS (Low Temperature Solder) alloys: near eutectic-bismuth alloys that have a melting point in the range of 150°C and 170°C.

**PBGA:** Plastic ball grid array package.

**Printed Circuit Board (PCB):** Printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base (also sometimes termed Printed Wiring Board). (Ref. IPC-T-50G)

**SAC:** A type of lead-free solder made from tin, silver, and copper (Sn=S, Ag=A, Cu=C). (Ref. IPC-7095B)

**surface mount process technology (SMT):** A method of constructing electronic printed circuit boards in which components (small or large devices) are placed onto solder paste (or flux) in specified locations and exposed to reflow process window with varying sets of elevated temperature and time that allows solder coalescence and metallization.

**solder void area:** The area of the solder void region within the X-ray image of a BGA solder ball or joint.

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### 3 Normative References

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J-STD-609, *Marking, Symbols, and Labels of Leaded and Lead-Free Terminal Finished Materials Used in Electronic Assembly*

JESD16-A, *Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM)*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

JESD22-B112, *Package Warpage Measurement of Surface-Mount Integrated Circuits at Elevated Temperature*

IPC-A-610D, *Acceptability of Printed Circuit Assemblies*

IPC-7095B, *Design and Assembly Process Implementation for BGAs*

IPC-T-50G, *Terms and Definition for Interconnecting and Packaging Electronic Circuits*

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**4 Ball Attach Process Flow**

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Solder balls are attached by applying a flux/paste material on to the BGA pads, placing the solder balls on the pads, and reflowing the BGA package. The reflow process forms a metallurgical joint between the solder ball and the substrate ball pad. Alignment is a key parameter during ball placement to avoid missing solder balls or solder balls bridging.

Figure 2 gives a sequential representation of the BGA ball attach process flow.

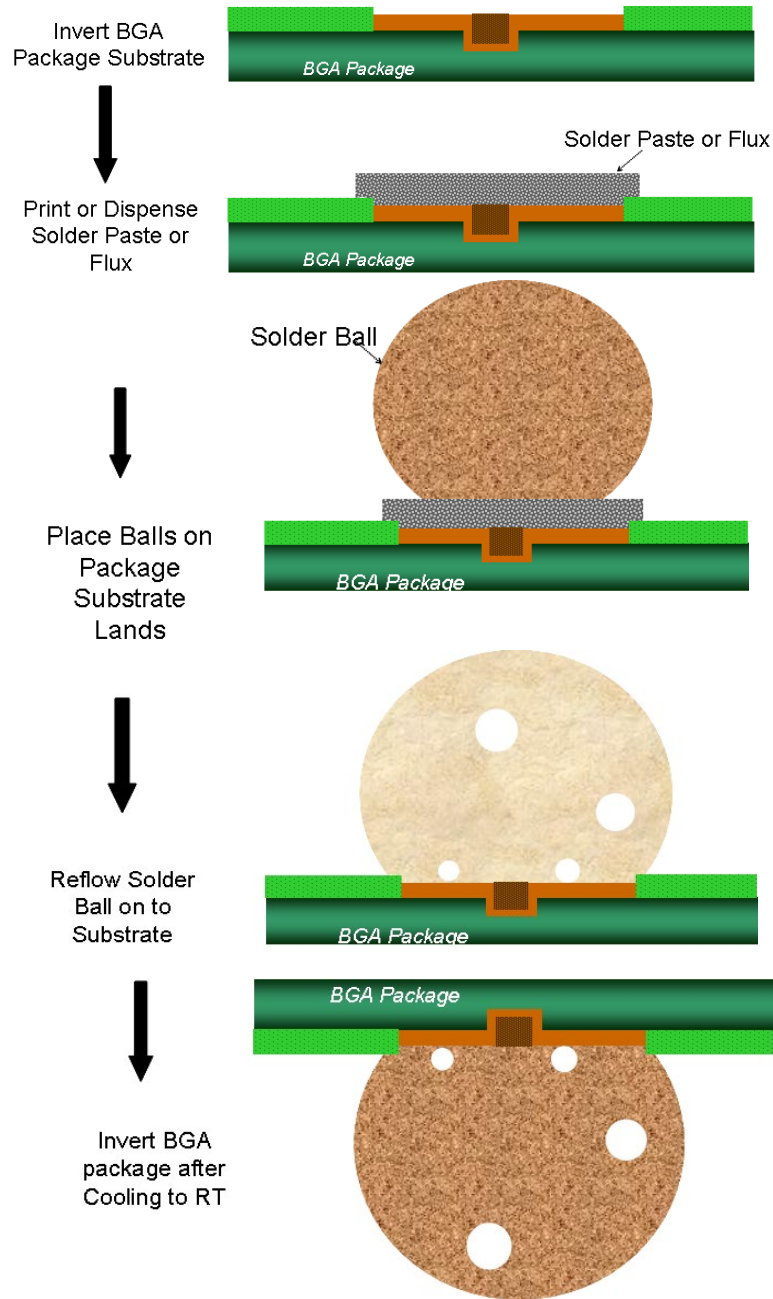


**Figure 2 — BGA Ball Attach Process Flow Diagram**

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## 5 Types of Solder Voids

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For the sake of completeness, all six types of voids observed in solder joints are described in this section, including potential voids that manifest after BGA-type packages are mounted onto a board. The individual characteristics of each of these voids are detailed here.

**Macrovoids** are the most common voids in solder joints. These are caused by volatile compounds that evolve during the soldering processes. These macrovoids generally do not affect the solder joint reliability unless they are present at interfacial regions in the solder joints where cracks typically propagate. This type of voids is within scope of this document.

**Planar Microvoids** are a series of small voids, in relatively the same plane, located at the interface between the PCB lands and the solder. These are caused by copper caves predominantly observed under immersion silver (ImAg) surface-finish coated lands. They do not affect initial product quality, but can affect long term solder joint reliability. They can be eliminated by strict control of the ImAg surface finish plating and etching materials and critical process parameters.

**Shrinkage Voids** are caused by the shrinkage during solidification, mostly for SAC and other lead free solders. They do not generally appear near the solder-to-PCB land interface and do not impair the solder joint reliability. These shrinkage voids can be minimized by increasing the cooling rate during soldering and avoiding disturbance to the joint while it is solidifying.

**Micro-via Voids** are caused by the presence of micro-vias designed in the PCB lands. Large micro-via voids, if located in solder joints in high stress areas of a package can impact solder joint reliability. Plating the micro-via shut, or filling it completely with solder paste by double printing can minimize the creation of these voids.

**IMC Microvoids** occur within the intermetallic compound (IMC) formed between copper and high Sn solders, including SAC and SnPb solders. These IMC microvoids do not form immediately after the soldering process, but after aging at high temperatures or during temperature cycling of the solder joints. The true root cause is still under investigation, but a *Kirkendall* voiding mechanism may play a part. These voids can affect solder joint reliability, particularly in instances when brittle fracture is initiated within the IMC during drop or mechanical shock to the solder joint.

**Pinhole Voids** are caused by pinholes in the copper lands of the PCB. With sufficient quantity, they can affect solder joint reliability. These voids are caused by entrapped PCB fabrication chemicals within these pinholes that volatilize during the reflow soldering process. The pinholes occur due to an excursion within the copper plating process at the PCB fabricator and can be eliminated by improved copper plating process control systems. These types of voids are considered out-of-scope

## 5 Types of Solder Voids (cont'd)

Figure 3 illustrates all six types of voids and their typical size and location in a BGA solder joint.

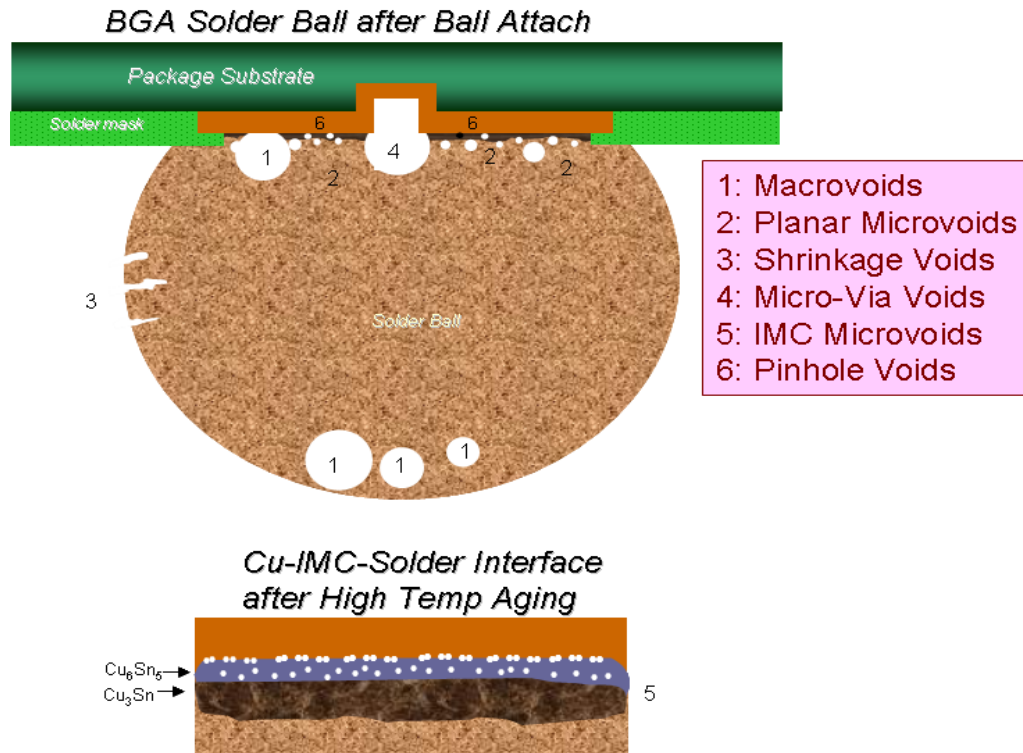


**Figure 3 — Typical Size and Location of Various Types of Voids in a BGA Solder Joint**

For this standard, focus is placed on macrovoids, because they are most likely to manifest prior to SMT process and can be identified by most metrologies. The other types of voids are noted for completeness, but out-of-scope due to metrology detection and void formation concerns.

## 6 Solder Void Metrologies

### 6.1 2-D X-ray

2-D X-ray is one of the metrologies being used to detect and measure the voids in BGA solder joints. There are a variety of 2-D X-ray tool vendors. Care must be taken to optimize the tool settings to achieve the best possible measurements. Generic guidelines for the 2-D X-ray technique are described in this section.

### 6.1.1 2-D X-Ray Tool Requirement/Limitation

The X-ray tube should be perpendicular to the test sample during image capture, as shown in Figure 4. Oblique viewing does not provide “true” void %.

The field of view may be modulated by adjusting the distance between the test sample and X-ray tube. Field of view ought to be set considering accuracy of the inspection as well as throughput requirements. Variations in the field of view that permits 3x3, 4x4 and 5x5 ball array are commonly reported.

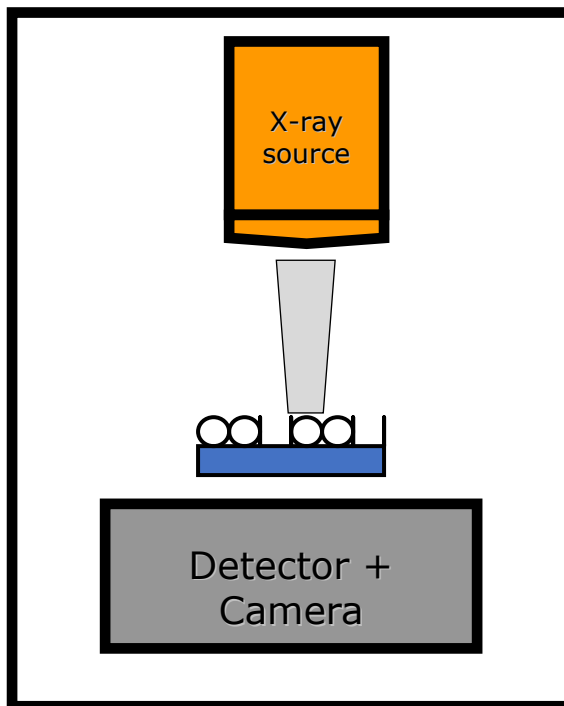


**Figure 4 — Illustration of X-ray Setup and its Orthogonal Alignment to Test Sample**

To achieve the best possible contrast between BGA voids and the surrounding area for solder void detection, adjustments to the grey scale should be considered. Ranges of settings that may be utilized as starting points are provided. The settings are given in terms of % grey scale (black is 0%, white is 100%):

- Solderball setting range from 36% to 48%.
- Background setting range from 85% to 100%.

The above settings can be achieved by adjusting the current and voltage on the X-ray tool. Figure 5 emphasizes the importance of proper contrast; voids are barely visible in the left image, while the right image was collected after achieving the best possible contrast.