

JEDEC STANDARD

Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test

JESD22-A117C

(Revision of JESD22-A117B, March 2009)

OCTOBER 2011

JEDEC Solid State Technology Association



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2011
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

**PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications online at
<http://www.jedec.org/Catalog/catalog.cfm>**

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies
through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107
or call (703) 907-7559

ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION STRESS TEST

(From JEDEC Board Ballot JCB-11-73, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Method and Packaged Devices.)

1 Scope

This stress test is intended to determine the ability of an EEPROM integrated circuit or an integrated circuit with an EEPROM module (such as a microprocessor) to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life of the EEPROM (data retention). This Standard specifies the procedural requirements for performing valid endurance and retention tests based on a qualification specification. Endurance and retention qualification specifications (for cycle counts, durations, temperatures, and sample sizes) are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

This stress test does not replace other stress test qualification requirements. The program/erase endurance and data retention test for qualification and monitoring, using the parameter levels specified in JESD47, is considered destructive. Lesser test parameter levels (e.g., of temperature, number of cycles, retention bake duration) may be used for screening as long as these parameter levels have been verified by the device manufacturer to be nondestructive; this can be performed anywhere from wafer level to finished device.

2 Terms and definitions

2.1 EEPROM

A reprogrammable read-only memory in which the cells at each address can be erased electrically and reprogrammed electrically.

NOTE The term EEPROM in this document includes all such memories, including FLASH EEPROM integrated circuits and embedded memory in integrated circuits such as Erasable Programmable Logic Devices (EPLDs) and microcontrollers. Destructive-read memories such as ferroelectric memories, in which the read operation re-writes the data in the memory cells, are beyond the scope of this document.

2.2 Data pattern

The mix of 1s and 0s in the memory and their physical or logical positions.

NOTE A device may be single-bit-per-cell (SBC), meaning that one physical memory cell stores a “0” or a “1”, or multiple-bits-per-cell (MBC), meaning that one cell stores typically two bits of data: “00”, “01”, “10”, or “11”. In some MBC memories, the two bits represent logically-adjacent bit-pairs in each byte of data. For example, a byte containing binary data 10110001 would correspond to four physical cells with data 2301 in base-four logic. In other MBC memories, the two bits may represent bits in entirely different address locations. For an SBC memory a physical checkerboard pattern consists of alternating 0s and 1s, with each 0 surrounded by 1s on either side and above and below; a logical checkerboard pattern consists of data bytes AAH or 55H in which each 0 is logically adjacent to 1s. In some qualifications only logical positions may be known.

2.3 Endurance

The ability of a reprogrammable read-only memory to withstand data rewrites and still comply with its specifications.

NOTE 1 EEPROM device specifications often require an erase step before reprogramming data; in this case a data rewrite includes both erase and programming steps, which together are called a program/erase cycle. Direct-write memories allow data to be written directly over old, without an erase; in this case the use of the generic term “program/erase cycle” will refer to a single rewrite with no erase. For SBC memories that require an erase step, one program/erase cycle consists of programming cells (typically to “0”) and then erasing (“1”). For the comparable MBC case, a cycle would consist of programming cells (to “0”, “1”, or “2”) and then erasing (“3”).

NOTE 2 Endurance stressing consists of performing multiple rewrites in succession, and the data pattern or patterns for these rewrites must be chosen. There is no one data pattern or set of patterns that is worst-case for all failure mechanisms. For example, for floating-gate memories a fully-programmed pattern is worst-case for charge transfer, but a physical checkerboard pattern is worst-case for spurious programming of adjacent cells, and a mostly-erased pattern may be worst-case for mechanisms related to erase-preconditioning algorithms. For MBC memories, programming to the highest state is worst-case for charge transfer, but intermediate-state cells may experience more programming time and also have less sensing margin. Finally, in some memories, the margin of a cell is influenced by the data states of the physically adjacent cells.

2.4 Endurance failure

A failure that arises during endurance cycling.

NOTE 1 An endurance failure occurs if the device fails to complete the program or erase operations within the datasheet-specified times or if it fails to meet any of its other datasheet requirements as a result of program/erase cycling. A program operation that results in incorrect data being stored in the device counts as an endurance failure. However, if an error-management method such as an error-correction code is built into the device or specified to be applied by the system, then failure is taken to occur only if the error is not properly managed by the specified method.

NOTE 2 Certain products are specified to operate with either internal or external bad-block management system (BBM). When the BBM system detects an endurance failure it directs the data to another (spare) block and removes the address of the failing block from an appropriate address table. An endurance failure of such product is taken to occur when a pre-set number of spare blocks of the product had been consumed within that product datasheet specified cycle count.

NOTE 3 A number of distinct failure mechanisms are responsible for endurance failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters. For example, in floating-gate memories failure may be caused by charge trapping (normally accelerated by lower temperatures) in the charge transfer dielectric or by oxide rupturing (normally accelerated by higher temperatures) in the transfer dielectric or in peripheral dielectrics.

2.5 Failure

The loss of the ability of a component to meet the electrical or physical performance specifications that (by design or testing) it was intended to meet.

NOTE 1 The term *failure* is often qualified by an adjective describing the type of failure. For example, a component is a functional failure if it fails to function and a parametric failure if it functions but does not meet a datasheet specification for a parameter such as power consumption. Endurance and retention failures are defined in 2.4 and 2.7.

NOTE 2 Failures may be firm or transient. For the purpose of this standard, a firm failure is a component that fails sometime during a reliability stress and continues to fail at the final test at the end of that same stress. A transient failure is a component that fails during a reliability stress but passes in the final test at the end of that stress.

2.6 Retention

The ability of the EEPROM cell to retain data over time.

NOTE 1 The term data retention may refer to the ability of a device to retain data in the unbiased state, but the term will sometimes be used to include the ability to retain data under bias. The term “disturb” refers unambiguously to the ability of an EEPROM cell to retain data over time under bias. For example, read disturb refers to the ability of an EEPROM cell to retain data after being read a given number of times. A detailed discussion of disturbs is beyond the scope of this document.

NOTE 2 Retention stressing consists of writing a data pattern into a device and then verifying that the pattern is intact after a specified time at a specified temperature. There is no single data pattern that is worst-case for all retention mechanisms, cell designs, or process architectures. There are generally some failure mechanisms which primarily affect programmed cells and some which primarily affect erased cells, and there are also failure mechanisms which depend on the data in adjacent cells.

2.7 Retention failure

A change of stored data by one bit or more detected when the device is read according to data sheet specifications.

NOTE 1 If an error-management method such as an error-correction-code is built into the device or specified to be applied by the system, then failure is taken to occur only if the error is not properly managed by the specified method.

NOTE 2 A number of distinct failure mechanisms are responsible for retention failures, and in general these are accelerated in different ways by temperature and other adjustable qualification parameters. For example, in floating-gate memories, failure may occur due to defects that allow charge to leak through the transfer dielectric or by the detrapping of charge in the transfer dielectric; the former can be weakly accelerated or even decelerated by high temperature, and the latter can be highly temperature-accelerated.