JEDEC STANDARD

Standard for Definition of ‘CU878 PLL Clock Driver for Registered DDR2 DIMM Applications

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STANDARD FOR DEFINITION OF ’CU878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS

(Formerly JEDEC Board Ballot JCB-04-56A, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ’CU878 PLL clock device for registered DDR2 DIMM applications.

The purpose is to provide a standard for a ’CU878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Definitions for the purpose of this document

$C_{I(\Delta)}$ – Delta input capacitance.

3 Device standard

3.1 Description

This PLL Clock Buffer is designed for a V_{DDQ} of 1.8 V, an AV_{DD} of 1.8 V and differential data input and output levels. Package options include a plastic 52-ball VFBGA and a 40-pin MLF.

The device is a zero delay buffer that distributes a differential clock input pair (CK, $\overline{CK}$) to ten differential pair of clock outputs (Y[0:9], $\overline{Y[0:9]}$) and one differential pair feedback clock outputs (FBOUT, $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CK, $\overline{CK}$), the feedback clocks (FBIN, $\overline{FBIN}$), the LVCMOS (OE, OS) and the Analog Power input (AV_{DD}). When OE is low, the outputs (except FBOUT/$\overline{FBOUT}$) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to GND or V_{DDQ}. When OS is high, OE will function as described above. When OS is low, OE has no effect on Y7/$\overline{Y7}$ (they are free running in addition to FBOUT/$\overline{FBOUT}$). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When both clock signals (CK, $\overline{CK}$) are logic low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffers, will detect the logic low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When the inputs transition from both being logic low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair (FBIN, $\overline{FBIN}$) and the input clock pair (CK, $\overline{CK}$) within the specified stabilization time t_L.

The PLL in the ’CU878 clock driver uses the input clocks (CK, $\overline{CK}$) and the feedback clocks (FBIN, $\overline{FBIN}$) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{Y[0:9]}$). The ’CU878 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

The ’CU878 is characterized for operation from 0 ^{o}C to 70 ^{o}C.

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3.1 Description (cont'd)

Topview

B G A

	1	2	3	4	5	6
A	Y 1	Y 0	$\overline{\text{Y 0}}$	$\overline{\text{Y 5}}$	Y 5	Y 6
B	$\overline{\text{Y 1}}$	G N D	G N D	G N D	G N D	$\overline{\text{Y 6}}$
C	$\overline{\text{Y 2}}$	G N D	N B	N B	G N D	$\overline{\text{Y 7}}$
D	Y 2	V D D Q	V D D Q	V D D Q	O S	Y 7
E	C K	V D D Q	N B	N B	V D D Q	F b in
F	$\overline{\text{C K}}$	V D D Q	N B	N B	O E	$\overline{\text{F b in}}$
G	A G N D	V D D Q	V D D Q	V D D Q	V D D Q	$\overline{\text{F b o u t}}$
H	A V D D	G N D	N B	N B	G N D	F b o u t
J	Y 3	G N D	G N D	G N D	G N D	Y 8
K	$\overline{\text{Y 3}}$	$\overline{\text{Y 4}}$	Y 4	Y 9	$\overline{\text{Y 9}}$	$\overline{\text{Y 8}}$

Figure 1 — 52-Ball VF-BGA (10x6 Array, 7.0x4.5 mm Body Size, 0.65 mm Pitch, MO-225 Variation BA) package pinouts

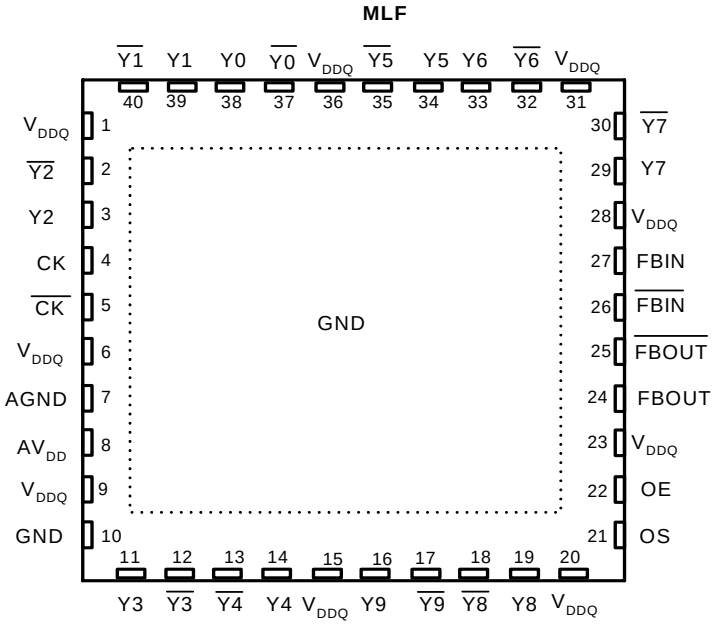

Figure 2 — 40-pin HP-VFQFP-N (6.0x6.0 mm Body Size, 0.5 mm Pitch, MO-220, variation VJJD-2, E2 & D2 nominal = 2.9 mm +/- 0.15 mm) package pinouts

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3.2 Terminal functions

Table 1 — Terminal Functions

Terminal Name	Description	Electrical Characteristics
AGND	Analog Ground	Ground
AV_{DD}	Analog power	1.8 V nominal
CK	Clock input with a (10K-100K Ohm) pulldown resistor	Differential input
$\overline{CK}$	Complementary clock input with a (10K-100K Ohm) pulldown resistor	Differential input
FBIN	Feedback clock input	Differential input
$\overline{FBIN}$	Complementary feedback clock input	Differential input
FBOUT	Feedback clock output	Differential output
$\overline{FBOUT}$	Complementary feedback clock output	Differential output
OE	Output Enable (Asynch)	LVCMOS input
OS	Output Select (tied to GND or V_{DDQ})	LVCMOS input
GND	Ground	Ground
V_{DDQ}	Logic and output power	1.8 V nominal
Y[0:9]	Clock outputs	Differential outputs
$\overline{Y[0:9]}$	Complementary clock outputs	Differential outputs
NB	No ball	

3.3 Function table

Table 2 — Function table

Inputs					Outputs				PLL
AV_{DD}	OE	OS	CK	$\overline{CK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	H	X	L	H	L	H	L	H	Bypassed/ Off
GND	H	X	H	L	H	L	H	L	Bypassed/ Off
GND	L	H	L	H	$*L_{(Z)}$	$*L_{(Z)}$	L	H	Bypassed/ Off
GND	L	L	H	L	$*L_{(Z)}$, Y7 active	$*L_{(Z)}$, $\overline{Y7}$ active	H	L	Bypassed/ Off
1.8V(nom)	L	H	L	H	$*L_{(Z)}$	$*L_{(Z)}$	L	H	On
1.8V(nom)	L	L	H	L	$*L_{(Z)}$, Y7 active	$*L_{(Z)}$, $\overline{Y7}$ active	H	L	On
1.8V(nom)	H	X	L	H	L	H	L	H	On
1.8V(nom)	H	X	H	L	H	L	H	L	On
1.8V(nom)	X	X	L	L	$*L_{(Z)}$	$*L_{(Z)}$	$*L_{(Z)}$	$*L_{(Z)}$	Off
1.8V(nom)	X	X	H	H	Reserved				

* $L_{(Z)}$ means the outputs are disabled to a low state meeting the I_{ODL} limit in Table 5.

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