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Universal Flash Storage Host Controller Interface (UFSHCI), Unified Memory Extension

Version 1.1A

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Foreword

This Unified Memory Extension standard is an extension to the UFSHCI standard, JESD223.

Introduction

The UFSHCI standard defines the interface between the UFS driver and the UFS host controller. In addition to the register interface, it defines data structures inside the system memory, which are used to exchange data, control and status information. Furthermore the UFSHCI standard defines the protocol layer structure and abstract entities within these layers.

Unified Memory offers the possibility to move Device internal working memory into the system memory to reduce overall system cost and to improve Device performance.

The Unified Memory feature impacts Host and Device side. This standard, UFSHCI Unified Memory Extension, describes the requirements to implement Unified Memory functionality in a UFS Host Controller. It is based on the “UFS Unified Memory Extension” standard, which describes the general Unified Memory protocol.

UNIVERSAL FLASH STORAGE HOST CONTROLLER INTERFACE (UFSHCI), UNIFIED MEMORY EXTENSION, Version 1.1

(From JEDEC Board Ballot JCB-13-40 and JCB-15-61, under the cognizance of the JC-64.1 Subcommittee on Electrical Specifications and Command Protocols.)

1 Scope

This document provides a comprehensive definition of the requirements for implementation of a UFS Host Controller, which supports the optional Unified Memory extension.

2 Normative Reference

The following normative documents contain provisions that through reference in this text, constitutes provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

[MIPI-UniPro], *MIPI Alliance Specification for Unified Protocol (UniProSM)*, Version 1.6

[SAM], *INCITS T10 draft standard: SCSI Architecture Model – 5 (SAM–5)*, Revision 05, 19 May 2010

[UFSHCI], JEDEC JESD223C, *Universal Flash Storage Host Controller Interface (UFSHCI)*, Version 2.1

[UFS], JEDEC JESD220C, *Universal Flash Storage (UFS)*, Version 2.1

[UFS-UME], JEDEC JESD220-1A, *UFS Unified Memory Extension*, Version 1.1

3 Keywords, Abbreviations, Acronyms, and Conventions

3.1 Keywords

Several keywords are used to differentiate levels of requirements and options, as follow:

Can: A keyword used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

Expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

Ignored: A keyword that describes bits, bytes, quadlets, or fields whose values are not checked by the recipient.

Mandatory: A keyword that indicates items required to be implemented as defined by this standard.

May: A keyword that indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

Must: The use of the word *must* is deprecated and shall not be used when stating mandatory 61 requirements; *must* is used only to describe unavoidable situations.

Optional: A keyword that describes features which are not required to be implemented by this standard. However, if any optional feature defined by the standard is implemented, it shall be implemented as defined by the standard.

Reserved: A keyword used to describe objects—bits, bytes, and fields—or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization. Usage and interpretation may be specified by future extensions to this or other standards. A reserved object shall be zeroed or, upon development of a future standard, set to a value specified by such a standard. The recipient of a reserved object shall not check its value. The recipient of a defined object shall check its value and reject reserved code values.

Shall: A keyword that indicates a mandatory requirement strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this standard.

Should: A keyword used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).

Will: The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.

3 Keywords, Abbreviations, Acronyms, and Conventions (cont'd)

3.2 Abbreviations

etc. - And so forth (Latin: et cetera)

e.g. - For example (Latin: exempli gratia)

i.e. - That is (Latin: id est)

3.3 Acronyms

BOM	Bill Of Material
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
LUN	Logical Unit Number
NVM	Non-Volatile Memory
PC	Personal Computer
SAP	Service Access Point
SCSI	Small Computer System Interface
SRAM	Static Random Access Memory
TC	Traffic Class
UBMTP	UFS Bus Master Transport Protocol
UFS	Universal Flash Storage
UM	Unified Memory
UMA	Unified Memory Architecture
UME	Unified Memory Extension
UMPIU	Unified Memory Protocol Information Unit
UniPro	Unified Protocol.
UTP	UFS Transport Protocol

3.4 Conventions

The conventions used for registers in this standard are defined in the sections that follow.

Hardware shall return '0' for all bits and registers that are marked as reserved, and host software shall write all reserved bits and registers with the value of '0'.

Inside the register section, the following abbreviations are used:

HwInit	The default state is dependent on device and system configuration. The value is initialized at reset, either by an expansion ROM, or in the case of integrated devices, by a platform BIOS.
Impl Spec	Implementation Specific – the controller has the freedom to choose its implementation.
RO	Read Only
ROC	Read Only and Read to clear
RW	Read Write
R/W	Read Write. The value read may not be the last value written.
RWC	Read/Write '1' to clear
RWS	Read/Write '1' to set