

JEDEC STANDARD

Wide I/O 2 (WideIO2)

JESD229-2

AUGUST 2014

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by

©JEDEC Solid State Technology Association 2014

3103 North 10th Street

Suite 240 South

Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by the JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street, Suite 240 South
Arlington, Virginia 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information

WIDE I/O 2 (WideIO2) STANDARD

(From JEDEC Board Ballot JCB-14-40, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This standard defines Wide I/O 2 (WideIO2), including features, functionality, AC and DC characteristics, packages, and micropillar signal assignments. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant, 8 Gb through 32 Gb SDRAM devices with 4 or 8 64-bit wide channels using direct chip-to-chip attach methods for between 1 and 4 memory devices and a controller/buffer device. This standard was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3) and WIO (JESD229-1). Each aspect of the standard will require approval by committee ballot(s). The accumulation of these ballots will then be incorporated into the WideIO2 standard.

The WideIO2 architecture is an evolution of the WIO architecture to enable bandwidth scaling with capacity.

2 General Description

2.1 Terms and Definitions

Within the WideIO2 standard, these terms have particular meanings:

Stack: All memory chips in the memory system taken together in one assembly. The WideIO2 standard supports memory stacks of up to 4 memory chips.

Slice: One memory chip in the stack of memory chips as shown in Figure 1.

Quadrant: A single memory chip is divided into 4 quadrants as shown in Figure 8.

Micropillar: An electrical connection between two stacked die. The connection is made between the lower die's top metal layer and an upper die's pad by cutting a hole in the passivation on the lower die and inserting a conducting pillar.

Rank: Multiple slices can be connected to a single channel in a multidrop fashion within the memory stack. The DRAM array connected to the channel is referred to as a rank. WideIO2 supports single and dual rank configurations.

Channel: A set of physically discrete connections within the WideIO2 interface that independently control a partition of the WideIO2 device. (see Figure 1).

NOTE The WideIO2 interface supports 4 or 8 physical channels. Each channel contains all the control, data, and clock signals necessary to independently control a partition of the WideIO2 device. Each channel can have different DRAM pages open, can be independently clocked, and can be in different power states. The physical channel also includes I/O power and ground signals. All power and ground signals for all channels must be at their appropriate levels for any portion of the WideIO2 device to operate correctly. The physical channel also contains a reset signal but the WideIO2 interface defines reset to be per slice rather than per channel.

2.1 Terms and Definitions (cont'd)

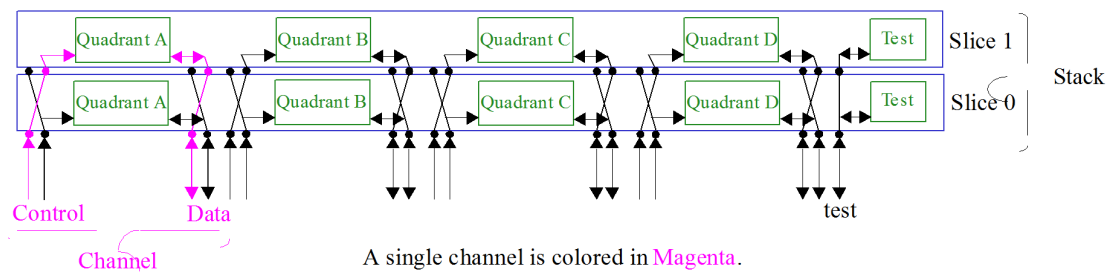


Figure 1 — Definition of Terms for WideIO2 stack

2.2 Key Features

- . Support for 800MT/s and 1067MT/s data rates.
- . 25.6GB/s and 34.1GB/s with four 64b channels (4x64 die)
- . 51.2GB/s and 68.3GB/s with eight 64b channels (8x64 die)
- . DRAM core frequencies of 200MHz and 266MHz.
- . Configurable with 1, 2, or 4 stacked die for bandwidth and capacity scaling.
- . 4KB page size with 8 banks per channel for 4x64 die
- . 2KB page size with 4 banks per channel for 8x64 die
- . 64 Data Bits per channel.
- . Support for burst lengths of 4 and 8.
- . Complementary data strobe for every 16 data bits.
- . Double Data Rate for command and data.
- . Unterminated CMOS I/O signaling
- . No PLL or DLL in the DRAM
- . Per byte write data mask and data bus inversion
- . Multiplexed Command Address (11 CA signals over 2 UI).
- . Each rank in each channel will have its own set of Mode Registers.
- . Each channel is independent.
- . Support for 8, 16, and 32Gb DRAM die density.
- . Per slice scan chain.
- . Per slice Reset.
- . Support for supplier specific Direct Access Mode test feature with 10 digital and 1 analog signals per quadrant.
- . Support for GPIO Mode test access.
- . Support for Post Package Repair
- . Power micropillar count supports current requirements of low-power memory space.
- . VDDQ = VDD2 = 1.1V
- . VDD1 = 1.8V

2.3 Bandwidth vs. Capacity Relationship

The WideIO2 device is targeted to operate up to 800 or 1067MT/s with 64b per channel. The per die density will be either 8, 16, or 32 Gb. Depending on the configuration, the bandwidth and capacity scale as shown in Table 1. The bandwidth is calculated by the transfers x bytes/channel x number of channels. P22P configurations will double the capacity while the bandwidth stays constant.

Table 1 — Capacity vs. Bandwidth (8 - 32Gb Die Density)

Die	Configuration	Capacity	800 MT/s Bandwidth	1067 MT/s Bandwidth	Figure
4x64 Die	1 Slice, 4 Channel	1 - 4GB	25.6GB/s	34.1GB/s	Figure 2
	2 Slice, 8 Channel	2 - 8GB	51.2GB/s	68.3GB/s	Figure 3
	4 Slice, 8 Channel, P22P Dual Rank	4 - 16GB	51.2GB/s	68.3GB/s	Figure 4
8x64 Die	1 Slice, 8 Channel	1 - 4GB	51.2GB/s	68.3GB/s	Figure 5
	2 Slice, 8 Channel, P22P Dual Rank	2 - 8GB	51.2GB/s	68.3GB/s	Figure 6

2.4 WideIO2 Topologies

WideIO2 topologies require a shifting of signals through the stack. This shifting is done in the metal layers of the lower die. The WideIO2 topologies shown in this section are from an SOC point of view (SOC at bottom of stack). A 4 channel topology will only have a single channel (channel 0) for each of the 4 quadrant (A-D). The 4 channels will be referred to as: 0A, 0B, 0C, and 0D. An 8 channel topology will have a channel 0 and channel 1 for each of the 4 quadrants (A-D). The 8 channels will be referred to as: 0A, 1A, 0B, 1B, 0C, 1C, 0D, and 1D. All of the figures in this section will show one of the channels in a magenta color.

2.4.1 WideIO2 Topologies with 4x64 Die

2.4.1.1 1-High 4Ch x 64b

Figure 2 shows the baseline WideIO2 1 slice, 4 channel P2P topology. There are a total of 128 DQs per quadrant with only 64 being used in this topology.

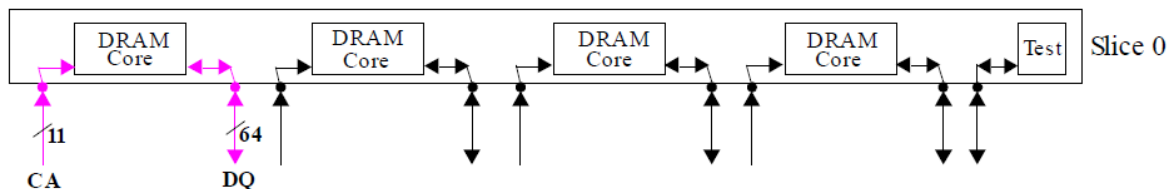


Figure 2 — P2P WideIO2: 1 Slice, 4 Channel

2.4.1.2 2-High 8Ch x 64b Capacity and Bandwidth Scaling

Figure 3 shows a WideIO2 2 slice, 8 channel P2P topology. Since this is an 8 channel, P2P topology, each channel from the second slice increases the overall bandwidth with a constant capacity per channel.

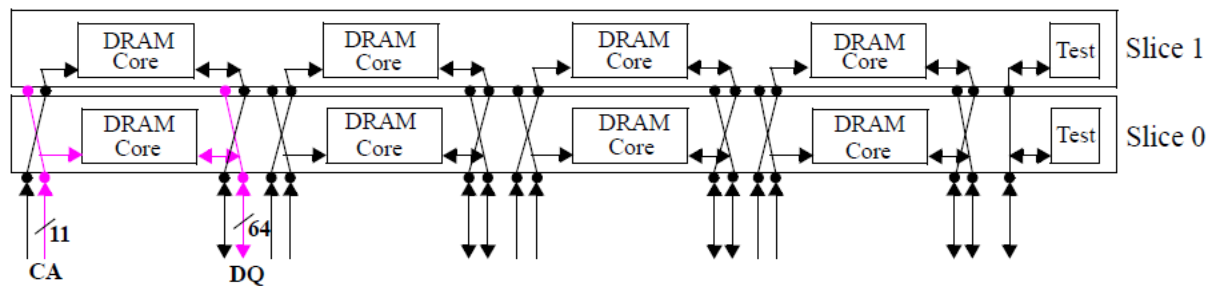


Figure 3 — P2P WideIO2: 2 Slice, 8 Channel

2.4.1.3 4-High, 8Ch x 64b, P22P Capacity and Bandwidth Scaling

Figure 4 shows a WideIO2 4 slice, 2 rank, 8 channel P22P topology with separate CA buses to avoid P24P loading on CA. This configuration scales both capacity and bandwidth.

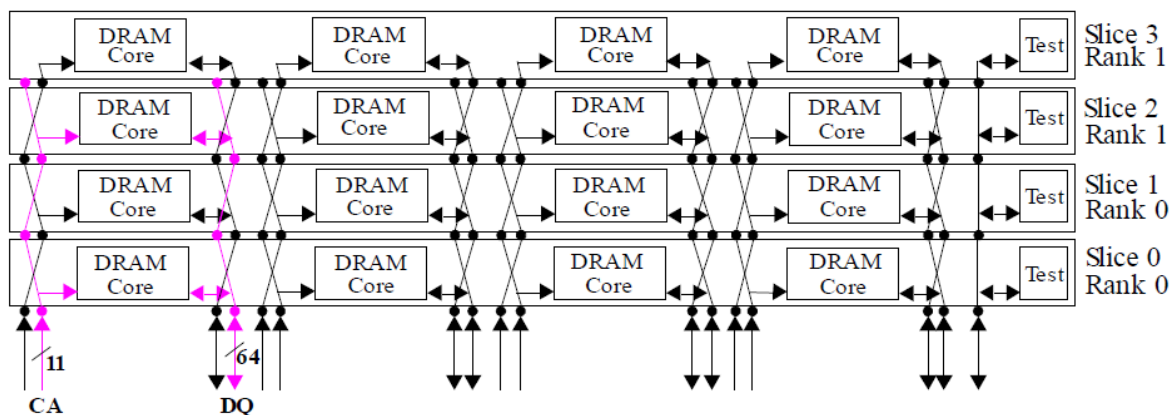


Figure 4 — P22P WideIO2: 4 Slice, 2 Rank, 8 Channel

2.4.2 WideIO2 Topologies with 8x64 Die

2.4.2.1 1-High 8Ch x 64b

Figure 5 shows a WideIO2 1-slice, 8-channel P2P topology.

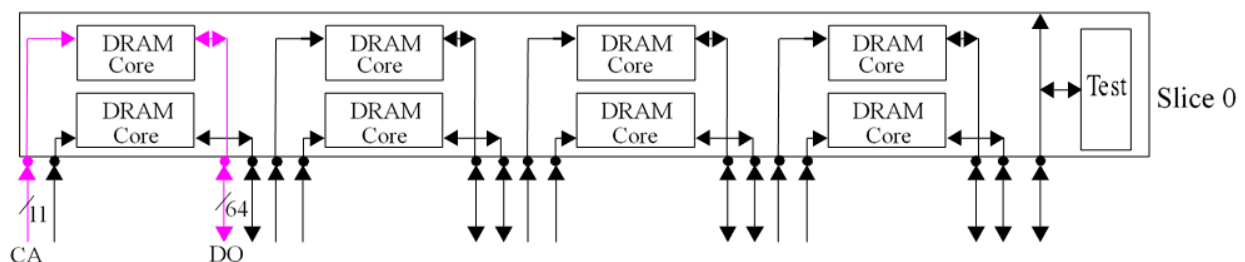


Figure 5 — P2P WideIO2: 1 Slice, 8 Channels

2.4.2.2 2-High 8Ch x 64b

Figure 6 shows a WideIO2 2-slice, 8-channel, P22P topology. The CS and CKE signals are staggered in pairs. CS2/CKE2 is connected to CS0/CKE0 on upper die and CS3/CKE3 is connected to CS1/CKE1 on upper die.

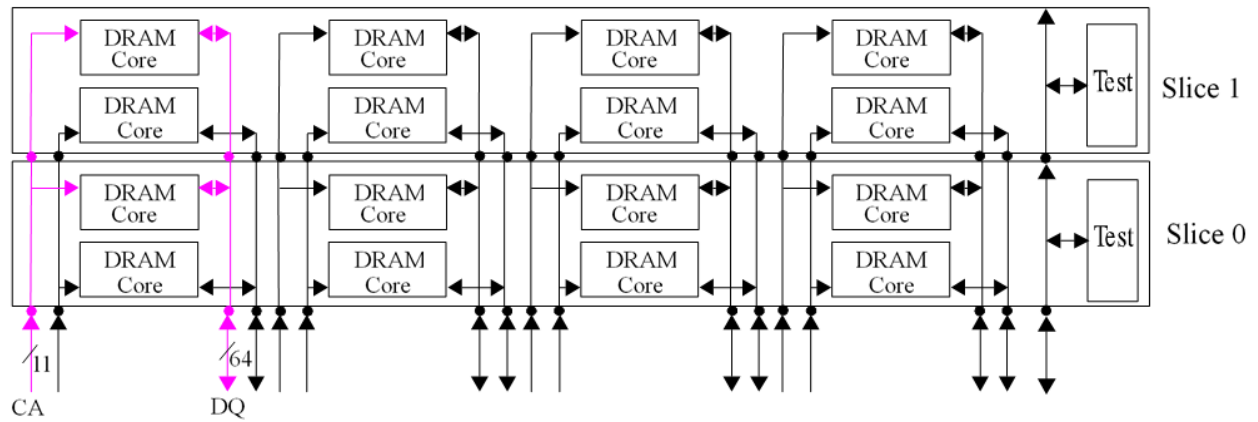


Figure 6 — P22P WideIO2: 2 Slice, 8 Channels

2.5 Micropillar-out

2.5.1 Micropillar Definition and Description

Note on nomenclature: unless otherwise designated, each channel is independent and implements independent sets of the designated micropillars. Signal naming convention designates quadrant and channel within each quadrant as follows:

<SignalName>[1:0][D:A][msb:lsb]

. [1:0] denotes which channel within the quadrant

. [D:A] denotes which quadrant

. [msb:lsb] denotes index of bus

. _n for active low, _t for true, and _c for complement polarity

For example DQ1A13 would be DQ13 in quadrant A channel 1.

Table 2 — Micropillar Definition and Description

Name Signal[Ch] [Quad][bit]	Type	Description
CK[1:0][D:A]_t, CK[1:0][D:A]_c	Input	Clock: CK_t and CK_c are Complementary clock inputs to each channel. All Command signals are sampled on the positive edges of CK_t and CK_c providing a double rate command bus. The clocks are not free running, they will toggle as commands are latched into the device and long enough after the command is latched to allow the command to complete. Clock is defined as the complementary pair CK_t and CK_c.
CA[1:0][D:A][10:0]	Input	Command/Address: There are 11 command/address signals per channel and a command packet is 2UI in length giving a payload of 22 bits of information. The CA bus will be clocked by CK_t/CK_c clocks.
CS[D:A][3:0]_n	Input	Chip Select: CS_n is considered part of the command code. Each of CS[D:A][3:0]_n address a single rank on each of the channels. See Table 20 - Command Truth Table for command code descriptions. See Table 6 for CS_n signal mapping.
CKE[D:A][3:0]	Input	Clock Enables: CKE HIGH activates and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Table 21 - Command Truth Table for command code descriptions. See Table 6 for CKE signal mapping.
DQ[1:0][D:A][63:0]	I/O	Data Inputs/Output: Bi-directional data bus. 64 DQs per channel.
DQS[1:0][D:A][3:0]_t DQS[1:0][D:A][3:0]_c	I/O	Data Strobe (Bi-directional, Complementary): The data strobe is bidirectional (used for read and write data) and complimentary (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t and DQS_c are edge-aligned to read data and centered with write data. Each DQS pair strobes 16 DQ I/Os.
DMI[1:0][D:A][7:0]	I/O	Data Mask and Data Bus Inversion: DMI is a bidirectional signal sampled on the rising edges of DQS_t and DQS_c. See section 3.3.
RST[3:0]_n	Input	Reset: Unidirectional reset inputs. These are per slice reset signals.
SEN[2:0]	Input	Boundary Scan Enable: Used to enable normal operation, boundary scan, or 1 of 6 vendor specific scan chains. Boundary scan modes may be operational in all normal and test modes, as defined by each individual memory vendor.
SSH_n	Input	Boundary Scan Shift: There is one SSH_n provided to all slices in the WideIO2 stack using Through routing.
SDI	Input	Boundary Scan Serial Data In: There is one SDI provided to all slices in the WideIO2 stack using Through routing.
SCK	Input	Boundary Scan Clock: There is one SCK provided to all slices in the WideIO2 stack using Through routing.

Table 2 — Micropillar Definition and Description

Name Signal[Ch] [Quad][bit]	Type	Description
SCS[3:0]_n	Input	Boundary Scan Chip Selects: There is a one SCS[3:0]_n per slice using Staggered routing.
SDO[3:0]	Output	Boundary Scan Output: There is one SDO output per slice using Staggered routing.
TEST	Input	TEST: This input enables memory GPIO test mode. It may be routed through a controller I/O buffer before driving the memory I/O pad.
DAA[D:A]	I/O	Direct Access Analog: This is a vendor specific test feature. These I/Os provide an analog direct access path to DRAM core signals for test/debug purposes. They must be routed directly to external package I/O pads to allow unbuffered visibility to an internal analog signal. They can be connected through the vertical stack in a multidrop topology as defined by each individual memory vendor. There is one DAA per quadrant. DAA pins may be operational in all normal and test modes, as defined by each individual memory vendor.
DA[D:A][9:0]	I/O	Direct Access: This is a vendor specific test feature. These I/Os provide digital direct access to internal DRAM core signals for test/debug purposes. They can be connected through the vertical stack in a multidrop topology as defined by each individual memory vendor. There are 10 digital DA's per quadrant. One of these I/Os may be used to enabled Direct Access test mode. If DA Mode is supported by an SOC design, they must be routed directly to external package I/O pads to allow unbuffered access to these signals. When not in DA mode each DA pin on the device will either be left floating or have a keeper to pull it low. The SOC is not required to pull up or pull down any of the DA pins and should leave these signals floating. The device must account for up to 5uA of SOC leakage current on these signals.
NC	NA	No Connection: This micropillar is a spare and not connected in the WideIO2 device.
VDD1	Supply	Core Voltage Supply 1: Core power supply.
VDD2	Supply	Core Voltage Supply 2: Core power supply.
VDDQ	Supply	I/O Voltage Supply: Power supply for the DQ, DQS, and DMI I/O buffers.
VSS	Supply	Ground
VSSQ	Supply	I/O Ground

NOTE 1 All DA pins must be ESD harden, in the WideIO2 device, up to 2KV HBM (Human Body Model) level or 200V for MM (Machine Model) level, as stated in ANSI/ESDA/JEDEC JS-001-2012 spec.

2.5.2 Quadrant Micropillars

Table 3 — Micropillar Definitions (Per Quadrant)

Micropillar Type	Count	Description
VDD1	12	Core Voltage 1
VDD2	60	Core Voltage 2
VSS	72	Core Ground
VDDQ	42	I/O Voltage
VSSQ	42	I/O Ground
DQ	128	Data
DMI	16	Data Mask and Data Bus Inversion
DQS	16	Complementary Data Strobe: DQS_t, DQS_c
CA	22	Encoded address and command
CS_n	4	Chip Select
CKE	4	Clock Enable
CK	4	Complementary Clock: CK_t, CK_c
Misc	5	Miscellaneous (RST_n, Serial Port, TEST (average. per quadrant))
DAA/DA	11	Direct Access for Test (1 analog, 10 digital)
Total	438	Per Quadrant

NOTE 1 The power and ground signal counts remain the same for both 4 channel and 8 channel configurations (all power and grounds need to be connected for all configurations).

NOTE 2 For configurations with 4 channels the SOC will need to connect their unused signals to a known value.

2.5.3 Channel Interface Signals

Table 4 — Channel Interface Signals

Micropillar Type	Count	Description
DQ	64	Data
DMI	8	Data Mask and Data Bus Inversion
DQS	8	Complementary Data Strobe: DQS_t, DQS_c
CA	11	Encoded address and command
CKE	2	Clock Enable
CS_n	2	Chip Select
CK	2	Complementary Clock: CK_t, CK_c
Total	97	Per Quadrant

2.5.3 Channel Interface Signals (cont'd)

Table 5 — DQS and DMI Mapping

DQ Signal	DQS Mapping	DMI Mapping
DQ[7:0]	DQS[0]_t, DQS[0]_c	DMI[0]
DQ[15:8]	DQS[0]_t, DQS[0]_c	DMI[1]
DQ[23:16]	DQS[1]_t, DQS[1]_c	DMI[2]
DQ[31:24]	DQS[1]_t, DQS[1]_c	DMI[3]
DQ[39:32]	DQS[2]_t, DQS[2]_c	DMI[4]
DQ[47:40]	DQS[2]_t, DQS[2]_c	DMI[5]
DQ[55:48]	DQS[3]_t, DQS[3]_c	DMI[6]
DQ[63:56]	DQS[3]_t, DQS[3]_c	DMI[7]

NOTE 1 The table does not show quadrant and slice information. For example, the DQS true signal for DQ39, Channel 1, Quadrant C would be DQS1C2 (Micropillar Definition and Description).

2.5.4 CKE and CS Mapping

Table 6 — CKE and CS Mapping

Configuration	4x64	8x64
1 High P2P	CKE[0], CS[0] for Ch. 0	CKE[0], CS[0] for Ch. 0 CKE[1], CS[1] for Ch. 1
2 High P2P	CKE[0], CS[0] for Ch. 0 CKE[1], CS[1] for Ch. 1	NA
2 High P22P	NA	CKE[0], CS[0] for Ch. 0 of Rank 0 CKE[1], CS[1] for Ch. 1 of Rank 0 CKE[2], CS[2] for Ch. 0 of Rank 1 CKE[3], CS[3] for Ch. 1 of Rank 1
4 High P22P	CKE[0], CS[0] for Ch. 0 of Rank 0 CKE[1], CS[1] for Ch. 1 of Rank 0 CKE[2], CS[2] for Ch. 0 of Rank 1 CKE[3], CS[3] for Ch. 1 of Rank 1	NA

2.5.5 Test Sub-Block Micropillar Signals

The Test Sub-Block allocates 5 test pins per quadrant. Table 7 shows the signals contained in the Test Sub-Block and Figure 12 shows their micropillar assignments.

Table 7 — Test Sub-Block Micropillar Signals

Signal Name	Type	Number	Description
SEN[2:0]	Input	3	Scan chain enable
SSH_n	Input	1	Boundary scan chain shift
SDI	Input	1	Boundary scan data input
SCK	Input	1	Boundary scan clock
SCS[3:0]_n	Input	4	Boundary scan chip select
SDO[3:0]	Output	4	Boundary scan chain data out
TEST	Input	1	Test mode enable
NC	NA	1	No Connection
RST[3:0]_n	Input	4	Reset Slice (all ranks, quadrants, and channels)
Totals		20	

2.5.6 Bump Plan

The WideIO2 micro-bumps will be a 40um x 40um rectangular pattern as shown in Figure 7. The bumps are divided into 4 quadrants with signal assignments mirrored both horizontally and vertically with the exception of the Test Sub-Block of each quadrant. Figure 8 shows a high level quadrant bump plan. There will be a space between quadrants in the x-direction of 1000um and in the y-direction of 120um (Micropillar center-to-center). Note: Figure 8 is a bottom view looking down upon the memory micropillars, i.e., with the memory micropillars facing out of the page. In the anticipated mounting orientation, this will be looking up from the board.

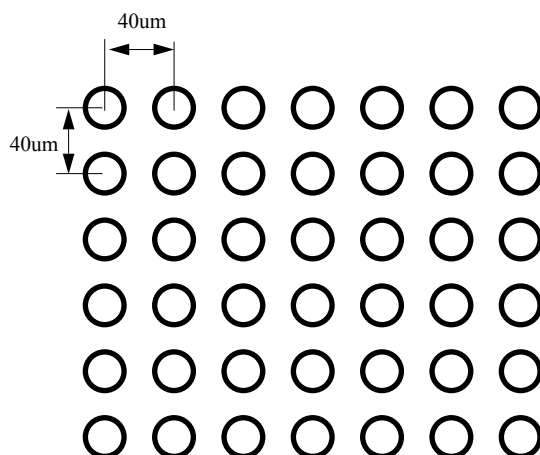
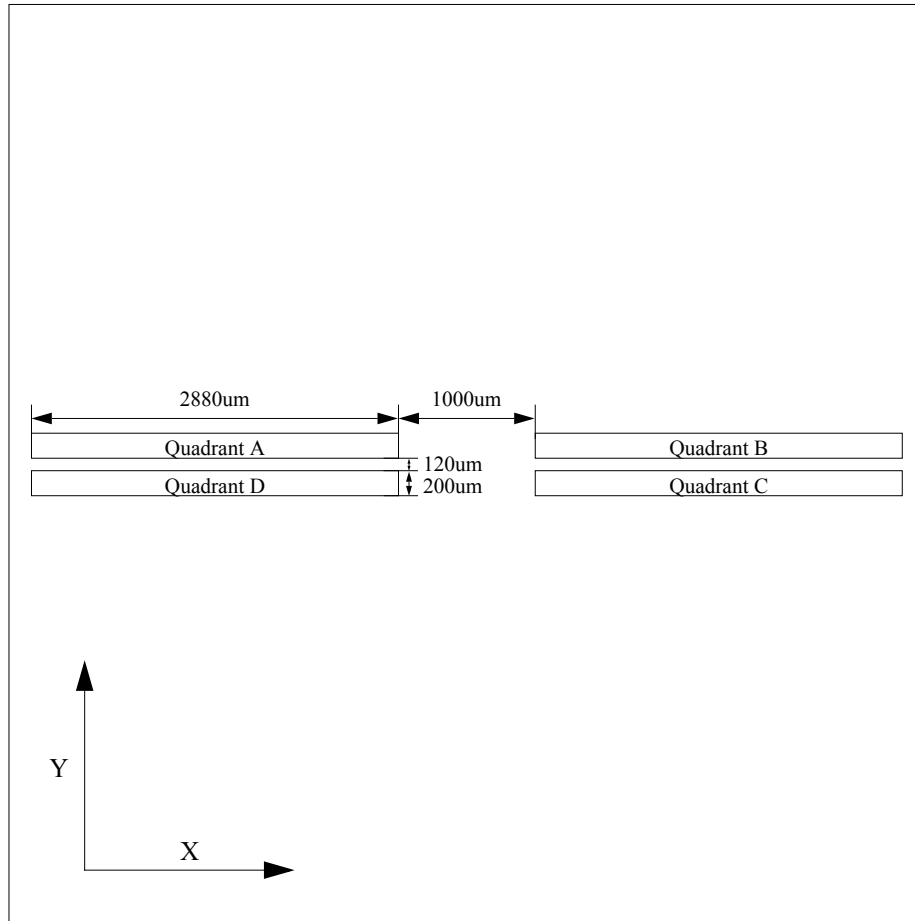


Figure 7 — Bump Pattern

2.5.6 Bump Plan (cont'd)



NOTE 1 Dimensions are micropillar center-to-center.

Figure 8 — Bottom View Quadrant Placement

2.6 TSV Signal Routing

Signal routing through the slices can be Swizzled, Staggered, or Through (see Figure 9). Swizzled routing is used as P2P for 1 or 2-high stack and P22P for 4-high stack. Staggered routing is used to deliver unique signals to each slice. To match capacitive loading, signals will continue up the stack regardless of where they are terminated. Through routing delivers common signals to all slices. Shaded micropillars indicate the active connections in each slice.

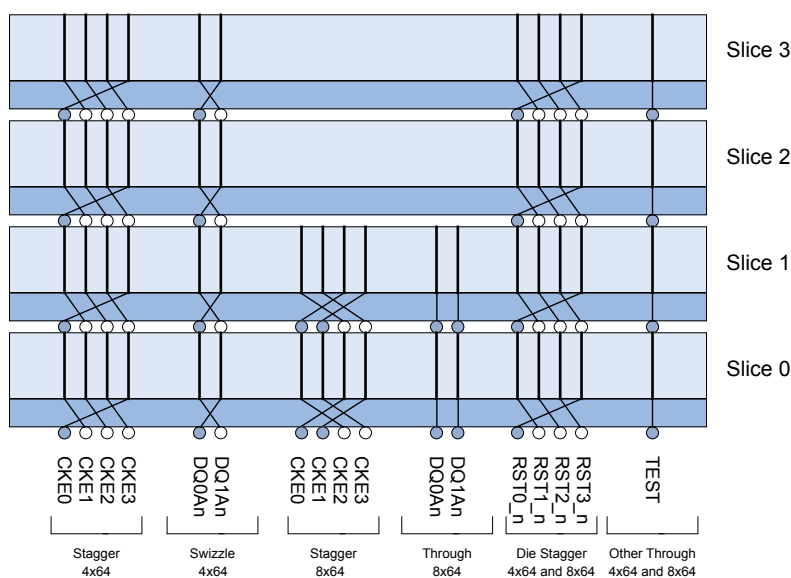


Figure 9 — TSV Routing Example

Table 8 — TSV Signal Routing for 4ch x64b

Signal Name	Routing	Signal Name	Routing
CK[1:0][D:A]_t, CK[1:0][D:A]_c	Swizzled	SSH_n	Through
CA[1:0][D:A][10:0]	Swizzled	SDI	Through
CS[D:A][3:0]_n	Staggered	SCK	Through
CKE[D:A][3:0]	Staggered	SCS[3:0]_n	Staggered
DQ[1:0][D:A][63:0]	Swizzled	SDO[3:0]	Staggered
DQS[1:0][D:A][3:0]_t, DQS[1:0][D:A][3:0]_c	Swizzled	TEST	Through
DMI[1:0][D:A][7:0]	Swizzled	DAA[D:A]	Through
RST[3:0]_n	Staggered	DA[D:A][9:0]	Through
SEN[2:0]	Through		

2.6 TSV Signal Routing (cont'd)

Table 9 — TSV Signal Routing for 8ch x64b

Signal Name	Routing	Signal Name	Routing
CK[1:0][D:A]_t, CK[1:0][D:A]_c	Through	SSH_n	Through
CA[1:0][D:A][10:0]	Through	SDI	Through
CS[D:A][3:0]_n	Staggered	SCK	Through
CKE[D:A][3:0]	Staggered	SCS[3:0]_n	Staggered
DQ[1:0][D:A][63:0]	Through	SDO[3:0]	Staggered
DQS[1:0][D:A][3:0]_t, DQS[1:0][D:A][3:0]_c	Through	TEST	Through
DMI[1:0][D:A][7:0]	Through	DAA[D:A]	Through
RST[3:0]_n	Staggered	DA[D:A][9:0]	Through
SEN[2:0]	Through		

2.6.1 Micropillar Locations

Each WideIO2 channel signal (e.g., DQ0) takes two micropillars; one for channel 0 and one for channel 1 (see Micropillar Definition and Description for signal naming methodology). These signals are swizzled to the slice(s) above as needed (see Table 8). The columns are 6 bumps high alternating between signal and power which allows area on both sides of signal columns for routing. Each quadrant contains one 14-column CA sub-block, one 56-column data sub-block, and one 3-column test sub-block (these sub-blocks column counts include the power supply columns).

Figure 10 shows the CA sub-block for quadrants A and D, Figure 11 shows the data sub-block for quadrant A, and Figure 12 shows the test sub-block for quadrants A, B, C, and D. Since quadrants are flipped images of each other with the only variation in test sub-block, all micropillar locations can be derived from these three figures.

NOTE 1 All views are the bottom views looking down upon the memory micropillars, i.e., with the memory micropillars facing out of the page. In the anticipated mounting orientation, this will be looking up from the board.

Quadrant A																
VDD1			1	2	3	4	5	6	7	8	9	10	11	12	13	14
VDD2		um	0	40	80	120	160	200	240	280	320	360	400	440	480	520
VSS	M	520	VDD1	VSS	VSS	DAA8	VDD2	CA0A6	VSS	CA0A3	VDD2	CA0A0	VSS	CK0A_t	VDD2	CK0A_c
VDDQ	L	480	VDD1	VSS	VSS	CA0A9	VDD2	CA1A6	VSS	CA1A3	VDD2	CA1A0	VSS	CK1A_t	VDD2	CK1A_c
VSSQ	K	440	VDD1	VSS	VSS	CA1A9	VDD2	CA0A7	VSS	CA0A4	VDD2	CA0A1	VSS	CKEA0	VDD2	CSA0_n
DQ	J	400	VDD1	VSS	VSS	CA0A10	VDD2	CA1A7	VSS	CA1A4	VDD2	CA1A1	VSS	CKEA1	VDD2	CSA1_n
DMI	H	360	VDD1	VSS	VSS	CA1A10	VDD2	CA0A8	VSS	CA0A5	VDD2	CA0A2	VSS	CKEA2	VDD2	CSA2_n
DQS	G	320	VDD1	VSS	VSS	DAA9	VDD2	CA1A8	VSS	CA1A5	VDD2	CA1A2	VSS	CKEA3	VDD2	CSA3_n
CA		280														
CS		240														
CKE	F	200	VDD1	VSS	VSS	DAD9	VDD2	CA1D8	VSS	CA1D5	VDD2	CA1D2	VSS	CKED3	VDD2	CSD3_n
CK	E	160	VDD1	VSS	VSS	CA1D10	VDD2	CA0D8	VSS	CA0D5	VDD2	CA0D2	VSS	CKED2	VDD2	CSD2_n
Misc	D	120	VDD1	VSS	VSS	CA0D10	VDD2	CA1D7	VSS	CA1D4	VDD2	CA1D1	VSS	CKED1	VDD2	CSD1_n
DA	C	80	VDD1	VSS	VSS	CA1D9	VDD2	CA0D7	VSS	CA0D4	VDD2	CA0D1	VSS	CKED0	VDD2	CSD0_n
	B	40	VDD1	VSS	VSS	CA0D9	VDD2	CA1D6	VSS	CA1D3	VDD2	CA1D0	VSS	CK1D_t	VDD2	CK1D_c
	A	0	VDD1	VSS	VSS	DAD8	VDD2	CA0D6	VSS	CA0D3	VDD2	CA0D0	VSS	CK0D_t	VDD2	CK0D_c
		um	0	40	80	120	160	200	240	280	320	360	400	440	480	520
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
Quadrant D																

Figure 10 — Quadrant A and D CA Sub-Block Micropillar Locations

2.6.1 Micropillar Locations (cont'd)

15	16	17	18	19	20	21	22	23	24	25	26	27	28
560	600	640	680	720	760	800	840	880	920	960	1000	1040	1080
VSS	DQ0A61	VDDQ	DMI0A7	VSSQ	DQ0A56	VDD2	DAA6	VSS	DQ0A53	VDDQ	DMI0A6	VSSQ	DQ0A48
VSS	DQ1A61	VDDQ	DMI1A7	VSSQ	DQ1A56	VDD2	DQS0A3_t	VSS	DQ1A53	VDDQ	DMI1A6	VSSQ	DQ1A48
VSS	DQ0A62	VDDQ	DQ0A59	VSSQ	DQ0A57	VDD2	DQS1A3_t	VSS	DQ0A54	VDDQ	DQ0A51	VSSQ	DQ0A49
VSS	DQ1A62	VDDQ	DQ1A59	VSSQ	DQ1A57	VDD2	DQS0A3_c	VSS	DQ1A54	VDDQ	DQ1A51	VSSQ	DQ1A49
VSS	DQ0A63	VDDQ	DQ0A60	VSSQ	DQ0A58	VDD2	DQS1A3_c	VSS	DQ0A55	VDDQ	DQ0A52	VSSQ	DQ0A50
VSS	DQ1A63	VDDQ	DQ1A60	VSSQ	DQ1A58	VDD2	DAA7	VSS	DQ1A55	VDDQ	DQ1A52	VSSQ	DQ1A50

29	30	31	32	33	34	35	36	37	38	39	40	41	42
1120	1160	1200	1240	1280	1320	1360	1400	1440	1480	1520	1560	1600	1640
VDD2	DQ0A45	VSS	DMI0A5	VDDQ	DQ0A40	VSSQ	DAA4	VDD2	DQ0A37	VSS	DMI0A4	VDDQ	DQ0A32
VDD2	DQ1A45	VSS	DMI1A5	VDDQ	DQ1A40	VSSQ	DQS0A2_t	VDD2	DQ1A37	VSS	DMI1A4	VDDQ	DQ1A32
VDD2	DQ0A46	VSS	DQ0A43	VDDQ	DQ0A41	VSSQ	DQS1A2_t	VDD2	DQ0A38	VSS	DQ0A35	VDDQ	DA0A33
VDD2	DQ1A46	VSS	DQ1A43	VDDQ	DQ1A41	VSSQ	DQS0A2_c	VDD2	DQ1A38	VSS	DQ1A35	VDDQ	DQ1A33
VDD2	DQ0A47	VSS	DQ0A44	VDDQ	DQ0A42	VSSQ	DQS1A2_c	VDD2	DQ0A39	VSS	DQ0A36	VDDQ	DQ0A34
VDD2	DQ1A47	VSS	DQ1A44	VDDQ	DQ1A42	VSSQ	DAA5	VDD2	DQ1A39	VSS	DQ1A36	VDDQ	DQ1A34

43	44	45	46	47	48	49	50	51	52	53	54	55	56
1680	1720	1760	1800	1840	1880	1920	1960	2000	2040	2080	2120	2160	2200
VSSQ	DQ0A29	VDD2	DMI0A3	VSS	DQ0A24	VDDQ	DAA2	VSSQ	DQ0A21	VDD2	DMI0A2	VSS	DQ0A16
VSSQ	DQ1A29	VDD2	DMI1A3	VSS	DQ1A24	VDDQ	DQS0A1_t	VSSQ	DQ1A21	VDD2	DMI1A2	VSS	DQ1A16
VSSQ	DQ0A30	VDD2	DQ0A27	VSS	DQ0A25	VDDQ	DQS1A1_t	VSSQ	DQ0A22	VDD2	DQ0A19	VSS	DQ0A17
VSSQ	DQ1A30	VDD2	DQ1A27	VSS	DQ1A25	VDDQ	DQS0A1_c	VSSQ	DQ1A22	VDD2	DQ1A19	VSS	DQ1A17
VSSQ	DQ0A31	VDD2	DQ0A28	VSS	DQ0A26	VDDQ	DQS1A1_c	VSSQ	DQ0A23	VDD2	DQ0A20	VSS	DQ0A18
VSSQ	DQ1A31	VDD2	DQ1A28	VSS	DQ1A26	VDDQ	DAA3	VSSQ	DQ1A23	VDD2	DQ1A20	VSS	DQ1A18

57	58	59	60	61	62	63	64	65	66	67	68	69	70
2240	2280	2320	2360	2400	2440	2480	2520	2560	2600	2640	2680	2720	2760
VDDQ	DQ0A13	VSSQ	DMI0A1	VDD2	DQ0A8	VSS	DAA0	VDDQ	DQ0A5	VSSQ	DMI0A0	VDD2	DQ0A0
VDDQ	DQ1A13	VSSQ	DMI1A1	VDD2	DQ1A8	VSS	DQS0A0_t	VDDQ	DQ1A5	VSSQ	DMI1A0	VDD2	DQ1A0
VDDQ	DQ0A14	VSSQ	DQ0A11	VDD2	DQ0A9	VSS	DQS1A0_t	VDDQ	DQ0A6	VSSQ	DQ0A3	VDD2	DQ0A1
VDDQ	DQ1A14	VSSQ	DQ1A11	VDD2	DQ1A9	VSS	DQS0A0_c	VDDQ	DQ1A6	VSSQ	DQ1A3	VDD2	DQ1A1
VDDQ	DQ0A15	VSSQ	DQ0A12	VDD2	DQ0A10	VSS	DQS1A0_c	VDDQ	DQ0A7	VSSQ	DQ0A4	VDD2	DQ0A2
VDDQ	DQ1A15	VSSQ	DQ1A12	VDD2	DQ1A10	VSS	DAA1	VDDQ	DQ1A7	VSSQ	DQ1A4	VDD2	DQ1A2

Figure 11 — Quadrant A Data Sub-Block Micropillar Locations

2.6.1 Micropillar Locations (cont'd)

Quadrant A				Quadrant B			
71	72	73			74	75	76
2800	2840	2880			3880	3920	3960
VSS	DAAA	VDD1			VDD1	DAAB	VSS
VSS	SDI	VDD1			VDD1	SDO0	VSS
VSS	SCK	VDD1			VDD1	SDO1	VSS
VSS	SSH_n	VDD1			VDD1	SDO2	VSS
VSS	SEN0	VDD1			VDD1	SDO3	VSS
VSS	SEN1	VDD1			VDD1	NC	VSS
VSS	SEN2	VDD1			VDD1	TEST	VSS
VSS	SCS3_n	VDD1			VDD1	RST3_n	VSS
VSS	SCS2_n	VDD1			VDD1	RST2_n	VSS
VSS	SCS1_n	VDD1			VDD1	RST1_n	VSS
VSS	SCS0_n	VDD1			VDD1	RST0_n	VSS
VSS	DAAD	VDD1			VDD1	DAAC	VSS
2800	2840	2880			3880	3920	3960
71	72	73			74	75	76
Quadrant D				Quadrant C			

Figure 12 — Quadrants A, B, C, and D Test Sub-Block Micropillar Locations

2.7 Addressing

2.7.1 Addressing for 4x64 Die

Table 10 shows WideIO2 addressing for 4x64 die supported slice densities.

Table 10 — Address Table (4x64 Die)

Parameter	Density					Notes
	8Gb	12Gb	16Gb	24Gb	32Gb	
Prefetch Size	256b	256b	256b	256b	256b	
Row Address	RA[12:0]	RA[13:0] ³⁾	RA[13:0]	RA[14:0] ⁴⁾	RA[14:0]	
Column Address	CA[8:0]	CA[8:0]	CA[8:0]	CA[8:0]	CA[8:0]	1,2
Bank Address	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	BA[2:0]	
Page Size	4KB	4KB	4KB	4KB	4KB	

NOTE 1 The least-significant column address C0 is not transmitted on the CA bus and is implied to be zero.

NOTE 2 CA[1] is used to drive 16B critical data first in burst order for BL4 transfers. CA[2:1] are used to drive 16B critical data first in burst order for BL8.

NOTE 3 No memory present at addresses with R12=R13=HIGH. ACT command with R12=R13=HIGH is ignored (NOP). Write to R12=R13=HIGH is ignored (NOP).

NOTE 4 No memory present at addresses with R13=R14=HIGH. ACT command with R13=R14=HIGH is ignored (NOP). Write to R13=R14=HIGH is ignored (NOP).

2.7.2 Addressing for 8x64 Die

Table 11 shows WideIO2 addressing for 8x64 supported slice densities.

Table 11 — Address Table (8x64 Die)

Parameter	Density					Notes
	8Gb	12Gb	16Gb	24Gb	32Gb	
Prefetch Size	256b	256b	256b	256b	256b	
Row Address	RA[13:0]	RA[14:0] ³⁾	RA[14:0]	RA[15:0] ⁴⁾	RA[15:0]	
Column Address	CA[7:0]	CA[7:0]	CA[7:0]	CA[7:0]	CA[7:0]	1,2
Bank Address	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	BA[1:0]	
Page Size	2KB	2KB	2KB	2KB	2KB	

NOTE The least-significant column address C0 is not transmitted on the CA bus and is implied to be zero.

NOTE 2 CA[1] is used to drive 16B critical data first in burst order for BL4 transfers. CA[2:1] are used to drive 16B critical data first in burst order for BL8.

NOTE 3 No memory present at addresses with R13=R14=HIGH. ACT command with R13=R14=HIGH is ignored (NOP). Write to R13=R14=HIGH is ignored (NOP).

NOTE 4 No memory present at addresses with R14=R15=HIGH. ACT command with R14=R15=HIGH is ignored (NOP). Write to R14=R15=HIGH is ignored (NOP).

3.1 State Diagram

For a complete definition of the device behavior, the information provided in Figure 13 should be integrated with the truth tables and timing specification.

The diagram illustrates the state transitions for the 7T1000 device. States are represented by circles, and transitions are labeled with commands. A legend indicates that thick lines represent the Automatic Sequence and thin lines represent the Command Sequence.

- Power Applied** leads to **Power Ramp**.
- Power Ramp** leads to ***2 Reset** via the **Reset Procedure *2**.
- From any state *2 Reset Procedure** leads to ***2 Reset**.
- *2 Reset** leads to **Idle *1** via the **Initialization Procedure**.
- Idle *1** is the central state with multiple transitions:
 - MRW** (Automatic) and **MRR** (Automatic) lead to **MR Write** and **Idle MR Read** respectively.
 - SREF** (Automatic) and **SREFX** (Command) lead to **Self Refresh**.
 - REFA** (Automatic) leads to **Refresh**.
 - PD** (Automatic) and **PDX** (Automatic) lead to **Idle Power Down**.
 - ACT** (Automatic) leads to **Active**.
- Active** is the central state with multiple transitions:
 - MRR** (Automatic) leads to **Active MR Read**.
 - PD** (Automatic) and **PDX** (Automatic) lead to **Active Power Down**.
 - WR/MWR** (Automatic) leads to **Write or Masked WR**.
 - RD** (Automatic) leads to **Read**.
 - PR, PRA** (Automatic) leads to **Precharge**.
- Write or Masked WR** has a self-loop labeled **WR/MWR** and leads to **Write/Masked WR with Autoprecharge** via **WRA MWRA**.
- Read** has a self-loop labeled **RD** and leads to **Read with Autoprecharge** via **RDA**.
- Write/Masked WR with Autoprecharge** and **Read with Autoprecharge** both lead to **Precharge** via thick Automatic Sequence lines.
- Precharge** leads back to **Idle *1** via a thick Automatic Sequence line.
- Active** also has a direct thick Automatic Sequence line leading to **Precharge**.

PR(A) = Precharge (All)
 ACT = Activate
 WR(A) = Write (with Autoprecharge)
 Masked WR(A) = Masked Write (with Autoprecharge)
 RD(A) = Read (with Autoprecharge)
 Reset = Reset Procedure
 MRW = Mode Register Write
 MRR = Mode Register Read
 PD = Enter Power Down
 PDX = Exit Power Down
 SREF = Enter Self Refresh
 SREFX = Exit Self Refresh
 REFA = Auto Refresh

NOTE 1 For Wide I/O2 DRAM in the Idle state, all banks are precharged.
NOTE 2 Reset Function are per slice (not per channel)

Figure 13 — WideIO2 Device Simplified State Diagram

3.2 Power-up, Initialization, and Power-off

3.2.1 Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory to avoid permanent damage to the WideIO2 device.

1. Voltage Ramp: While applying power, RST_n is recommended to be maintained below $0.2 \times V_{DD2}$; all other inputs shall be between V_{ILmin} and V_{IHmax} . Voltage ramp power supply requirements are provided in Table 12.

Table 12 — Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than $V_{DD2}-200mV$
	V_{DD1} and V_{DD2} must be greater than $V_{DDQ}-200mV$

NOTE 1 Ta is the point when any power supply first reaches 300mV.

NOTE 2 Noted conditions apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply and reference voltages are within their defined operating ranges.

NOTE 4 Power ramp duration t_{INIT0} ($T_b - T_a$) must not exceed 20ms.

NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not exceed 100mV.

NOTE 6 The Wide IO2 DRAM device will guarantee that outputs are in a high impedance state while RST_n is held low.

2. RST_n: RST_n must be maintained for a minimum 200 us with stable power. CKE must be pulled “Low” a minimum of 10ns before RST_n is de-asserted.

3. CKE and Clock: After RST_n is de-asserted, CKE must remain deasserted for 2 ms. During this time, the DRAM will initialize internal state independent of external clocks. The clock must be started and stable for at least 5 clocks before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must also be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) the clock before CKE goes active. After CKE is registered high, tINIT5 must pass before issuing the MRS command to load a mode register.

4. MR: Issue MRS Command(s) to load mode registers with all application settings.

5. Normal Operation: The Wide IO2 DRAM device is now ready for normal operation.

3.2.1 Voltage Ramp and Device Initialization (cont'd)

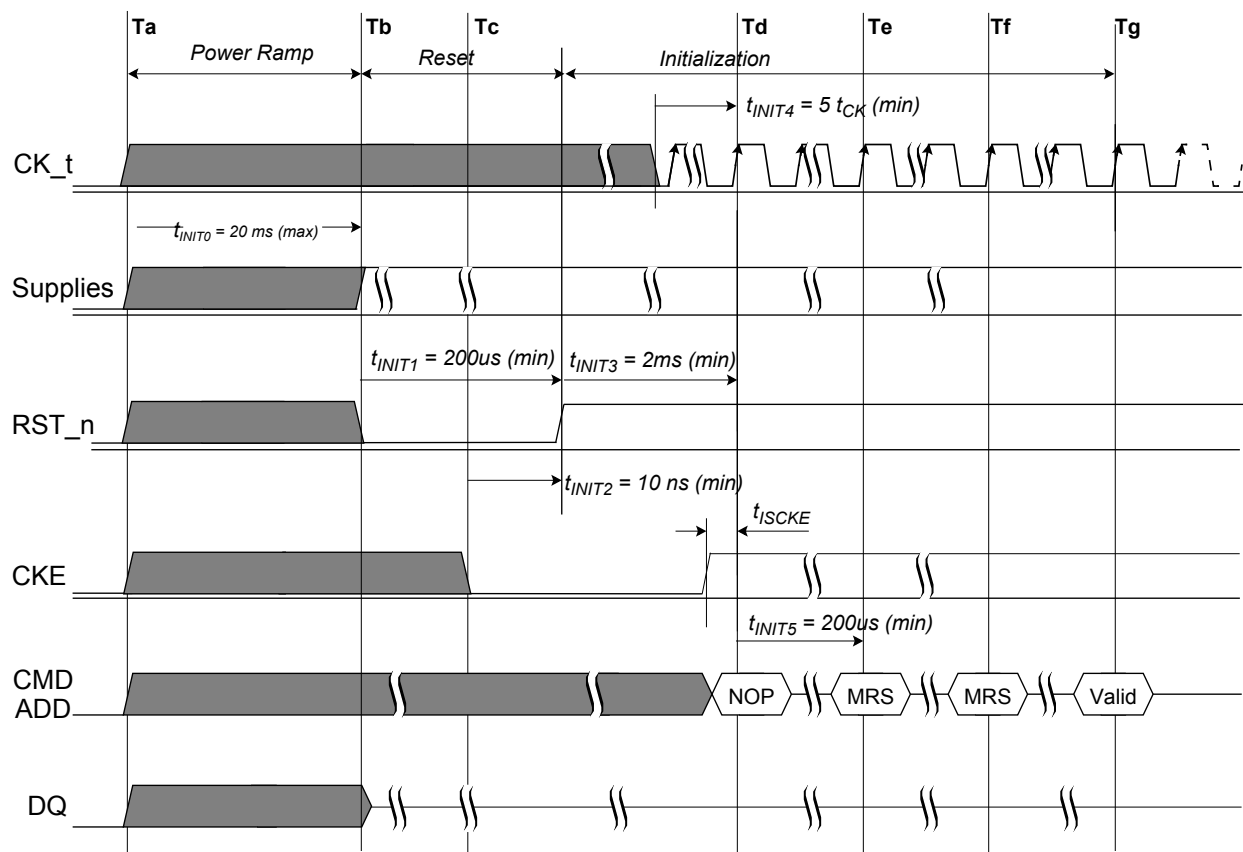


Figure 14 — Voltage Ramp and Initialization Sequence

NOTE 1 High-Z on the CA bus indicates NOP.

NOTE 2 For t_{INIT} values, see Table 13.

Table 13 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	200		us	Minimum RST _n low Time with stable power
t_{INIT2}	10		ns	Minimum CKE low Time before RST _n high
t_{INIT3}	2		ms	Minimum CKE low Time after RST _n high
t_{INIT4}	5		tCK	Minimum stable clock before first CKE high
t_{INIT5}	200		us	Minimum idle time after first CKE assertion

3.2.2 Reset Initialization with stable power

The following sequence is required for RESET with no power interruption initialization.

1. Assert RST_n (active low) anytime when reset is needed. All other inputs may be undefined. RST_n must be maintained for at least 100 ns. CKE must be pulled “LOW” 10ns before RST_n is deasserted.
2. Follow the Power-up and Initialization Sequence steps 3 and 4.
3. The Reset sequence is now completed; The Wide IO2 DRAM device is ready for normal operation.

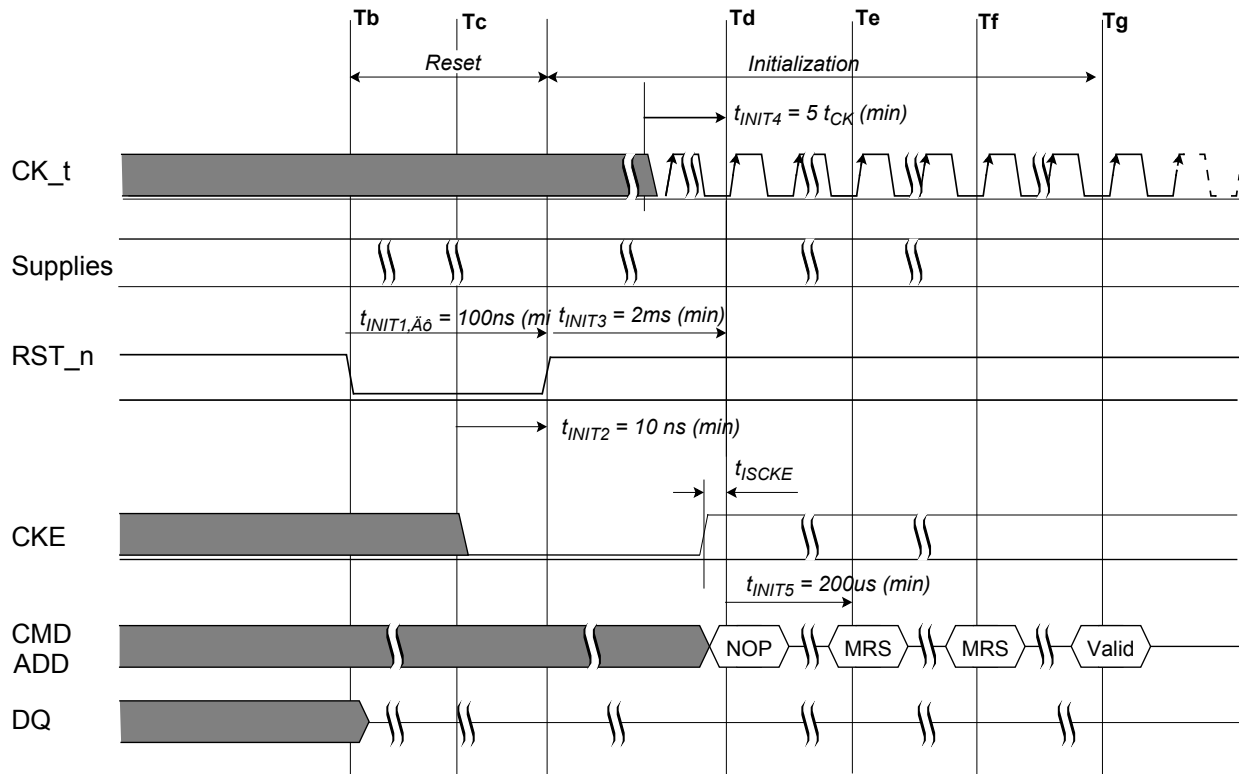


Figure 15 — Reset Initialization with stable Power

Table 14 — Timing Parameters for Reset Initialization with stable Power

Symbol	Value		Unit	Comment
	min	max		
t_{INIT1}	100		ns	Minimum RST_n low Time for Reset Initialization with stable power
t_{INIT2}	10		ns	Minimum CKE low Time before RST_n high
t_{INIT3}	2		ms	Minimum CKE low Time after RST_n high
t_{INIT4}	5		t_{CK}	Minimum stable clock before first CKE high
t_{INIT5}	200		us	Minimum idle time after first CKE assertion

3.2.3 Power-off Sequence

The following sequence shall be used to power off the Wide IO2 DRAM device. Unless specified otherwise, these steps are mandatory.

If system requires DQ remain Hi-Z while removing power, RST_n shall be held at a logic low level ($\leq 0.2 \times V_{DD2}$) or CKE shall be held in logic low level. All other inputs shall be between V_{ILmin} and V_{IHmax} . The Wide IO2 DRAM device will guarantee that outputs are in a high impedance state while RST_n is held low.

Tx is the point where any power supply decreases under its minimum value specified in Table 42, DC operating conditions.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

Table 15 — Power Supply Conditions

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than $V_{DD2} - 200\text{mV}$
Tx and Tz	V_{DD1} and V_{DD2} must be greater than $V_{DDQ} - 200\text{mV}$

The voltage difference between VSS and VSSQ micropillars may not exceed 100 mV.

3.2.3 Power-off Sequence (cont'd)

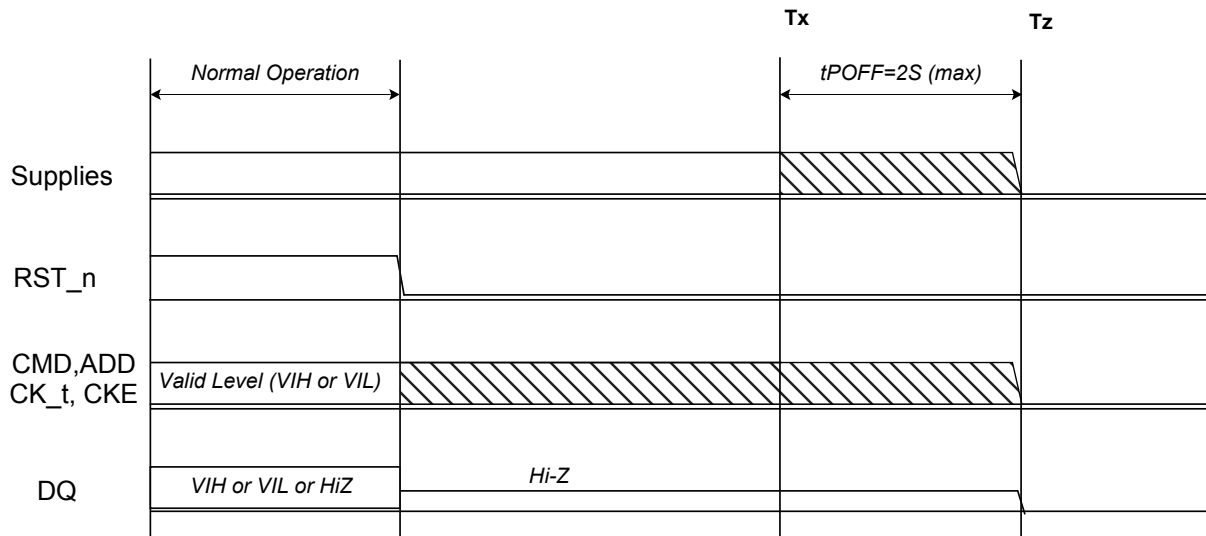


Figure 16 — Power-Off Sequence with RST_n

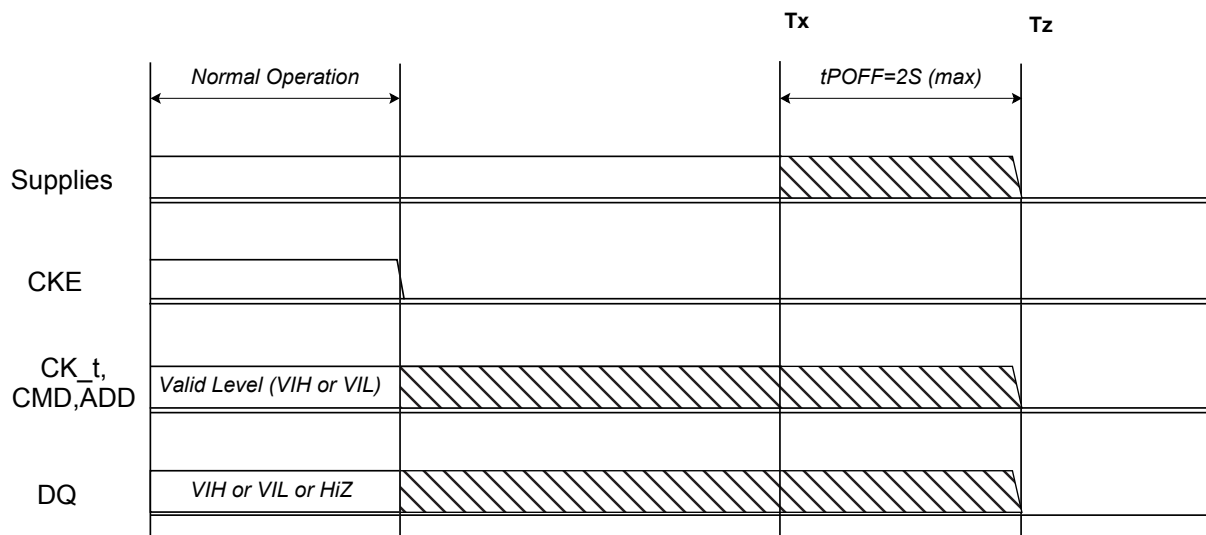


Figure 17 — Power-Off Sequence with CKE

3.2.4 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/ μ s between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 16 — Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

3.3 Input Clock Stop and Frequency Change

WideIO2 devices support input clock frequency change during CKE LOW under the following conditions:

- . tCK(MIN) and tCK(MAX) are met for each clock cycle;
- . Refresh Requirements apply during clock frequency change;
- . During clock frequency change, only REF commands may be executing;
- . Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- . The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
- . The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- . The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRS commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

WideIO2 devices support clock stop during CKE LOW under the following conditions:

- . CK_t is held LOW and CK_c is held HIGH during clock stop;
- . Refresh Requirements apply during clock stop;
- . During clock stop, only REF commands may be executing;
- . Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- . The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
- . The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- . The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

WideIO2 devices support input clock frequency change during CKE HIGH under the following conditions:

- . tCK(MIN) and tCK(MAX) are met for each clock cycle;
- . Refresh Requirements apply during clock frequency change;
- . Any Activate, Read, Write, Precharge, Mode Register Set, or Status Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- . The related timing conditions (tRCD, tWR, tRP, tMRD, tSRR, etc.) have been met prior to changing the frequency;
- . CS_n shall be held HIGH during clock frequency change;
- . During clock frequency change, only REF commands may be executing;
- . The WideIO2 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

After the input clock frequency is changed, additional MRS commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

WideIO2 devices support clock stop during CKE HIGH under the following conditions:

- . CK_t is held LOW and CK_c is held HIGH during clock stop;
- . CS_n shall be held HIGH during clock stop;
- . Refresh Requirements apply during clock stop;
- . During clock stop, only REF commands may be executing;
- . Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- . The related timing conditions (tRCD, tWR, tRP, tMRD, tSRR, etc.) have been met prior to stopping the clock;

The WideIO2 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

3.4 Mode Register Definition

For application flexibility, various functions, features, and modes are programmable in WideIO2 Mode Registers. Values are programmed into Mode Registers via a Mode Register Write (MRW) command. The default values of the Mode Registers (MR#) are defined so they must be programmed during the reset and initialization sequence. The Mode Registers are defined for one channel.

The contents of the Mode Registers can be altered by re-executing the MRW command during normal operation. When programming the Mode Registers, even if the user chooses to modify only a sub-set of the MRW fields, all address fields within the accessed Mode Register will be redefined when the MRW command is issued.

MRW commands do not affect array contents regardless of when these commands are executed.

After the Mode Register write command, tMRD is required to complete the write operation to the Mode Register. tMRW is the minimum time required between two MRW commands.

Table 17 shows the mode registers for WideIO2 SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 17 — Mode Register Assignment in WideIO2 SDRAM

	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	(Reserved)	(RFU)	(RFU)							
1	Device Feature-1	W	nWR			RRO	Programma- ble postamble	BL		
2	Device Feature-2	W	SRA	PPRE	WL			RL & nRTP		
3	I/O Config-1	W	DBI WE	DBI RE	Thermal offset		DME	DS		
4	Refresh Rate	R	TUF	(RFU)			Refresh Mode	SDRAM Refresh Rate		
5	Basic Config-1	R	Wide IO2 manufacturer ID							
6	Basic Config-2	R	Revision ID1							
7	Basic Config-3	R	Revision ID2							
8	Basic Config-4	R	(RFU)	IO Width / channel		Density / die			Channel / die	
9	Test Mode	W	Test Mode							
10	(Reserved)	(RFU)	(RFU)							
11	PASR-1	W	Bank Masking							
12	PASR-2	W	Segment Masking							
13	PPR Resources	R	Post Package Repair							
14	TRR-1	W	TRR Mode	TRR Mode - Bank			(RFU)			
15	TRR-2	R	(RFU)				Mac Cap.	Mac Value		

NOTE 1 RFU bits shall be set to ‘0’ during mode register writes.

NOTE 2 RFU bits shall be read as ‘0’ during mode register reads.

NOTE 3 All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.

NOTE 4 All mode registers that are specified as RFU shall not be written.

NOTE 5 See vendor device datasheets for details on vendor specific mode registers

NOTE 6 Writes to read-only registers shall have no impact on the functionality of the device.

NOTE 7 Mode Register Read data OP0 is delivered on DQ0 and so forth.

3.4.1 MR0_Reserved (MA<7:0> = 00_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)							

3.4.2 MR1_Device Feature 1 (MA<7:0> = 01_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			RRO	Programmable Postamble	BL		

BL	Write-only	OP<2:0>	010_B : BL4 (default) 011_B : BL8 111_B : BL4 or BL8 (on the fly enabled) All others : Reserved	
Programmable Read Post-amble		OP<3>	0_B : Standard Post-amble (default) 1_B : Extended Post-amble	
RRO (Refresh Rate Option)		OP<4>	0_B : Disable codes 001 and 010 in MR4 OP[2:0] (default) 1_B : Enable all codes in MR4 OP[2:0]	1,2,3
nWR		OP<7:5>	010_B : nWR=6 (default) 011_B : nWR=7 100_B : nWR=8 101_B : nWR=10 110_B : nWR=11 All others : Reserved	4

NOTE 1 MR1 OP4 RRO bit is valid only when MR4 OP3 = 1. For WideIO2 devices with MR4 OP3 = 0, MR4 OP[2:0] bits are not dependent on MR1 OP4.

NOTE 2 When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. WideIO2 devices must report 011b instead of 001b or 010b in this case.

NOTE 3 TCSR function does not depend on RRO setting.

NOTE 4 Programmed value in nWR register determines when to start internal precharge operation for a write burst with AP (nWR).

Table 18 — Burst Sequence

C2	C1	C0	BT	BL	Burst Cycle Number and Burst Address Sequence							
					1	2	3	4	5	6	7	8
X	0 _B	0 _B	seq	4	0	1	2	3				
X	1 _B	0 _B			2	3	0	1				
0 _B	0 _B	0 _B	seq	8	0	1	2	3	4	5	6	7
0 _B	1 _B	0 _B			2	3	0	1	6	7	4	5
1 _B	0 _B	0 _B			4	5	6	7	0	1	2	3
1 _B	1 _B	0 _B			6	7	4	5	2	3	0	1

NOTE 1 C0 input is not present on CA bus. It is implied zero.

NOTE 2 For BL=4, the burst address represents C1 - C0.

NOTE 3 For BL=8, the burst address represents C2 - C0.

3.4.3 MR2_Device Feature 2 (MA<7:0> = 02_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
SRA	PPRE	WL					RL & nRTP

RL & nRTP	Write-only	OP<2:0>	DBI disable (MR3 OP[6] = 0B) 000_B : RL=5, nRTP=2 (default) 001_B : RL=6, nRTP=3 010_B : RL=7, nRTP=3 011_B : RL=8, nRTP=4 100_B : RL=9, nRTP=4 All others : reserved DBI enable (MR3 OP[6] = 1B) 000_B : RL=6, nRTP=2 001_B : RL=7, nRTP=3 010_B : RL=8, nRTP=3 011_B : RL=9, nRTP=4 100_B : RL=10, nRTP=4 All others : reserved
WL		OP<5:3>	000_B : WL=3 (default) 001_B : WL=4 010_B : WL=5 011_B : WL=6 100_B : WL=7 All others : reserved
PPRE (Post Package Repair Entry/Exit)		OP<6>	0_B : PPR mode exit (default) 1_B : PPR mode entry
SRA (Self Refresh Abort)		OP<7>	0_B : Self-Refresh Abort disabled (default) 1_B : Self-Refresh Abort enabled

NOTE 1 Self Refresh Abort is only implemented for 12Gb densities and above.

Read Latency		Write Latency	nWR	nRTP	Lower Frequency limit (Greater than)	Upper Frequency Limit (Same or less than)	Unit
No DBI	W/ DBI						
5	6	3	6	2	10	266	MHz
6	7	4	7	3	266	333	
7	8	5	8	3	333	400	
8	9	6	10	4	400	466	
9	10	7	11	4	466	533	

NOTE 1 The Wide I/O2 SDRAM device should not be operated at a frequency below the Lower-Frequency Limit shown for each RL, WL, or nWR value.

NOTE 2 The Wide I/O2 SDRAM device should not be operated at a frequency above the Upper Frequency Limit shown for each RL, WL, or nWR value.

3.4.4 MR3_I/O Configuration 1 (MA<7:0> = 03_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI WE	DBI RE	Thermal Offset		DME	DS		

DS (Driver Strength)	Write-only	OP<2:0>	000 _B : Weak 001 _B : Strong (default) All others : Reserved
DME		OP<3>	0 _B : Data Mask Disable 1 _B : Data Mask Enable (default)
Thermal Offset		OP<5:4>	00 _B : No offset, 0~5°C gradient (default) 01 _B : 5 °C offset, 5~10°C gradient 10 _B : 10°C offset, 10~15°C gradient 11 _B : Reserved
DBI RE		OP<6>	0 _B : Data Bus Inversion on Reads Disable (default) 1 _B : Data Bus Inversion on Reads Enable
DBI WE		OP<7>	0 _B : Data Bus Inversion on Writes Disable (default) 1 _B : Data Bus Inversion on Writes Enable

3.4.4.1 Thermal Offset

Because of their tight thermal coupling with WideIO2 DRAMs, hot spots on WideIO2 controllers can induce thermal gradients into the DRAMs. As these hot spots may not be located near the DRAM thermal sensor, the DRAM's temperature compensated selfrefresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR3 in channel A0 and it will not be affected through MR3 in the other channels. This temperature offset will modify refresh behavior for all channels in the slice. If the induced thermal gradient from controller's corresponding location for temperature sensor location of DRAM to hot spot location of controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents.

During normal operation, the controller will update this register in channel A0 whenever it detects changes in the induced thermal gradient. Updating this register may modify the self-refresh behavior for all channels, including channels in self-refresh operation. It will take max tRRU(Refresh Rate Update) to change self-refresh period and have the change reflected in MR4.

To accurately determine the controller die's temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the WideIO2 memory controller.

To ensure that the memory thermal sensor is located above an X-Y location on the controller, the memory thermal sensor must be located within a rectangle centered on the memory-controller physical interface. Additionally, the minimum size of a controller that wants to use this feature is within that rectangle as otherwise the memory's thermal sensor could be located outside the controller die's perimeter.

3.4.5 MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)			Refresh mode	SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	000_B : SDRAM Low temperature operating limit exceeded 001_B : 4x t _{REFI} , 4x t _{REFIpb} , 4x t _{REFW} 010_B : 2x t _{REFI} , 2x t _{REFIpb} , 2x t _{REFW} 011_B : 1x t _{REFI} , 1x t _{REFIpb} , 1x t _{REFW} (<=85'C) 100_B : 0.5x t _{REFI} , 0.5x t _{REFIpb} , 0.5x t _{REFW} , do not de-rate SDRAM AC timing (optional) 101_B : 0.25x t _{REFI} , 0.25x t _{REFIpb} , 0.25x t _{REFW} , do not de-rate SDRAM AC timing 110_B : 0.25x t _{REFI} , 0.25x t _{REFIpb} , 0.25x t _{REFW} , de-rate SDRAM AC timing 111_B : SDRAM High temperature operating limit exceeded
Refresh mode		OP<3>	0_B : Both legacy & modified refresh mode supported 1_B : Only modified refresh mode supported
Temperature Update Flag (TUF)		OP<7>	0_B : OP<2:0> value has not changed since last read of MR4. 1_B : OP<2:0> value has changed since last read of MR4.

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.

NOTE 2 OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85 °C.

NOTE 4 OP7 is set to '1' if OP[2:0] has changed at any time since the last read of MR4.

NOTE 5 WideIO2 might not operate properly when OP[2:0] = 000B or 111B

NOTE 6 WideIO2 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in temperature derating table¹. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.

NOTE 7 See 3.4.5.1, Temperature Sensor, for information on the recommended frequency of reading MR4.

NOTE 8 MR4 in channel 0A will only provide the information, and the other channels will not provide.

1. As of publication of this document, under discussion by the formulating committee.

3.4.5.1 Temperature Sensor

WideIO2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

WideIO2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85 °C when MR4[2:0] equals 'b011. WideIO2 devices shall allow for 2 °C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2 \text{ }^{\circ}\text{C}$$

Table 19 — Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if Temp Gradient is 10 °C/s and the SysRespDelay is 1 ms:

$$(10 \text{ }^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2 \text{ }^{\circ}\text{C}$$

In this case, ReadInterval shall be no greater than 167 ms.

3.4.5.1 Temperature Sensor (cont'd)

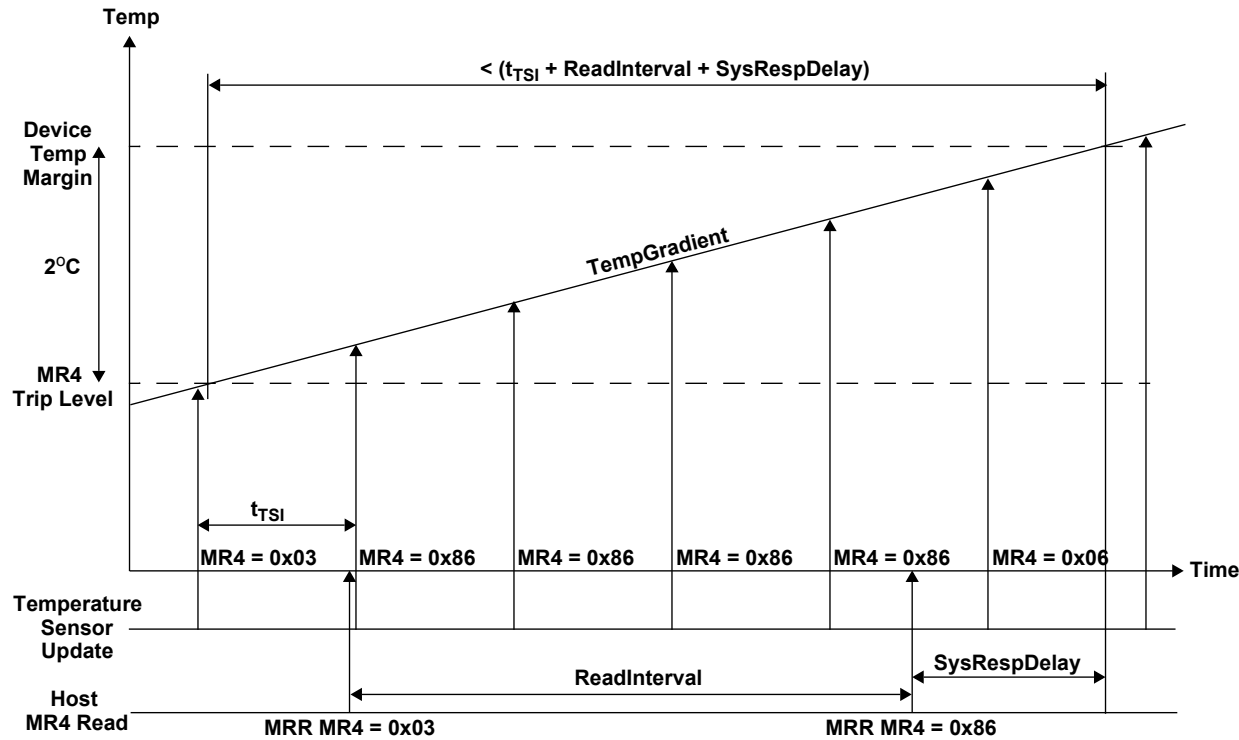


Figure 18 — Temp Sensor Timing

3.4.6 MR5_Basic Configuration 1 (MA<7:0> = 05_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Wide IO2 Manufacturer ID							

Wide IO2 Manufacturer ID	Read-only	OP<7:0>	See JEP166, WideIO2 Manufacturer ID Codes
--------------------------	-----------	---------	---

3.4.7 MR6_Basic Configuration 2 (MA<7:0> = 06_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	00000000 _B : A-version (Vendor specific)
--------------	-----------	---------	---

3.4.8 MR7_Basic Configuration 3 (MA<7:0> = 07_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	00000000 _B : A-version (Vendor specific)
--------------	-----------	---------	---