

JEDEC STANDARD

Wide I/O Single Data Rate (Wide I/O SDR)

JESD229

DECEMBER 2011

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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Published by

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WIDE I/O SINGLE DATA RATE (WIDE I/O SDR)

(From JEDEC Board Ballot JCB-11-79, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This standard defines the Wide I/O specification, including features, functionality, AC and DC characteristics, packages, and micropillar signal assignments. This standard covers the following technologies: Wide I/O. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant, 1 Gb through 32 Gb SDRAM (monolithic density) devices with 4, 128b wide channels using direct chip-to-chip attach methods between 1 to 4 memory devices and a controller device. This standard was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR2 (JESD209-2). Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the Wide I/O standard.

2 General Description

2.1 Terms and Definitions

Within the Wide I/O standard, these terms have particular meanings:

Stack: All memory chips in the memory system taken together in one assembly.

NOTE This Wide I/O standard supports memory stacks that include up to 4 memory chips.

Slice: One memory chip in the stack of memory chips.

Rank: That portion of memory from one memory die that is logically connected to a single channel within the memory stack.

Channel: Both a set of physically discrete connections within the Wide I/O interface and a logically discrete, independently controlled partition of the Wide I/O interface.

NOTE The Wide I/O interface supports 4 physical and 4 logical channels. Each physical channel contains all the control, data and clock signals necessary to independently control each of the 4 logical channels in the Wide I/O interface. Aside from a few global configuration options, each logical channel has its own set of mode registers, can have different DRAM pages open, can be independently clocked and can even be in different power states. The physical channel also contains power and ground signals but all power and ground signals on all physical channels must be at their appropriate levels for any portion of the Wide I/O device to operate correctly. The physical channel also contains a reset signal but the Wide I/O interface defines reset to be per slice rather than per channel.

2.2 Micropillar-out

2.2.1 Key Features

- 128 Data Bits per channel
- Support for up to 32 Gbit monolithic density
- micropillars allocated for differential CK/DQS for future DDR extension
- 5 Serial Scan connections/channel + 1 overall serial enable
- Per byte write masks
- 1 “must be routed through substrate” Direct Access micropillar per channel
- 2 missing row vertical channel spacing, 6 missing column horizontal channel spacing
- Power micropillar count supports current requirements of low-power memory space

2.2.2 Micropillar Definitions

Table 1 — Micropillar Definitions

Micropillar Type	Count	Description
VDD1	6	Core Power
VDD2	20	Core Power
VDDQ	16	I/O Power
VSS	24	Core Ground
VSSQ	16	I/O Ground
DQ	128	Data
DQS	16	Data Strobe DQS_t, DQS_c (unused in current definition)
DM	16	Data Mask
ADDR	19	Address (0-16), Bank (0-1)
CMD	4	RAS_n, CAS_n, WE_n, RESET
CK	2	CK_t, CK_c (unused in current definition)
CS	4	Chip (Rank) Select
CKE	4	Clock Enable
TEST	1/0	Memory DA Test Mode Enable (only on channel A, location is DA(o) on other channels)
SER	5	Serial Boundary Scan micropillars (uses CS to select rank)
KEY	1	Vendor Specific micropillar in channel A, n/c in channel B, Scan Enable in channel C, missing micropillar in channel D.
NC	9	no connect
DA	1	Direct Access (all SoC vendors will provide direct connection to memory through substrate)
DA(o)	8/9	Direct Access (optional, SoC vendors may or may not provide direct connections to memory through substrate)
Total	300	

NOTE 1 All views are the bottom views looking down upon the memory micropillars, i.e., with the memory micropillars facing out of the page. In the anticipated mounting orientation, this will be looking up from the board.

NOTE 2 There are 10 NC micropillars in channel B and 9 NC micropillars in channel A, C and D. The NC micropillar will be with micro bump and the missing micropillar will be without micropillar and microbump.

2.2.3 Left Side of Array Showing Two of Four Channels

			Channel A							
			1	2	3	4	5	6	7	8
			C1	C2	C3	C4	C5	C6	C7	C8
			0	50	100	150	200	250	300	350
M	CA	520	VSS	A0a	VDD2	DA(o)7a	VSS	CK_ta	VDD2	TESTa
L	CB	480	VSS	A1a	VDD2	NC	VSS	CK_ca	VDD2	SDOa
K	CC	440	VPIN	A2a	A9a	A10a	BA1a	RAS_na	CS0_na	CS3_na
J	CD	400	VDD1	A3a	A8a	A11a	BA0a	CAS_na	CS1_na	CS2_na
H	CE	360	VDD1	A4a	A7a	A12a	A15a	WE_na	CKE0a	CKE3a
G	CF	320	VDD1	A5a	A6a	A13a	A14a	A16a	CKE1a	CKE2a
			nb	nb	nb	nb	nb	nb	nb	nb
			nb	nb	nb	nb	nb	nb	nb	nb
F	CF	200	VDD1	A5d	A6d	A13d	A14d	A16d	CKE1d	CKE2d
E	CE	160	VDD1	A4d	A7d	A12d	A15d	WE_nd	CKE0d	CKE3d
D	CD	120	VDD1	A3d	A8d	A11d	BA0d	CAS_nd	CS1_nd	CS2_nd
C	CC	80	KEY	A2d	A9d	A10d	BA1d	RAS_nd	CS0_nd	CS3_nd
B	CB	40	VSS	A1d	VDD2	NC	VSS	CK_cd	VDD2	SDOd
A	CA	0	VSS	A0d	VDD2	DA(o)7d	VSS	CK_td	VDD2	DA(o)8d
			0	50	100	150	200	250	300	350
			C1	C2	C3	C4	C5	C6	C7	C8
			1	2	3	4	5	6	7	8
			Channel D							

Figure 1 — Left Side of Array Showing Two of Four Channels

2.2.4 Channel A Micropillar Locations

			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15
			0	50	100	150	200	250	300	350	400	450	500	550	600	650	700
M	CA	520	VSS	A0a	VDD2	DA(o)7a	VSS	CK_ta	VDD2	TESTa	VSS	VSS	DM0a	DA(o)6a	DM1a	VDD2	VDD2
L	CB	480	VSS	A1a	VDD2	NC	VSS	CK_ca	VDD2	SD0a	VSS	VSS	D06a	NC	D011a	VDD2	VDD2
K	CC	440	VPIN	A2a	A9a	A10a	BA1a	RAS_na	CS0_na	CS3_na	SC1a	DQ0a	VSSQ	DQ00_ca	VDDQ	DQ12a	DQ28a
J	CD	400	VDD1	A3a	A8a	A11a	BA0a	CAS_na	CS1_na	CS2_na	SD1a	DQ1a	VSSQ	DQ00_ta	VDDQ	DQ13a	DQ29a
H	CE	360	VDD1	A4a	A7a	A12a	A15a	WE_na	CKE0a	CKE3a	SSH_na	DQ2a	DQ6a	DQ7a	DQ10a	DQ14a	DQ30a
G	CF	320	VDD1	A5a	A6a	A13a	A14a	A16a	CKE1a	CKE2a	SOE_na	DQ3a	DQ4a	DQ8a	DQ9a	DQ15a	DQ31a
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
C16	C17	C18	C19	C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	C32	
750	800	850	900	950	1000	1050	1100	1150	1200	1250	1300	1350	1400	1450	1500	1550	
DM3a	DA(o)5a	DM2a	VSS	VSS	DM4a	DA(o)4a	DM5a	VDD2	VDD2	DM7	DA(o)3a	DM6a	VSS	VSS	DM8a	DA(o)2a	
DQ27a	NC	DQ22a	VSS	VSS	DQ38a	NC	DQ43a	VDD2	VDD2	DQ59a	NC	DQ64a	VSS	VSS	DQ70a	NC	
VDDQ	DQS1_ca	VSSQ	DQ16a	DQ32a	VSSQ	DQS2_ca	VDDQ	DQ44a	DQ60a	VDDQ	DQS3_ca	VSSQ	DQ48a	DQ64a	VSSQ	DQS4_ca	
VDDQ	DQS1_ta	VSSQ	DQ17a	DQ33a	VSSQ	DQS2_ta	VDDQ	DQ45a	DQ61a	VDDQ	DQS3_ta	VSSQ	DQ49a	DQ65a	VSSQ	DQS4_ta	
DQ26a	DQ23a	DQ21a	DQ18a	DQ34a	DQ37a	DQ39a	DQ42a	DQ46a	DQ62a	DQ68a	DQ65a	DQ63a	DQ65a	DQ63a	DQ65a	DQ68a	
DQ25a	DQ24a	DQ20a	DQ19a	DQ35a	DQ36a	DQ40a	DQ41a	DQ47a	DQ63a	DQ67a	DQ66a	DQ62a	DQ65a	DQ63a	DQ67a	DQ68a	
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
C33	C34	C35	C36	C37	C38	C39	C40	C41	C42	C43	C44	C45	C46	C47	C48	C49	C50
1600	1650	1700	1750	1800	1850	1900	1950	2000	2050	2100	2150	2200	2250	2300	2350	2400	2450
DM9a	VDD2	VDD2	DM11a	DA(o)1a	DM10a	VSS	VSS	DM12a	DA(o)0a	DM13a	VDD2	VDD2	DM15a	DAa	DM14a	VSS	VSS
DQ75a	VDD2	VDD2	DQ91a	NC	DQ86a	VSS	VSS	DQ102a	NC	DQ107a	VDD2	VDD2	DQ123a	NC	DQ118a	VSS	VSS
VDDQ	DQ76a	DQ92a	VDDQ	DQS5_c	VSSQ	DQ80a	DQ96a	VSSQ	DQS6_ca	VDDQ	DQ108a	DQ124a	VDDQ	DQS7_ca	VSSQ	DQ112a	VSS
VDDQ	DQ77a	DQ93a	VDDQ	DQS5_t	VSSQ	DQ81a	DQ97a	VSSQ	DQS6_ta	VDDQ	DQ109a	DQ125a	VDDQ	DQS7_ta	VSSQ	DQ113a	VSS
DQ74a	DQ78a	DQ94a	DQ90a	DQ87a	DQ85a	DQ82a	DQ98a	DQ101a	DQ103a	DQ106a	DQ110a	DQ126a	DQ112a	DQ119a	DQ117a	DQ114a	VDD
DQ73a	DQ79a	DQ95a	DQ89a	DQ88a	DQ84a	DQ83a	DQ99a	DQ100a	DQ104a	DQ105a	DQ111a	DQ127a	DQ121a	DQ120a	DQ116a	DQ115a	RST0

Figure 2 — Channel A Micropillar Locations

2.2.5 Center Area of 4-Channel Map

Channel A										Channel B									
14	45	46	47	48	49	50				51	52	53	54	55	56	57			
C45	C46	C47	C48	C49	C50					C50	C49	C48	C47	C46	C45	C44			
150	220	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950			
VD02	VD02	DM15a	D4a	DM14a	VSS	VSS	nb	nb	nb	VSS	VSS	DM14b	D4b	DM15b	VD02	VD02			
VD02	VD02	DQ123a	NC	DQ118a	VSS	VSS	nb	nb	nb	VSS	VSS	DQ118b	NC	DQ123b	VD02	VD02			
1108a	DQ124a	VDDQ	DCS7_a	VSSQ	DQ112a	VD01	nb	nb	nb	VD01	DQ112b	VSSQ	DCS7_b	VDDQ	DQ124b	DQ125a			
1109a	DQ125a	VDDQ	DCS7_b	VSSQ	DQ113a	VD01	nb	nb	nb	VD01	DQ113b	VSSQ	DCS7_b	VDDQ	DQ125b	DQ126a			
1110a	DQ126a	DQ122a	DQ119a	DQ117a	DQ114a	VD01	nb	nb	nb	VD01	DQ114b	DQ117b	DQ119b	DQ122b	DQ126b	DQ127a			
1111a	DQ127a	DQ121a	DQ120a	DQ116a	DQ115a	RST0_n	nb	nb	nb	RST1_n	DQ115b	DQ116b	DQ120b	DQ121b	DQ127b	DQ128a			
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb			
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb			
1111d	DQ127d	DQ121d	DQ120d	DQ116d	DQ115d	RST3_n	nb	nb	nb	RST2_n	DQ115c	DQ116c	DQ120c	DQ121c	DQ127c	DQ128c			
1110d	DQ126d	DQ122d	DQ119d	DQ117d	DQ114d	VD01	nb	nb	nb	VD01	DQ114c	DQ117c	DQ119c	DQ122c	DQ126c	DQ127c			
1109d	DQ125d	VDDQ	DCS7_b	VSSQ	DQ113d	VD01	nb	nb	nb	VD01	DQ113c	VSSQ	DCS7_b	VDDQ	DQ125c	DQ126c			
1108d	DQ124d	VDDQ	DCS7_a	VSSQ	DQ112d	VD01	nb	nb	nb	VD01	DQ112c	VSSQ	DCS7_a	VDDQ	DQ124c	DQ125c			
VD02	VD02	DQ123d	NC	DQ118d	VSS	VSS	nb	nb	nb	VSS	VSS	DQ118c	NC	DQ123c	VD02	VD02			
VD02	VD02	DM15d	D4d	DM14d	VSS	VSS	nb	nb	nb	VSS	VSS	DM14c	D4c	DM15c	VD02	VD02			
150	220	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950			
C45	C46	C47	C48	C49	C50					C50	C49	C48	C47	C46	C45	C44			
14	45	46	47	48	49	50				51	52	53	54	55	56	57			
Channel D										Channel C									

Figure 3 — Center Area of 4-Channel Map

Note the channel spacing and the micropillar assignments are reflections of Channel A.

The overall array size is (5.25mm + 1 micropillar diameter) x (0.52mm + 1 micropillar diameter).

The pitch (center to center) is 40 microns in the vertical dimension and 50 microns in the horizontal dimension.

2.3 Input/Output Functional Description

2.3.1 Micropillar Definition and Description

Note on nomenclature: unless otherwise designated, each channel is independent and implements independent sets of the designated micropillars. The channels are designated “a” to “d”. Additionally, unless otherwise designated, all signals are directly connected to all ranks (0 to 3) in the stack.

Table 2 — Micropillar Definition and Description

Name	Type	Description
CK_t[a:d]	Input	Clock: CK_t is a single-ended clock input. All Control, Address and Write Data (DQ) inputs are sampled on the positive edge of CK_t. The positive clock edge is defined by CK_t crossing 50% VDDQ.
CKE[0:3][a:d]	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. Each of CKE[0:3][a:d] address a single rank (0 to 3) on each of the channels (a to d).
CS[0:3]_n[a:d]	Input	Chip Select: CS_n is considered part of the command code. See Command Truth Table for command code descriptions. Each of CS[0:3]_n[a:d] address a single rank (0 to 3) on each of the channels (a to d).
RAS_n[a:d], CAS_n[a:d], WE_n[a:d]	Input	Command Inputs: Uni-directional command inputs. RAS_n, CAS_n and WE_n define the command being selected. See Command Truth Table for command code descriptions.
A[0:16][a:d]	Input	Address Inputs: Uni-directional address inputs. These provide the Row Address inputs for activate commands, the Column Address and Auto Precharge inputs for Read and Write commands, the Short Preamble inputs for Read commands, and the opcode for the Mode Register Set commands.
A10/AP[a:d]	Input	Autoprecharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (High: Autoprecharge, Low: No Autoprecharge)
A11/SP[a:d]	Input	Short Preamble: The controller indicate read with short preamble by driving A11 high when signalling a read command.
BA[0:1][a:d]	Input	Bank Inputs: Uni-directional bank select inputs. These provide the Bank Select inputs for activate, read, write and precharge commands.
RST[0:3]_n	Input	Reset Input: Uni-directional reset input. Each reset line resets all channels in a single slice. RST[0]_n appears on channel a and resets slice 0 (corresponding to CKE0/CS0_n) RST[1]_n appears on channel b and resets slice 1, RST[2]_n appears on channel c and resets slice 2, RST[3]_n appears on channel d and resets slice 3.
DQ[0:127] [a:d]	I/O	Data Inputs/Output: Bi-directional data bus
DQS[0:7]_t [a:d]	Output (possibly I/O in future)	Data Strobe: Data strobe (DQS_t) is output only in the current definition. Memories generate DQS_t such that a positive or a negative edge of DQS_t occurs in the middle of the read data eye with DQ providing a setup and a hold time to the DQS edge. Each DQS_t strobes two bytes of data. For timing purposes, the DQS edge is defined by DQS_t crossing 50% VDDQ. Note: write data is sampled on the positive edge of CK_t. In future extensions, DQS_t may be bidirectional.
DM[0:15][a:d]	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on the rising edge of CK_t coincident with the write data. Although DM is for input only, the DM loading shall match DQ, DQS_t and DQS_c. DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-DQ15, and so on, i.e., DM15 is the input data mask signal for data on DQ120-DQ127.
TEST	Input	Test: This input makes memory DA test mode enable. It may be routed through a controller I/O buffer before driving the memory I/O pad. Its function is defined by each individual memory vendor.
SDI[a:d], SCK[a:d], SOE_n[a:d], SSH_n[a:d]	Input	Boundary Scan Inputs: These inputs provide the necessary connections for the memory boundary scan functionality as defined in Section 5.

Name	Type	Description
SDO[a:d]	Output	Boundary Scan Outputs: This output provides the necessary connection for the memory boundary scan functionality as defined in Section 5.
DA[a:d]	Input/O utput	Direct Access Input/Output: This I/O is used by memory for direct access test functionality. It must be routed directly to an external package I/O pad. Its function is defined by each individual memory vendor.
DA(o)[0:7] [a:d] DA(o)8[b:d]	Input/O utput	Direct Access Input/Output: This I/O is used by memory for direct access test functionality. It may be routed through a controller I/O buffer before driving an external package I/O pad. Their functions are defined by each individual memory vendor.
KEY		This is a missing micropillar in the array used to indicate array orientation. It appears only in channel D.
VPIN	Input	This micropillar is used to select vendor specific features. It appears only in channel A.
SSEN	Input	This micropillar is used to set the entire DRAM to boundary scan mode (high) or normal operation mode (low). It appears only on channel C.
CK_c[a:d]		This is the compliment of CK_t. It is not currently used by the Wide I/O standard. It is included only for future extension.
DQS[0:7]_c [a:d]		These are the compliments of DQS_t. They are not currently used by the Wide I/O standard. They are included only for future extension.
NC		No connect pads.
V _{DD1}	Supply	Core Power Supply 1: Core power supply.
V _{DD2}	Supply	Core Power Supply 2: Core and input buffer power supply.
V _{DDQ}	Supply	I/O Power Supply: Power supply for Data input/output buffers.
V _{SS}	Supply	Ground
V _{SSQ}	Supply	I/O Ground

2.4 Addressing

Wide I/O has 4 channels and total x512 bit I/Os. Each channel has 4 Banks and x128 bit I/Os.

Table 3 — Wide I/O Addressing

Device Density	Density / Channel	Address		
		BA	Row	Column
1Gb	256Mb	BA0 - BA1	RA0 - RA11	CA0 - CA6
2Gb	512Mb	BA0 - BA1	RA0 - RA12	CA0 - CA6
4Gb	1Gb	BA0 - BA1	RA0 - RA13	CA0 - CA6
8Gb	2Gb	BA0 - BA1	RA0 - RA14	CA0 - CA6
16Gb	4Gb	BA0 - BA1	RA0 - RA14	CA0 - CA7
32Gb	8Gb	TBD	TBD	TBD

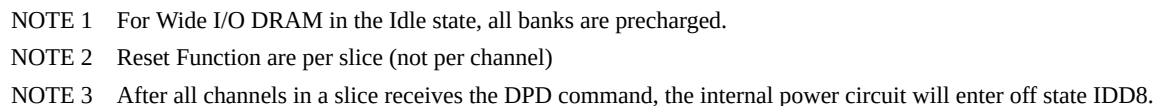
3 Functional Description

3.1 Wide I/O State Diagram

Wide I/O DRAM device state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. Unless otherwise specified, the state diagram describes the state and commands for only one channel in a slice.

For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restriction when considering the actual state of the banks.



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3.2 Power up, Initialization and Power Off Sequence

3.2.1 Power-up, Initialization, and Power-Off

Wide I/O DRAM Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence shall be used to power up the Wide I/O DRAM device. Unless specified otherwise, these steps are mandatory.

3.2.2 Power-up and Initialization Sequence

1. Power Ramp: While applying power, RST_n is recommended to be maintained below $0.2 \times VDD2$; all other inputs shall be between VIL_{min} and VIH_{max} . The following conditions apply:
 - T_a is the point where any power supply first reaches 300 mV.
 - T_b is the point when all supply voltages are within their respective min/max operating conditions.
 - After T_a is reached, $VDD1$ must be greater than $VDD2 - 200$ mV.
 - After T_a is reached, $VDD1$ and $VDD2$ must be greater than $VDDQ - 200$ mV.
 - The voltage difference between VSS and $VSSQ$ micropillars may not exceed 100 mV.
 - The above conditions apply between T_a and power-off (controlled or uncontrolled).
 - Power ramp duration t_{INIT0} ($T_b - T_a$) must be no greater than 20 ms and power ramp slope must be monotonic during t_{INIT0} .
 - The Wide I/O DRAM device will guarantee that outputs are in a high impedance state while RST_n is held low.
2. RST_n: RST_n must be maintained for a minimum 200 us with stable power. CKE must be pulled “Low” a minimum of 10ns before RST_n is de-asserted.
3. CKE and Clock: After RST_n is de-asserted, CKE must remain deasserted for 500 us. During this time, the DRAM will initialize internal state independent of external clocks.

The clock must be started and stable for at least 5 clocks before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must also be met. Also, a NOP or Deselect command must be registered (with t_{IS} set up time to clock) the clock before CKE goes active. After CKE is registered high, t_{INIT5} must pass before issuing the MRS command to load a mode register.
4. Mode Register: Issue MRS Command(s) to load mode registers with all application settings.
5. Normal Operation: The Wide I/O DRAM device is now ready for normal operation.

Table 4 — Timing Parameters for initialization

Symbol	Value		Unit	Comment
	Min	Max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	200		us	Minimum RST_n low Time with stable power
t_{INIT2}	10		ns	Minimum CKE low Time before RST_n high
t_{INIT3}	500		us	Minimum CKE low Time after RST_n high
t_{INIT4}	5		tCK	Minimum stable clock before first CKE high
t_{INIT5}	200		us	Minimum idle time after first CKE assertion

3.2.2 Power-up and Initialization Sequence (cont'd)

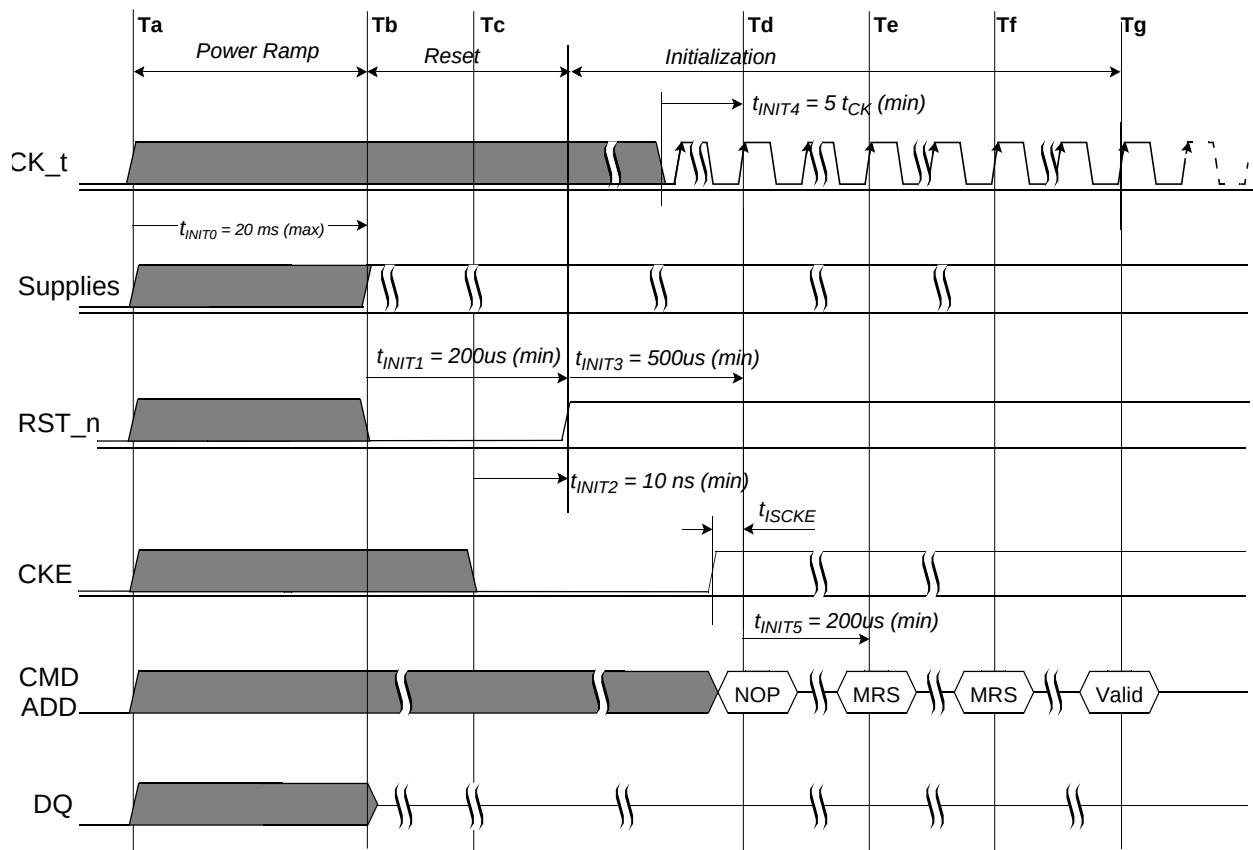


Figure 5 — Power Ramp and Initialization Sequence

3.2.3 Reset Initialization with Stable Power

The following sequence is required for RESET with no power interruption initialization.

1. Assert RST_n (active low) anytime when reset is needed. All other inputs may be undefined.
RST_n must be maintained for at least 100 ns. CKE must be pulled “LOW” 10ns before RST_n is deasserted.
2. Follow the Power-up and Initialization Sequence steps 3 and 4.
3. The Reset sequence is now completed; The Wide I/O DRAM device is ready for normal operation.

3.2.3 Reset Initialization with Stable Power (cont'd)

Table 5 — Timing Parameters for Reset Initialization with stable Power

Symbol	Value		Unit	Comment
	min	max		
t_{INIT1}	100		ns	Minimum RST_n low Time for Reset Initialization with stable power
t_{INIT2}	10		ns	Minimum CKE low Time before RST_n high
t_{INIT3}	500		us	Minimum CKE low Time after RST_n high
t_{INIT4}	5		tCK	Minimum stable clock before first CKE high
t_{INIT5}	200		us	Minimum idle time after first CKE assertion

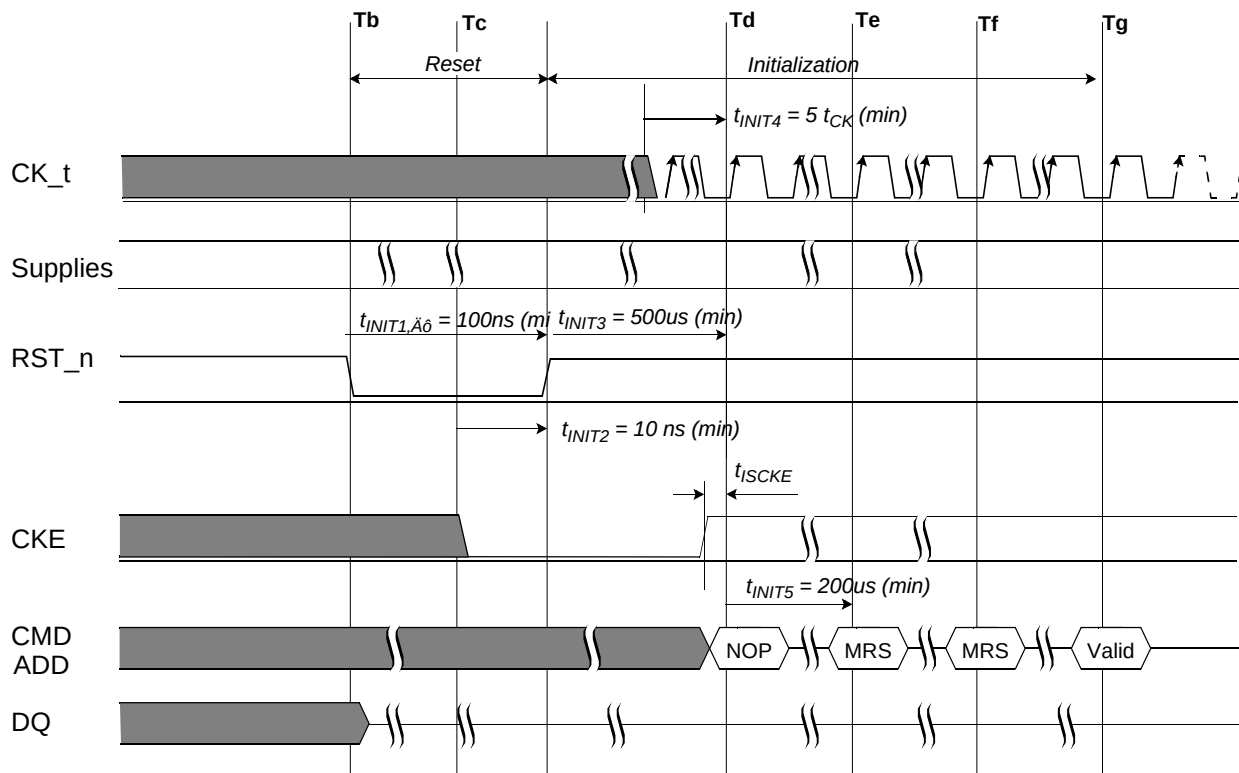


Figure 6 — Reset Initialization with stable Power

3.2.4 Power-off Sequence

The following sequence shall be used to power off the Wide I/O DRAM device. Unless specified otherwise, these steps are mandatory.

If system requires DQ remain Hi-Z while removing power, RST_n shall be held at a logic low level ($= < 0.2 \times VDD2$) or CKE shall be held in logic low level. All other inputs shall be between VILmin and VIHmax. The Wide I/O DRAM device will guarantee that outputs are in a high impedance state while RST_n is held low.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

The voltage difference between VSS and VSSQ micropillars may not exceed 100 mV.

Table 6 — Power-off Sequence

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

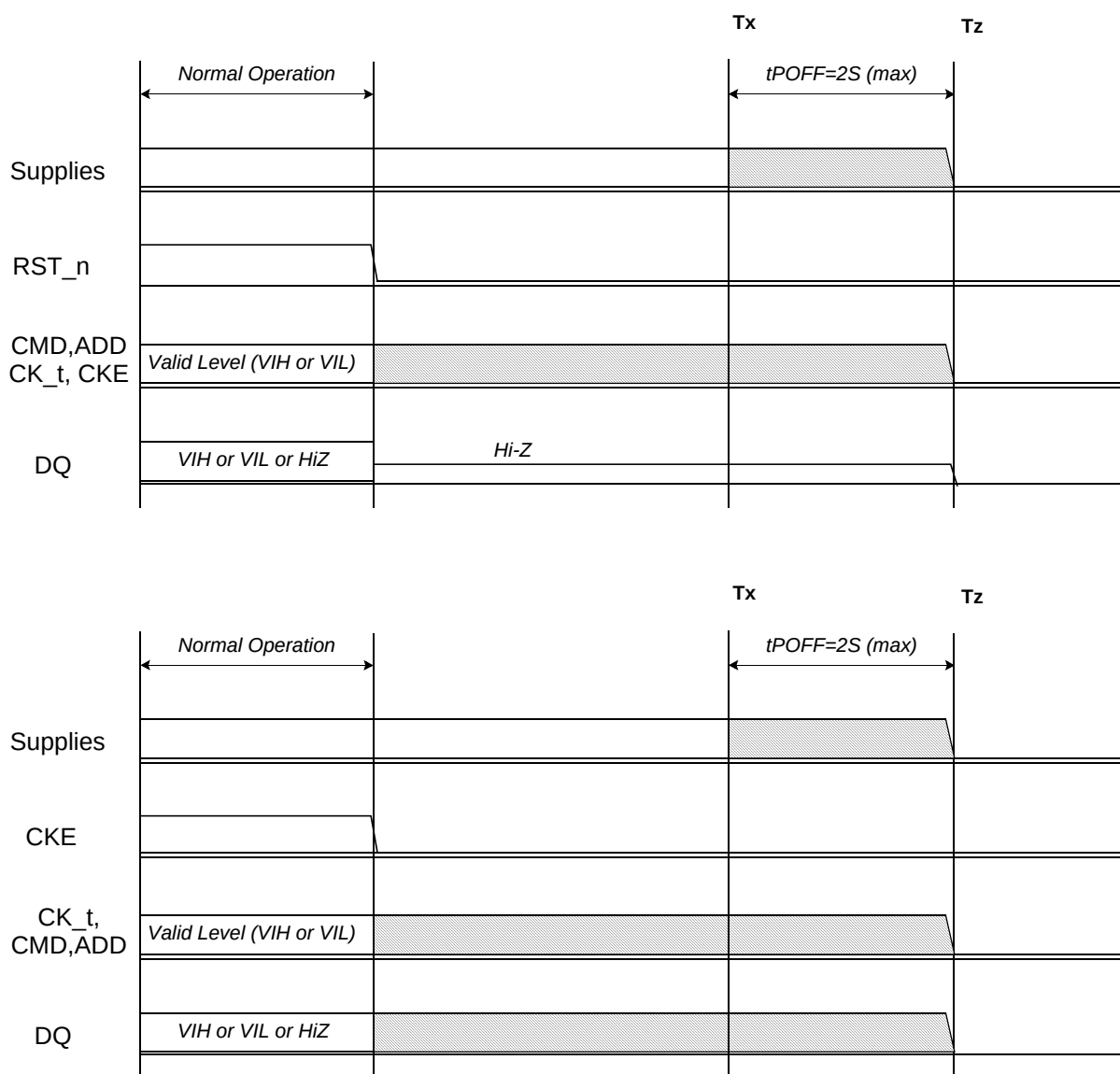


Figure 7 — Power-Off Sequence

3.2.5 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the Wide I/O device under uncontrolled condition. Unless specified otherwise, these steps are mandatory.

T_x is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

T_z is the point where all power supplies first reaches 300 mV. After T_z, the device is powered off.

The time between T_x and T_z (tPOFF) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between T_x and T_z.

The uncontrolled power off sequence can be applied only up to 400 times in the life of the device

3.3 Mode Register Definition

3.3.1 Register Definition

For application flexibility, various functions, features, and modes are programmable in Wide I/O DRAM Mode Registers. Values are programmed into Mode Registers via a Mode Register Set (MRS) command. The default values of the Mode Registers (MR#) are not defined so they must be programmed during the reset and initialization sequence. The Mode Registers are defined for one channel.

The contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register will be redefined when the MRS command is issued.

MRS commands do not affect array contents regardless of when these commands are executed.

After the mode register set command, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

The mode registers are divided into various fields depending on the functionality and/or modes.

Table 7 — Mode Register Definition

	A16	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0					Write Latency			TM	Read Latency			0	Burst Length		
MR1	0	0	1	Currently only one register is defined at A[15:0] = 0, DQ0-20 is used for SRR.															
MR2	0	1	0	0						nWR		TM	Drive Strength		0			Thermal Offset	
MR3	0	1	1	PASR															
MR4	1	0	0	Reserved for future use															
MR5	1	0	1	0								DQ/DQS Tuning							
MR6	1	1	0	Reserved for future use															
MR7	1	1	1	PASR															

3.3.2 Mode Register MR0

Mode register MR0 stores the data for controlling various operating modes of Wide I/O DRAM. It controls Burst Length, Read latency, and Write Latency.

A16	BA1	BA0	A15 - A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	Write Latency			TM	Read Latency			0	Burst Length		

A7	Mode
0	Normal
1	Test

A2	A1	A0	Burst length
0	0	0	Reserved
0	0	1	2
0	1	0	4
Others			Reserved

A10	A9	A8	Write Latency
0	0	1	WL=1
0	1	0	WL=2(Optional)
Others			Reserved

A6	A5	A4	Read Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	RL=2
0	1	1	RL=3
1	0	0	RL=4(Optional)
Others			Reserved

Figure 8 — Mode register MR0 definition

3.3.2.1 Burst Length

Read and write accesses to the Wide I/O DRAM are burst oriented, with the burst length being set as in Figure8 with the burst order as in Table 8.

The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2 or 4 locations are available for the sequential burst types.

Table 8 — Burst Length

Burst Length	Starting Column address		Order of accesses within a burst (Hexadecimal notation)
	A1	A0	Sequential
2		0	0-1
		1	1-0
4	0	0	0-1-2-3
	0	1	1-2-3-0
	1	0	2-3-0-1
	1	1	3-0-1-2

NOTE 1 For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.

NOTE 2 For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.

NOTE 3 Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to four

NOTE 4 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

3.3.2.2 Read Latency

The READ latency is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tAC delay for the first piece of output data is measured.

If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at $n + 3t_{CK} + t_{AC}$. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at $n + 2t_{CK} + t_{AC}$.

3.3.2.3 Write Latency

The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock where the first piece of input data is written.

If a WRITE command is registered at a clock edge n and the latency is 1 clock, the first data element will appear on the data bus at $n + t_{CK}$.

3.3.3 Mode Register MR1

The mode register MR1 is for SRR uses.

DQ127-DQ21	DQ20	DQ19	DQ18	DQ17	DQ16	DQ15	DQ14	DQ13	DQ12	DQ11-DQ10	DQ9	DQ8	DQ7-DQ4	DQ3	DQ2	DQ1	DQ0
Reserved	Temp. sensor location			Delay Step		Die Density			DT	Reserved	Refresh Interval		Reserved	Manufacturer ID			

DQ15	DQ14	DQ13	Die Density
0	0	0	1Gb
0	0	1	2Gb
0	1	0	4Gb
0	1	1	8Gb
1	0	0	16Gb
1	0	1	32Gb
1	1	0	Rsrv.
1	1	1	Rsrv.

DQ12	Device Type
0	Wide I/O SDR
1	Rsrv.

DQ9	DQ8	Refresh Interval
0	0	tREFI
0	1	0.50 x tREFI
1	0	0.25 x tREFI
1	1	High Temp. limit exceeded

DQ3	DQ2	DQ1	DQ0	Manufacturer's ID
0	0	0	0	Rsrv.
0	0	0	1	Samsung
0	0	1	0	Rsrv.
0	0	1	1	Elpida
0	1	0	0	Etron
0	1	0	1	Nanya
0	1	1	0	Hynix
0	1	1	1	Rsrv.
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	Rsrv.
1	0	1	1	Rsrv.
1	1	0	0	Rsrv.
1	1	0	1	Rsrv.
1	1	1	0	Rsrv.
1	1	1	1	Micron

DQ20	DQ19	DQ18	Temp. Sensor Location
0	0	0	Makes it reserved for Temp sensor location within a slice
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

DQ17	DQ16	Delay Step
0	0	No step
0	1	8 step
1	0	16 step
1	1	32 step

Figure 9 — Mode register MR1 definition

3.3.3.1 Status Register Read

SRR provides a method to read registers from the Wide I/O DRAM. The encoding for an SRR command is the same as a MRS with (A16, BA[1:0]) = "001", MR1, status register. The address micropillars (A[15:0]) encode which register is to

be read. Currently only one register is defined at A[15:0] = 0. Refer to Table 1 for the definition of this register. The sequence to perform an SRR command is as follows:

all reads/writes must be completed

all banks must be closed

issue MRS with (A16, BA[1:0]) = 001 (SRR)

wait tSRR

issue read to any bank with A[15:0] = 0

Read latency cycles later the Wide I/O DRAM returns the status register data as it would a normal read

tSRC after the Read command, the Wide I/O DRAM will return to Idle (all banks precharged) state.

Refer to Figure 10 for Status register read sequence.

The burst length for the SRR read is always fixed to length 2.

The 1st bit of data and the 2nd bit of data on each DQ are the same. (DQn=DQn+1)

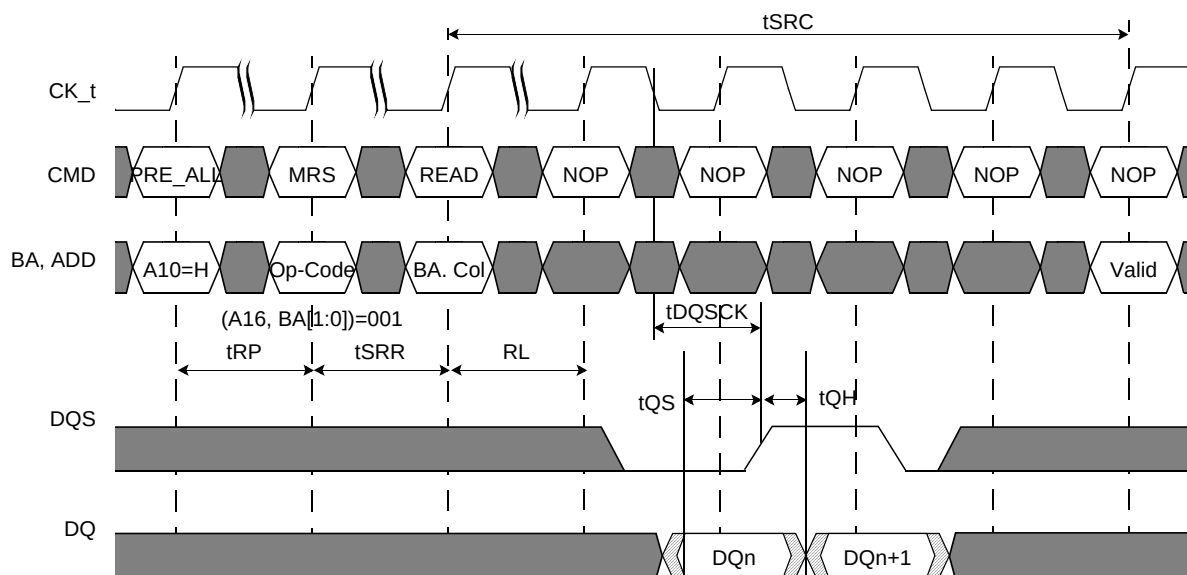


Figure 10 — Status Register Read Timing Diagram

NOTE1 SRR can only be issued after power-up and initialization sequence is complete;

NOTE2 SRR can only be issued with all banks precharged;

NOTE3 SRR RL is unchanged from value in the mode register;

NOTE4 SRR BL is fixed at 2. DQn and DQn+1 values are the same.

3.3.4 Mode Register MR2

Mode register MR2 stores the data for controlling various operating modes of Wide I/O DRAM. It controls Thermal Offset, Drive Strength, TM and nWR.

A16	BA1	BA0	A15 -A10	A9	A8	A7	A6	A5	A4 - A1	A0
0	1	0	0	nWR		TM	Drive Strength		0	Thermal Offset

A7	Mode	A0	Thermal Offset
0	Normal	0	<5
1	Test	1	5-15

A9	A8	nWR
0	0	Reserved (2)
0	1	nWR=3
1	0	Reserved (4)
1	1	Reserved

A6	A5	Drive strength
0	0	Full
0	1	Weak
1	0	Reserved
1	1	Reserved

Figure 11 — Mode Register MR2 definition

3.3.4.1 Thermal Offset

Because of their tight thermal coupling with Wide I/O DRAMs, hot spots on Wide I/O controllers can induce thermal gradients into the DRAMs. As these hot spots may not be located near the DRAM thermal sensor, the DRAM's temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through Mode Register 2 (A16=0, BA1=1, BA0=0) in channel A and it will not be affected through MR2(A0) in channel B, C or D. This temperature offset will modify refresh behavior for all channels in the slice. If the induced thermal gradient from temperature sensor location for DRAM to hot spot location of controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents. Bit 1 (A1) in MR2 is reserved for future thermal offset use.

During normal operation, the controller will update this register whenever it detects changes in the induced thermal gradient. Since updating this register may modify the self-refresh behavior for all channels, all channels must not be in self-refresh mode when this register is written in channel A.

If changes to the thermal offset indicate that the self refresh frequency increases (that is, the time between refreshes decreases), the memory must reflect these changes immediately. If changes to the thermal offset indicate that the self refresh frequency decreases (that is, the time between refreshes increases), the controller cannot put the memory into self refresh until the controller has refreshed all memory on the device.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor must be located in a predictable location. To provide maximum flexibility, several locations on the memory die are supported. The supported locations are TBD. The specific location used by an individual memory die is indicated by 3 bits in the memory status register. All memory dice in a stack must use the same thermal X-Y location.

To ensure that the memory thermal sensor is located above an X-Y location on the controller, the memory thermal sensor must be located within a rectangle centered on the memory-controller physical interface. Additionally, the minimum size of a controller that wants to use this feature is within that rectangle as otherwise the memory's thermal sensor could be located outside the controller die's perimeter.

3.3.4.2 Drive Strength

Drive strength can be set to full or weak strength via address bits A5 and A6.

Full strength supports 3pF channel load and weak strength supports 2pF channel load to achieve minimum slew rates of 1V/ns.

3.3.4.3 nWR

This is used to program internal auto precharge start timing for Write with auto precharge command.

$$nWR \geq RU(tWR/tCK)$$

3.3.5 Mode Register MR3

The mode register MR3 is used for partial array self refresh.

Table 9 — Mode Register MR3 definition

A16	BA1	BA0	A15 -A0
0	1	1	PASR

Table 10 — Bank/Segment mask definition for PASR

Monolithic die density				1Gb	2Gb	4Gb		8Gb		16Gb		32Gb
MR#	MR bit	PASR Mask Area	BA1:0	BA1:0	BA1:0	RA13	BA1:0	RA14:13	BA1:0	RA14:12		
MR3	A0	Bank0	Segment0	00B	00B	00B	0B	00B	00B	00B	000B	TBD
	A1	Bank1		01B	01B	01B	0B	01B	00B	01B	000B	
	A2	Bank2		10B	10B	10B	0B	10B	00B	10B	000B	
	A3	Bank3		11B	11B	11B	0B	11B	00B	11B	000B	
	A4	Bank0	Segment1	-	-	00B	1B	00B	01B	00B	001B	
	A5	Bank1		-	-	01B	1B	01B	01B	01B	001B	
	A6	Bank2		-	-	10B	1B	10B	01B	10B	001B	
	A7	Bank3		-	-	11B	1B	11B	01B	11B	001B	
	A8	Bank0	Segment2	-	-	-	-	00B	10B	00B	010B	
	A9	Bank1		-	-	-	-	01B	10B	01B	010B	
	A10	Bank2		-	-	-	-	10B	10B	10B	010B	
	A11	Bank3		-	-	-	-	11B	10B	11B	010B	
	A12	Bank0	Segment3	-	-	-	-	00B	11B	00B	011B	
	A13	Bank1		-	-	-	-	01B	11B	01B	011B	
	A14	Bank2		-	-	-	-	10B	11B	10B	011B	
	A15	Bank3		-	-	-	-	11B	11B	11B	011B	

3.3.5.1 Partial Array Self Refresh (PASR)

With Partial Array Self Refresh (PASR), the self refresh may be restricted to a variable portion of the total array. The PASR detail scheme will be defined. Data outside the defined area will be lost. Address bits A0 to A15 are used to set PASR. When the bit is programmed 0, refresh operation to the corresponding area will not be blocked (not masked) and will be refreshed.

3.3.6 Mode Register MR5

3.3.6.1 Rank-to-Rank DQ/DQS Tuning

Wide I/O DRAMs must provide rank-to-rank timing accuracy to within 500ps between ranks across PVT. To enable this, Wide I/O DRAMs insert variable delays into their DQ and DQS generation circuits. In addition, Wide I/O controllers have phase discrimination circuits that can determine, within 100ps, the relative arrival times of two pulses on different DQ lines.

DRAM delay step size is not specified. The DRAM design should set the maximum step size to ensure that once alignment has been achieved, the ranks will stay aligned within 500ps across all subsequent operating conditions, i.e., as voltage and temperature within the DRAM stack changes. To achieve this, the DRAM may specify conditions that will require subsequent retuning. The DRAM design should set the minimum step size and step count to ensure that enough delay can be inserted into the fastest devices to align their DQ and DQS timing with the slowest devices.

Different delays can be inserted into the DQ generation circuits and the DQS generation circuits as DQ delays are from the rising edge of CK while DQS delays are from the falling edge of CK. This can be used to account for different sampling points for the rising and falling edges for CK in the memory devices to ensure DQS edges are more closely centered within the data eye.

Within a rank, the inserted DQ delay is the same for all DQ outputs. Within a rank, the inserted DQS delay is the same for all DQS outputs. Within a slice, each channel has independent delay elements and controls.

During initialization, the Wide I/O controller tells each rank in the memory system to place continuous CK/2 pulses on different DQ and DQS signals. The controller then tells each memory rank to insert delays into the DQ/DQS circuits until all channels' pulses align within the accuracy of the controller's phase discriminator.

DRAM vendors have the option of performing this tuning at the time of memory manufacture. If this is done, then tuning is not required at system initialization and the memory need not provide dynamic tuning functionality.

This functionality is required for all 2-, 3- and 4-slice configurations but is optional in 1-slice configurations.

Because this functionality adds delay to memory response, the tAC and tDQSCK parameters are specified with zero delay added.

The number of delay steps supported by the memory is in DQ17:16 of the status register:

Table 11 — Delay Steps

DQ17	DQ16	
0	0	no steps (factory tuning)
0	1	8 steps
1	0	16 steps
1	1	32 steps

Control of tuning is through Mode Register 5 (A16=1, BA1=0, BA0=1). Delay insertion for the DQ delay from the positive going edge of CK is shown in the following table:

Table 12 — DQ delay Insertion

A16	BA1	BA0	A1	A0	
1	0	1	0	0	Do not change delay
1	0	1	0	1	Increase +CK to DQ delay 1 element
1	0	1	1	0	Decrease +CK to DQ delay 1 element
1	0	1	1	1	Remove all +CK to DQ delay

