

JEDEC STANDARD

NAND Flash Interface Interoperability

JESD230C

(Revision of JESD230B, July 2014)

OCTOBER 2016

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2016
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

NAND FLASH INTERFACE INTEROPERABILITY

(From JEDEC Board Ballot JCB-16-34, formulated under the cognizance of the JC-42.4 Subcommittee on Nonvolatile Memory Devices.)

1 Scope

This standard was jointly developed by JEDEC and the Open NAND Flash Interface Workgroup, hereafter referred to as ONFI. This standard defines a standard NAND flash device interface interoperability standard that provides means for system be designed that can support Asynchronous SDR, Synchronous DDR and Toggle DDR NAND flash devices that are interoperable between JEDEC and ONFI member implementations.

2 Terms, definitions, abbreviations and conventions

2.1 Terms and definitions

address: A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172 and JESD88.)

NOTE 1 In a nonvolatile memory array, the address consists of characters, typically hexadecimal, to identify the row and column location of the memory cell(s).

NOTE 2 For NAND nonvolatile memory devices, the row address is for a page, block, or logical unit number (LUN); the column address is for the byte or word within a page.

NOTE 3 The least significant bit of the column address is zero for the source synchronous data interface.

asynchronous: Describing operation in which the timing is not controlled by a clock.

NOTE For a NAND nonvolatile memory, asynchronous also means that data is latched with the WE_n signal for the write operation and the RE_n signal for the read operation.

block: A continuous range of memory addresses. (Ref. IEC 748-2 and JESD88.)

NOTE 1 The number of addresses included in the range is frequently equal to 2^n , where n is the number of bits in the address.

NOTE 2 For nonvolatile memories, a block consists of multiple pages and is the smallest addressable memory segment within a memory device for the erase operation.

column: In a nonvolatile memory array, a series of memory cells whose sources and/or drains are connected via a bit line.

NOTE 1 Depending on the nonvolatile memory array, the bit line is accessed via the column select transistor, the column address decoder, or other decoding scheme.

NOTE 2 In nonvolatile memory device, a column decoder accesses a bit (x1), byte (x8), word (x16), or Dword (x32) either individually or within a page.

NOTE 3 In a typical schematic of a memory array, the column is in the vertical direction.

2.1 Terms and definitions (cont'd)

Dword (x32): A sequence of 32 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 31; the most significant bit is shown on the left. When shown as words, the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes, the least significant byte is byte 0 and the most significant byte is byte 3.

NOTE 2 See Figure 1 for a description of the relationship between bytes, words, and Dwords.

latching edge: The rising or falling edge of a waveform that initiates a latch operation.

NOTE 1 For a NAND nonvolatile memory the latching edge is the edge of the CK or DQS signal on which the contents of the data bus are latched for the source synchronous data interface.

NOTE 2 For a NAND nonvolatile data cycles, the latching edge is both the rising and falling edges of the DQS signal.

NOTE 3 For a NAND nonvolatile command and address cycles, the latching edge for the source synchronous interface is the rising edge of the CK signal.

NAND defect area: A designated location within the NAND memory where factory defects are identified by the manufacturer.

NOTE 1 The location is a portion of either the first page and/or the last page of the factory-marked defect block, this defect area in each page is defined as (# of data bytes) to (# of data bytes + # of spare bytes -1).

NOTE 2 For an 8-bit data access NAND memory device, the manufacturer sets the first byte in the defect area of the first or last page of the defect block to a value of 00h.

NOTE 3 For a 16-bit data access NAND memory device, the manufacturer sets the first word in the defect area of the first or last page of the defect block to a value of 0000h.

NAND nonvolatile memory device: The packaged NAND nonvolatile memory unit containing one or more NAND targets.

NOTE This is referred to as "device" in this standard.

NAND row address: An address referencing the LUN, block, and page to be accessed.

NOTE 1 The page address uses the least significant row address bits.

NOTE 2 The block address uses the middle row address bits.

NOTE 3 The LUN address uses the most significant row address bits.

page: The smallest nonvolatile memory array segment, within a device, that can be addressed for read or program operations.

page register: A register used to transfer data from a page in the memory array for a read operation or to transfer data to a page in the memory array for a program operation.

read request (for a nonvolatile memory): A data output cycle request from the host that results in a data transfer from the device to the host.

source synchronous (for a nonvolatile memory): Describing an operation in which the strobe signal (DQS) is transmitted with the data to indicate when the data should be latched.

NOTE The strobe signal (DQS) is similar in concept to an additional data bus bit.

2.1 Terms and definitions (cont'd)

status register (SR[x]): A register within a particular LUN containing status information about that LUN.

NOTE SR[x] refers to bit "x" within the status register.

target: A nonvolatile memory component with a unique chip enable (CE_n) select pin.

word (x16): A sequence of 16 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A word may be represented as 16 bits or as two adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 15; the most significant bit is shown on the left. When shown as bytes, the least significant byte (lower) is byte 0 and the most significant byte is byte 2.

NOTE 2 See Figure 1 for a description of the relationship between bytes, words, and Dwords.

2.2 Abbreviations

DDR: Abbreviation for "double data rate".

LUN (logical unit number): The minimum memory array size that can independently execute commands and report status.

N/A: Abbreviation for "not applicable". Fields marked as "na" are not used.

O/M: Abbreviation for Optional/Mandatory requirement. When the entry is set to "M", the item is mandatory. When the entry is set to "O", the item is optional.

2.3 Conventions

2.3.1 Active-low signals

While the preferred method for indicating a signal that is active when low is to use the over-bar as in $\overline{CE}$, the difficulty in producing this format has resulted in several alternatives meant to be equivalents. These are the use of a CE reverse solidus (\) or the trailing underscore (_) following the signal name as in CE\ and CE_. In this publication "_n" is used to indicate an active low signal (i.e., an inverted logic sense).

2.3.2 Signal names

The names of abbreviations, initials, and acronyms used as signal names are in all uppercase (e.g., CE_n). Fields containing only one bit are usually referred to as the "name bit" instead of the "name field". Numerical fields are unsigned unless otherwise indicated.

2.3.3 Precedence in case of conflict

If there is a conflict between text, figures, state machines, timing diagrams, and/or tables, the precedence shall be state machine, timing diagrams, tables, figures, and text.

2.4 Keywords

Several keywords are used to differentiate between different levels of requirements or suggestions.

mandatory: A keyword indicating items to be implemented as defined by a standard. Users are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the standard.

may: A keyword that indicates flexibility of choice between stated alternatives or possibly nothing with no implied preference.

optional: A keyword that describes features that are not required by the specification. However, if any optional feature defined by the specification is implemented, that feature shall be implemented in the way defined by the specification.

reserved: A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field may be cleared to zero or in accordance with a future extension to this publication. A host should not read/use reserved information.

shall: A keyword indicating a mandatory requirement.

should: A keyword indicating flexibility of choice with a strongly preferred alternative. This is equivalent to the phrase "it is recommended".

2.5 Byte, Word and Dword Relationships

Figure 1 illustrates the relationship between bytes, words and Dwords

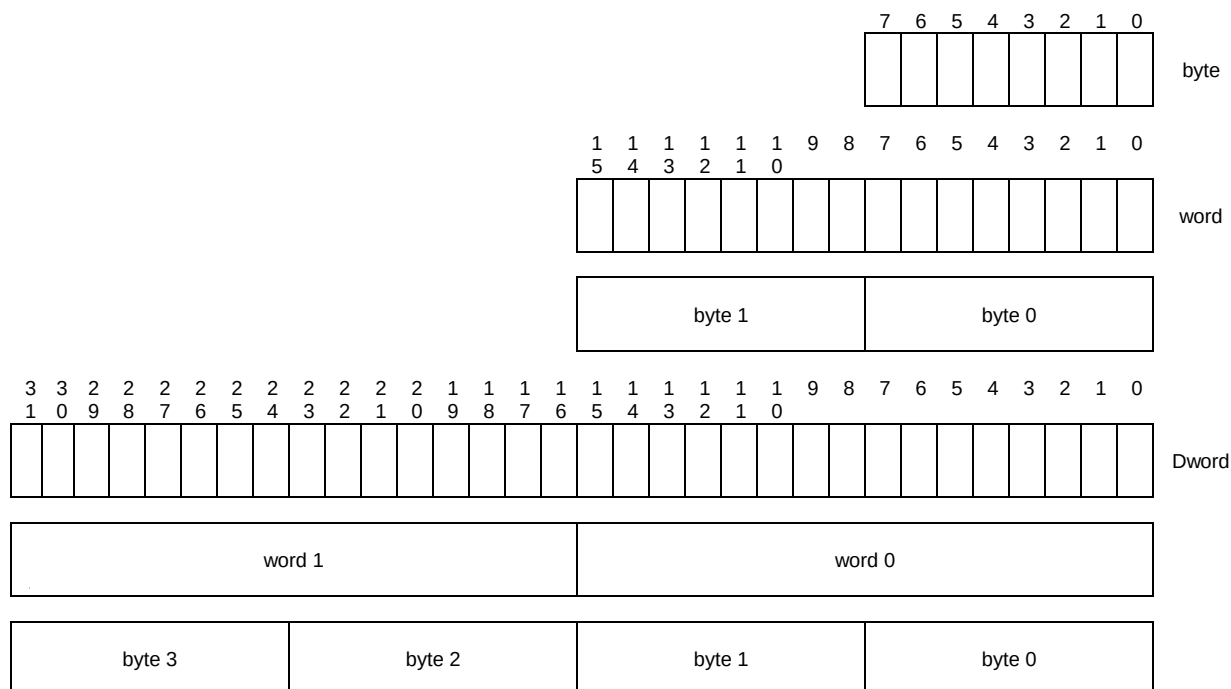


Figure 1 — Byte, word and Dword relationships

2.6 Pin description

Table 1 — Pin description

Name	Input/ Output	Description
IO0 ~ IO7(~ IO15) DQ0 ~ DQ7 DQ0_x ~ DQ7_x	I/O	DATA INPUTS/OUTPUTS These signals are used to input command, address and data, and to output data during read operations. The signals float to high-z when the chip is deselected or when the outputs are disabled. IO0 ~ IO15 are used in a 16-bit wide target configuration. With multi channel support, IO0_0~IO7_0 and IO0_1~IO7_1 are used for IOs of channel 0 and IOs of channel 1 respectively. Also known as DQ0~DQ7 for Toggle DDR and Synchronous DDR. The number after the underscore represents the channel. For example, DQ0_0 indicates DQ0 of channel-0 and DQ0_1 does DQ0 of channel-1.
CLE_x	I	COMMAND LATCH ENABLE The CLE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
ALE_x	I	ADDRESS LATCH ENABLE The ALE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
CEX_x_n	I	CHIP ENABLE The CEX_x_n input is the target selection control. When CEX_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CEX_x_n is low, the target is selected.
WE_x_n	I	WRITE ENABLE The WE_x_n input controls writes to the I/O port. For Asynchronous SDR Data, commands, addresses are latched on the rising edge of the WE_x_n pulse. For Toggle DDR commands, addresses are latched on the rising edge of the WE_x_n pulse.
R/B_x_n	O	READY/BUSY OUTPUT The R/B_x_n output indicates the status of the target operation. When low, it indicates that one or more operations are in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
RE_x_n (RE_x_t)	I	READ ENABLE The RE_x_n input is the serial data-out control. For Asynchronous SDR Data is valid tREA after the falling edge and for Toggle DDR Data is valid after the falling edge & rising edge of RE_x_n which also increments the internal column address counter by each one.
RE_x_c	I	Complement of Read Enable This is the complementary signal to Read Enable
DQS_x (DQS_x_t)	I/O	Data Strobe The data strobe signal that indicates the data valid window for Toggle DDR and Synchronous DDR data interface. Output with read data, input with write data. Edge-aligned with read data, centered in write data.
DQS_x_c	I/O	Complement of Data Strobe This is the complementary signal to Data Strobe.
W/R_x	I	Write/Read Direction The Write/Read Direction signal indicates the owner of the DQ bus and DQS signal in the Synchronous DDR data interface. This signal shares the same pin as RE_x_n in the asynchronous data interface.

2.6 Pin description (cont'd)

Table 1 — Pin description (cont'd)

Name	Input/ Output	Description
CK_x	I	Clock The Clock signal is used as the clock in Synchronous DDR data interface. This signal shares the same pin as WE_x_n in the asynchronous data interface.
WP_x_n	I	WRITE PROTECT The WP_x_n disables the Flash array program and erase operations.
Vcc	I	POWER VCC is the power supply for device.
VccQ	I	I/O POWER The VccQ is the power supply for input and/or output signals.
Vss	I	GROUND The Vss signal is the power supply ground.
VssQ	I	I/O GROUND The VssQ signal is the ground for input and/or output signals
VSPx	n/a	Vendor Specific The function of these signals is defined and specified by the NAND vendor. Any VSP signal not used by the NAND vendor shall not be connected internal to the device.
VREFQ	n/a	Reference voltage This is used as an external voltage reference.
RZQ_x	Supply	Reference pin for ZQ calibration This is used on ZQ calibration and RZQ ball shall be connected to Vss through 300ohm resistor
ENi / ENo	I/O	Enumeration pins These pins may be used for ONFI NAND
R	n/a	Reserved These pins shall not be connected by host.
RFU	n/a	Reserved For Future use These pins may be assigned for certain functions in the future
NU	n/a	Not Usable A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC	n/a	No (internal) connection A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.
NOTE 1 All Vcc, VccQ and Vss pins of each device shall be connected to common power supply outputs.		
NOTE 2 All Vcc, VccQ, Vss and VssQ shall not be disconnected.		

3 Physical Interface

3.1 AC/DC operating condition

Table 2 — Single-Ended AC and DC Input Levels for control signals¹⁾ and DQ-related signals²⁾

Parameter	Symbol	Min.	Max.	Unit
DC input high for control signals ¹⁾	VIH.CNT(DC)	0.7*V _{CCQ}	V _{CCQ}	V
DC input low for control signals ¹⁾	VIL.CNT(DC)	V _{SSQ}	0.3*V _{CCQ}	
AC input high for control signals ¹⁾	VIH.CNT(AC)	0.8*V _{CCQ}	Overshoot spec	
AC input low for control signals ¹⁾	VIL.CNT(AC)	Undershoot spec	0.2*V _{CCQ}	
DC input high for DQ-related signals ²⁾ w/o VREFQ	VIH.DQ(DC)	0.7*V _{CCQ}	V _{CCQ}	
DC input low for DQ-related signals ²⁾ w/o VREFQ	VIL.DQ(DC)	V _{SSQ}	0.3*V _{CCQ}	
AC input high for DQ-related signals ²⁾ w/o VREFQ	VIH.DQ(AC)	0.8*V _{CCQ}	Overshoot spec	
AC input low for DQ-related signals ²⁾ w/o VREFQ	VIL.DQ(AC)	Undershoot spec	0.2*V _{CCQ}	
DC input high for DQ-related signals ²⁾ w/ VREFQ (1.8V VccQ)	VIH.DQ(DC)	Note 3)	V _{CCQ}	
DC input low for DQ-related signals ²⁾ w/ VREFQ (1.8V VccQ)	VIL.DQ(DC)	V _{SSQ}	Note 3)	
AC input high for DQ-related signals ²⁾ w/ VREFQ (1.8V VccQ)	VIH.DQ(AC)	Note 3)	Note 3)	
AC input low for DQ-related signals ²⁾ w/ VREFQ (1.8V VccQ)	VIL.DQ(AC)	Note 3)	Note 3)	
DC input high for DQ-related signals ²⁾ w/ VREFQ (1.2V VccQ)	VIH.DQ(DC)	V _{REFQ} +0.1	V _{CCQ}	
DC input low for DQ-related signals ²⁾ w/ VREFQ (1.2V VccQ)	VIL.DQ(DC)	V _{SSQ}	V _{REFQ} -0.1	
AC input high for DQ-related signals ²⁾ w/ VREFQ (1.2V VccQ)	VIH.DQ(AC)	V _{REFQ} +0.15	Overshoot spec	
AC input low for DQ-related signals ²⁾ w/ VREFQ (1.2V VccQ)	VIL.DQ(AC)	Undershoot spec	V _{REFQ} -0.15	
NOTE 1 Control signals are CE_n, WE_n, WP_n, ALE and CLE				
NOTE 2 DQ-related signals are RE_n, DQS_n, DQs				
NOTE 3 Refer to vendor specification				

3.1 AC/DC operating condition (cont'd)

Table 3 — Single-Ended AC and DC Output Levels for control signals¹⁾ and DQ-related signals²⁾

Parameter	Symbol	Min.	Max.	Unit
DC Output high for control signals	VOH.CNT(DC)	0.7*V _{CCQ}	-	V
DC Output low for control signals	VOL.CNT(DC)	-	0.3*V _{CCQ}	
AC Output high for control signals	VOH.CNT(AC)	0.8*V _{CCQ}	-	
AC Output low for control signals	VOL.CNT(AC)	-	0.2*V _{CCQ}	
AC Output high for DQ-related signals (1.2V VccQ)	VOH.DQ(AC) (w/ termination)	V _{TT} + 0.1*V _{CCQ}	-	
AC Output low for DQ-related signals (1.2V VccQ)	VOL.DQ(AC) (w/ termination)	-	V _{TT} - 0.1*V _{CCQ}	
NOTE 1 Control signals are R/B_n				
NOTE 2 DQ-related signals are DQS_n, DQs				

Table 4 — Differential AC and DC Input/Output Levels (1.2V VccQ)

Parameter	Symbol	Min.	Unit
DC differential input ¹⁾	VID(DC)	0.2	V
AC differential input	VID(AC)	0.3	
AC differential output	VOD(AC)	0.2*V _{CCQ}	

NOTE 1 VID(AC) specifies the input differential voltage |V_{TR} -V_{CP} | required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal. The minimum value is equal to V_{IH}(AC) - V_{IL}(AC).

Table 5 — Differential signals cross point (1.2V VccQ)

Parameter	Symbol	Min.	Max.	Unit
AC differential input cross point ¹⁾	V _{IX}	0.5*V _{CCQ} - 0.12	0.5*V _{CCQ} +0.12	V
AC differential output cross point ²⁾	V _{OX}	0.5*V _{CCQ} - 0.15	0.5*V _{CCQ} +0.15	
NOTE 1 The typical value of V _{IX} is expected to be about 0.5 * V _{CCQ} of the transmitting device and V _{IX} (AC) is expected to track variations in V _{CCQ} . V _{IX} (AC) indicates the voltage at which differential input signals must cross.				
NOTE 2 V _{OX} shall be guaranteed only after ZQ calibration completed.				

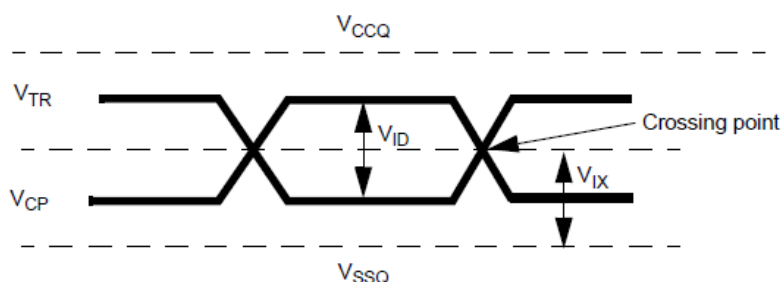


Figure 2 — Differential signal levels

3.2 AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from V_{CCQ} and V_{SSQ} levels. Table 6 defines the maximum values that the AC overshoot or undershoot may attain. These values apply for 1.2 V V_{CCQ} levels.

Table 6 — AC Overshoot/Undershoot Specification (1.2V V_{CCQ})

Parameter	Maximum value				Unit
	~200Mhz	~266Mhz	~333Mhz	~400Mhz	
Max. peak amplitude allowed for overshoot area	0.35				V
Max. peak amplitude allowed for undershoot area	0.35				V
Max. overshoot area above V_{CCQ}	0.40	0.30	0.24	0.20	V*ns
Max. undershoot area above V_{SSQ}	0.40	0.30	0.24	0.20	V*ns

NOTE 1 This standard is intended for devices with no clamp protection and is guaranteed by design.

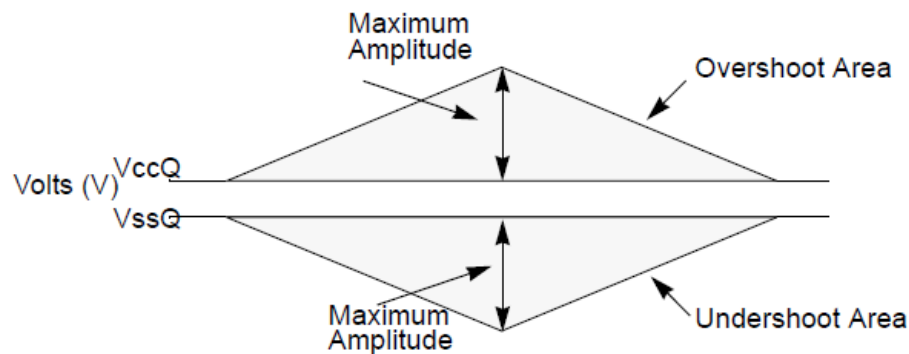


Figure 3 — Overshoot/Undershoot Diagram

3.3 Recommended DC Operating Conditions

3.3.1 DC Supply Voltage

Lower voltage is generally more preferred for high speed operation in terms of signal integrity and power consumption. 1.2 V V_{CCQ} is recommended to enable speeds up to 800Mbps. A NAND device shall support at least one of 3.3 V V_{CCQ} or 1.8 V V_{CCQ} or 1.2 V V_{CCQ} .

Table 7 — Supply Voltage Parameter Description

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage for 3.3 V devices ²	V_{CC}	2.7	3.3	3.6	V
Supply voltage for 1.8 V devices ²	V_{CC}	1.7	1.8	1.95	V
Supply voltage for 3.3 V I/O signaling ²	V_{CCQ}	2.7	3.3	3.6	V
Supply voltage for 1.8 V I/O signaling ²	V_{CCQ}	1.7	1.8	1.95	V
Supply voltage for 1.2 V I/O signaling ²	V_{CCQ}	1.14	1.2	1.26	V
Ground voltage supply	V_{SS}	0	0	0	V
Ground voltage supply for I/O signaling	V_{SSQ}	0	0	0	V
External voltage supply ¹	V_{PP}	10.8	12.0	13.2	V

NOTE 1 The maximum external voltage supply (I_{pp}) is 5 mA per LUN.
 NOTE 2 AC noise requirements on V_{CC} and V_{CCQ} are the following:
 a) From 10KHz to 40MHz, the AC noise shall be less than +/- 3% of the nominal voltage
 b) From 40MHz to 800MHz, the AC noise shall always be less than +/- 3% of the nominal voltage. If the AC noise is more than +/- 1% of the nominal voltage, a different vendor specific tQSH/tQSL value may be specified.
 c) More than 800MHz, the AC noise shall be less than +/- 3% of the nominal voltage.

3.3.2 DC Output leakage current requirements for V_{CCQ} of 1.8 V and V_{CCQ} of 1.2 V

Table 8 — DC output leakage current requirements (ILO) for conditions for V_{CCQ} of 1.8 V and for V_{CCQ} of 1.2 V

Symbol	Parameter	Max
ILOpd	Pull-Down Output leakage current: DQ are disabled: $V_{OUT}=V_{CCQ}$;	7uA ¹
ILOpu	Pull-Up Output leakage current: DQ are disabled: $V_{OUT}=0V$; ODT disabled	7uA ¹

NOTE 1 Absolute leakage value per DQ pin per NAND die. The following signals are required to meet output leakage (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c)

4 Package and Addressing

4.1 BGA-63 (Single x8 / x16 BGA)

Figure 4 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the asynchronous SDR data interface. Figure 5 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 8-bit data access for the synchronous DDR data interface. Figure 6 defines the ball assignments for devices using NAND Single x8 / x16 BGA packaging with 16-bit data access for the asynchronous SDR data interface. The NAND Single x8/x16 BGA package with 16-bit data access does not support the Synchronous DDR data interface.

This package uses MO-201

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	NC	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	NC	NC	VSP2		
H			NC	IO0	NC	NC	NC	VCCQ		
J			NC	IO1	NC	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 4 — Ball assignments for 8-bit data access, asynchronous SDR only data interface

4.1 BGA-63 (Single x8 / x16 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	NC	R/B0_n		
D			VCC	W/R_n or RE_0_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	VREFQ	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	NC	NC	VSP2		
H			NC	DQ0	DQS_c	CK_c	CK or WE_0_n	VCCQ		
J			NC	DQ1	DQS	VCCQ	DQ5	DQ7		
K			VSSQ	DQ2	DQ3	DQ4	DQ6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

NOTE 1 WE_n is located at ball H7 when a Synchronous DDR capable part is used in asynchronous SDR mode.

Figure 5 — Ball assignments for 8-bit data access, Synchronous DDR data interface

4.1 BGA-63 (Single x8 / x16 BGA) (cont'd)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP_n	ALE	VSS	CE0_n	WE_n	R/B0_n		
D			VCC	RE_n	CLE	CE1_n	CE2_n	R/B1_n		
E			NC	NC	NC	NC	CE3_n	R/B2_n		
F			NC	NC	NC	NC	VSS	R/B3_n		
G			VSP3	VCC	VSP1	IO13	IO15	VSP2		
H			IO8	IO0	IO10	IO12	IO14	VCCQ		
J			IO9	IO1	IO11	VCCQ	IO5	IO7		
K			VSSQ	IO2	IO3	IO4	IO6	VSSQ		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

Figure 6 — Ball assignments for 16-bit, asynchronous SDR only data access

4.2 BGA-100 (Dual x8 BGA)

Figure 7 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the asynchronous SDR data interface. Figure 8 defines the ball assignments for devices using NAND Dual x8 BGA packaging with dual 8-bit data access for the Toggle DDR or Synchronous DDR data interface. The minimum package size is 12x18mm and the maximum package size is 14x18mm.

This package uses MO-304.

	1	2	3	4	5	6	7	8	9	10
A	R	R							R	R
B	R									R
C										
D		R	VSP	VSP2_1	WP_1_n	VSP1_1	VSP0_1	VSP	R	
E		R	VSP	VSP2_0	WP_0_n	VSP1_0	VSP0_0	VSP	VDDi	
F		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	
G		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	
H		VSSQ	VCCQ	R	R	R/B0_1_n	R/B1_1_n or ENo	VCCQ	VSSQ	
J		IO0_1	IO2_1	ALE_1	CE1_1_n	R/B0_0_n	R/B1_0_n	IO5_1	IO7_1	
K		IO0_0	IO2_0	ALE_0	CE1_0_n or ENi	CE0_1_n	CE0_0_n	IO5_0	IO7_0	
L		VCCQ	VSSQ	VCCQ	CLE_1	RE_1_n	VCCQ	VSSQ	VCCQ	
M		IO1_1	IO3_1	VSSQ	CLE_0	RE_0_n	VSSQ	IO4_1	IO6_1	
N		IO1_0	IO3_0	NC	NC	NC	WE_1_n	IO4_0	IO6_0	
P		VSSQ	VCCQ	NC	NC	NC	WE_0_n	VCCQ	VSSQ	
R										
T	R									R
U	R	R							R	R

Figure 7 — Ball assignments for dual 8-bit data access, asynchronous SDR data interface