

JEDEC STANDARD

NAND Flash Interface Interoperability

JESD230F.01

(Editorial Revision of JESD230F, October 2022)

May 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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NAND FLASH INTERFACE INTEROPERABILITY

(From JEDEC Board Ballot JCB-22-09, formulated under the cognizance of the JC-42.4 Subcommittee on Nonvolatile Memory Devices, item numbers 1863.02 and 1767.58).

1 Scope

This standard was jointly developed by JEDEC and the Open NAND Flash Interface Workgroup, hereafter referred to as ONFI. This standard defines a standard NAND flash device interface interoperability standard that provides means for system be designed that can support Asynchronous SDR, Synchronous DDR and Toggle DDR NAND flash devices that are interoperable between JEDEC and ONFI member implementations.

2 Terms, Definitions, Abbreviations, and Conventions

2.1 Terms and Definitions

address: A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172 and JESD88.)

NOTE 1 In a nonvolatile memory array, the address consists of characters, typically hexadecimal, to identify the row and column location of the memory cell(s).

NOTE 2 For NAND nonvolatile memory devices, the row address is for a page, block, or logical unit number (LUN); the column address is for the byte or word within a page.

NOTE 3 The least significant bit of the column address is zero for the source synchronous data interface.

asynchronous: Describing operation in which the timing is not controlled by a clock.

NOTE For a NAND nonvolatile memory, asynchronous also means that data is latched with the WE_n signal for the write operation and the RE_n signal for the read operation.

block: A continuous range of memory addresses. (Ref. IEC 748-2 and JESD88.)

NOTE 1 The number of addresses included in the range is frequently equal to 2^n , where n is the number of bits in the address.

NOTE 2 For nonvolatile memories, a block consists of multiple pages and is the smallest addressable memory segment within a memory device for the erase operation.

column: In a nonvolatile memory array, a series of memory cells whose sources and/or drains are connected via a bit line.

NOTE 1 Depending on the nonvolatile memory array, the bit line is accessed via the column select transistor, the column address decoder, or other decoding scheme.

NOTE 2 In nonvolatile memory device, a column decoder accesses a bit (x1), byte (x8), word (x16), or Dword (x32) either individually or within a page.

NOTE 3 In a typical schematic of a memory array, the column is in the vertical direction.

2.1 Terms and Definitions (cont'd)

Dword (x32): A sequence of 32 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 31; the most significant bit is shown on the left. When shown as words, the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes, the least significant byte is byte 0 and the most significant byte is byte 3.

NOTE 2 See Figure 2.5-1 for a description of the relationship between bytes, words, and Dwords.

latching edge: The rising or falling edge of a waveform that initiates a latch operation.

NOTE 1 For a NAND nonvolatile memory, the latching edge is the edge of the CK or DQS signal on which the contents of the data bus are latched for the source synchronous data interface.

NOTE 2 For a NAND nonvolatile data cycle, the latching edge is both the rising and falling edges of the DQS signal.

NOTE 3 For a NAND nonvolatile command and address cycle, the latching edge for the source synchronous interface is the rising edge of the CK signal.

NAND defect area: A designated location within the NAND memory where factory defects are identified by the manufacturer.

NOTE 1 The location is a portion of either the first page and/or the last page of the factory-marked defect block, this defect area in each page is defined as (# of data bytes) to (# of data bytes + # of spare bytes -1).

NOTE 2 For an 8-bit data access NAND memory device, the manufacturer sets the first byte in the defect area of the first or last page of the defect block to a value of 00h.

NOTE 3 For a 16-bit data access NAND memory device, the manufacturer sets the first word in the defect area of the first or last page of the defect block to a value of 0000h.

NAND nonvolatile memory device: The packaged NAND nonvolatile memory unit containing one or more NAND targets.

NOTE This is referred to as "device" in this standard.

NAND row address: An address referencing the LUN, block, and page to be accessed.

NOTE 1 The page address uses the least significant row address bits.

NOTE 2 The block address uses the middle row address bits.

NOTE 3 The LUN address uses the most significant row address bits.

page: The smallest nonvolatile memory array segment, within a device, that can be addressed for read or program operations.

page register: A register used to transfer data from a page in the memory array for a read operation or to transfer data to a page in the memory array for a program operation.

read request (for a nonvolatile memory): A data output cycle request from the host that results in a data transfer from the device to the host.

source synchronous (for a nonvolatile memory): Describing an operation in which the strobe signal (DQS) is transmitted with the data to indicate when the data should be latched.

NOTE The strobe signal (DQS) is similar in concept to an additional data bus bit.

2.1 Terms and Definitions (cont'd)

status register (SR[x]): A register within a particular LUN containing status information about that LUN.

NOTE SR[x] refers to bit "x" within the status register.

target: A nonvolatile memory component with a unique chip enable (CE_n) select pin.

word (x16): A sequence of 16 bits that is stored, addressed, transmitted, and operated on as a unit within a computing system.

NOTE 1 A word may be represented as 16 bits or as two adjacent bytes. When shown as bits, the least significant bit is bit 0 and the most significant bit is bit 15; the most significant bit is shown on the left. When shown as bytes, the least significant byte (lower) is byte 0 and the most significant byte is byte 2.

NOTE 2 See Figure 2.5-1 for a description of the relationship between bytes, words, and Dwords.

2.2 Abbreviations

DDR: Abbreviation for "double data rate".

LUN (logical unit number): The minimum memory array size that can independently execute commands and report status.

N/A: Abbreviation for "not applicable". Fields marked as "na" are not used.

O/M: Abbreviation for Optional/Mandatory requirement. When the entry is set to "M", the item is mandatory. When the entry is set to "O", the item is optional.

2.3 Conventions

2.3.1 Active-low Signals

While the preferred method for indicating a signal that is active when low is to use the over-bar as in $\overline{CE}$, the difficulty in producing this format has resulted in several alternatives meant to be equivalents. These are the use of a CE reverse solidus (\) or the trailing underscore (_) following the signal name as in CE\ and CE_. In this publication "_n" is used to indicate an active low signal (i.e., an inverted logic sense).

2.3.2 Signal Names

The names of abbreviations, initials, and acronyms used as signal names are in all uppercase (e.g., CE_n). Fields containing only one bit are usually referred to as the "name bit" instead of the "name field". Numerical fields are unsigned unless otherwise indicated.

2.3.3 Precedence in Case of Conflict

If there is a conflict between text, figures, state machines, timing diagrams, and/or tables, the precedence shall be state machine, timing diagrams, tables, figures, and text.

2.4 Keywords

Several keywords are used to differentiate between different levels of requirements or suggestions.

mandatory: A keyword indicating items to be implemented as defined by a standard. Users are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the standard.

may: A keyword that indicates flexibility of choice between stated alternatives or possibly nothing with no implied preference.

optional: A keyword that describes features that are not required by the specification. However, if any optional feature defined by the specification is implemented, that feature shall be implemented in the way defined by the specification.

reserved: A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field may be cleared to zero or in accordance with a future extension to this publication. A host should not read/use reserved information.

shall: A keyword indicating a mandatory requirement.

should: A keyword indicating flexibility of choice with a strongly preferred alternative. This is equivalent to the phrase "it is recommended".

2.5 Byte, Word, and Dword Relationships

Figure 2.5-1 illustrates the relationship between bytes, words, and Dwords

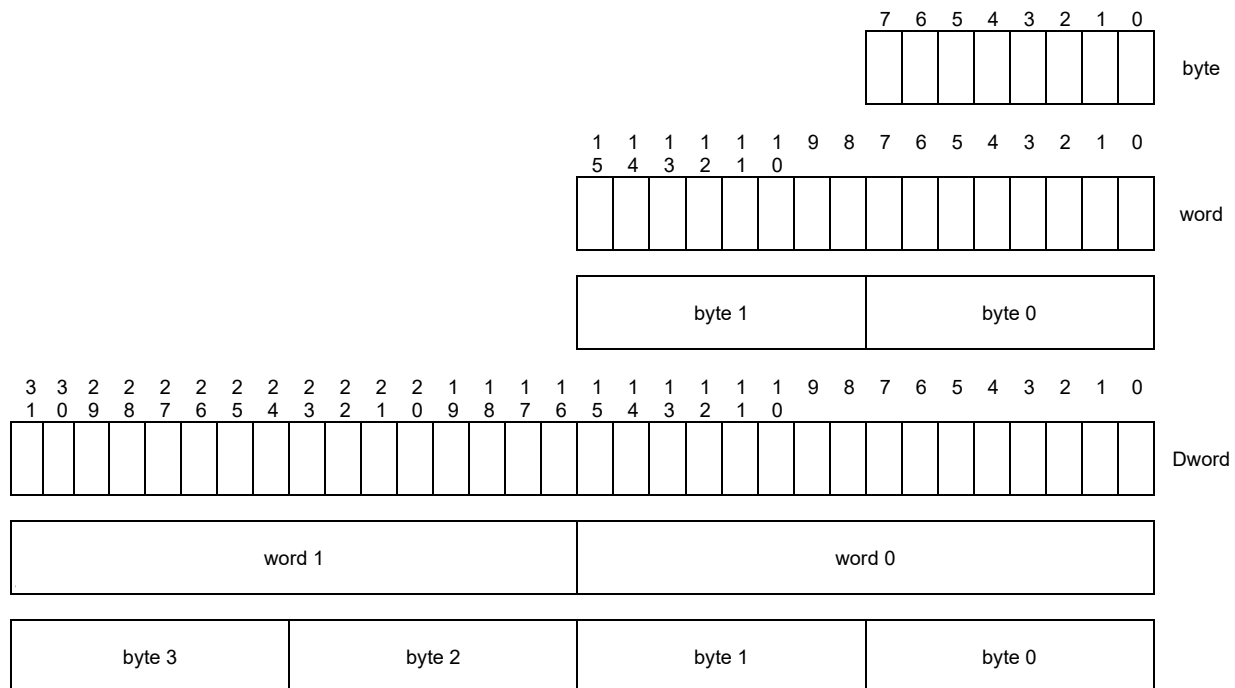


Figure 2.5-1 — Byte, Word, and Dword Relationships

2.6 Pin Description

Table 2.6-1 — Pin Description

Name	Input/ Output	Description
IO0 ~ IO7(~ IO15) DQ0 ~ DQ7 DQ0_x ~ DQ7_x	I/O	DATA INPUTS/OUTPUTS These signals are used to input command, address and data, and to output data during read operations. The signals float to high-z when the chip is deselected or when the outputs are disabled. IO0 ~ IO15 are used in a 16-bit wide target configuration. With multi channel support, IO0_0~IO7_0 and IO0_1~IO7_1 are used for IOs of channel 0 and IOs of channel 1 respectively. Also known as DQ0~DQ7 for Toggle DDR and Synchronous DDR. The number after the underscore represents the channel. For example, DQ0_0 indicates DQ0 of channel-0 and DQ0_1 does DQ0 of channel-1.
CLE_x	I	COMMAND LATCH ENABLE The CLE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
ALE_x	I	ADDRESS LATCH ENABLE The ALE_x signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
CEx_x_n	I	CHIP ENABLE The CEx_x_n input is the target selection control. When CEx_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CEx_x_n is low, the target is selected.
WE_x_n	I	WRITE ENABLE The WE_x_n input controls writes to the I/O port. For Asynchronous SDR Data, commands, addresses are latched on the rising edge of the WE_x_n pulse. For Toggle DDR commands, addresses are latched on the rising edge of the WE_x_n pulse.
R/B_x_n	O	READY/BUSY OUTPUT The R/B_x_n output indicates the status of the target operation. When low, it indicates that one or more operations are in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
RE_x_n (RE_x_t)	I	READ ENABLE The RE_x_n input is the serial data-out control. For Asynchronous SDR Data is valid tREA after the falling edge and for Toggle DDR Data is valid after the falling edge and rising edge of RE_x_n which also increments the internal column address counter by each one.
RE_x_c	I	Complement of Read Enable This is the complementary signal to Read Enable
DQS_x (DQS_x_t)	I/O	Data Strobe The data strobe signal that indicates the data valid window for Toggle DDR and Synchronous DDR data interface. Output with read data, input with write data. Edge-aligned with read data, centered in write data.
DQS_x_c	I/O	Complement of Data Strobe This is the complementary signal to Data Strobe.
DBI_x	I/O	Data Bus Inversion Optional pin/function for NAND device to reduce power consumption and power/noise during data input/output. The device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not.

Table 2.6-1 — Pin Description (cont'd)

Name	Input/ Output	Description
W/R_x	I	Write/Read Direction The Write/Read Direction signal indicates the owner of the DQ bus and DQS signal in the Synchronous DDR data interface. This signal shares the same pin as RE_x_n in the asynchronous data interface.
CK_x	I	Clock The Clock signal is used as the clock in Synchronous DDR data interface. This signal shares the same pin as WE_x_n in the asynchronous data interface.
WP_x_n ^{3,4}	I	WRITE PROTECT The WP_x_n disables the Flash array program and erase operations.
ODT_x_n ^{3,4}	I	ODT (On Die Termination) Pin This signal enables and disables termination on the NAND DQ, DQS, RE bus according to the specified set feature settings.
Vcc	I	POWER VCC is the power supply for device.
VccQ	I	I/O POWER The VccQ is the power supply for input and/or output signals.
Vss	I	GROUND The Vss signal is the power supply ground.
VssQ	I	I/O GROUND The VssQ signal is the ground for input and/or output signals
VSPx	n/a	Vendor Specific The function of these signals is defined and specified by the NAND vendor. Any VSP signal not used by the NAND vendor shall not be connected internal to the device.
VREFQ	n/a	Reference voltage This is used as an external voltage reference.
V _{PP}	I	High Voltage Power The V _{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g. improve power efficiency)
RZQ_x	Supply	Reference pin for ZQ calibration This is used on ZQ calibration and RZQ ball shall be connected to Vss through 300ohm resistor
ENi / ENo	I/O	Enumeration pins These pins may be used for ONFI NAND
R	n/a	Reserved. These pins shall not be connected by host.
RFU	n/a	Reserved for Future Use These pins may be assigned for certain functions in the future
NU	n/a	Not Usable A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC	n/a	No (internal) connection A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.

Table 2.6-1 — Pin Description (cont'd)

NOTE 1	All Vcc, VccQ and Vss pins of each device shall be connected to common power supply outputs.
NOTE 2	All Vcc, VccQ, Vss and VssQ shall not be disconnected.
NOTE 3	Some vendor define WP_x_n pin as multi-function. User can use ODT_x_n instead of WP_x_n via set-feature. The default mode of this multi-function pin is WP_x_n.
NOTE 4	WP/ODT mode selection should be set to WP before power-off to make the pin working as Write Protect for protecting against data corruption at power-off.

3 NAND Interface General Information

3.1 NAND Interface Spec Overview

Table 3.1-1 — NAND Interface Comparison Table

Interface Items	Toggle 4.0	ONFI 4.2	JESD230E	JESD230F
VCC	2.5 V/3.3 V (Optional)		2.5 V/3.3 V (Optional)	2.5 V/3.3 V (Optional)
VCCQ	1.2 V/1.8 V (Optional)		1.2 V	1.2 V
DQ (Bus Width)	x8		X8	X8
Max Data Rate	~1.2 Gbps	~1.6 Gbps	~2.4Gbps	~3.6 Gbps ⁷
Vref	External VrefQ is Required > 200 Mbps		Internal VrefQ is allowed for CTT ² > 200 Mbps, External VrefQ is optional for CTT ² > 200 Mbps, Internal VrefQ is required for LTT ³	Internal VrefQ is allowed for CTT ² > 200Mbps, External VrefQ is optional for CTT ² > 200Mbps, Internal VrefQ is required for LTT ³
Input Path Topology	Matched DQS		Matched DQS	Matched DQS or Unmatched DQS (see vendor datasheet)
OCD Topology	HSUL ¹ /CTT ²		HSUL/CTT/LTT ^{1,2,3}	HSUL/CTT/LTT ^{1,2,3}
ODT ⁴ Control	ODT (nWP) pin	Matrix Termination	ODT (nWP) pin or Matrix Termination	ODT (nWP) pin or Matrix Termination
Ron CAL	ZQ		ZQ	ZQ
CMD/ADDR IO	SDR (nWE sync, ~100 MHz)	SDR (nWE sync, ~40 MHz)	SDR (nWE sync, ~40 MHz – ~100 MHz)	SDR (nWE sync, ~40 MHz – ~100 MHz)
DBI ⁵	N/A		Optional	Optional
Training	Write/Read DQ/DCC ⁶		Write/Read DQ/DCC/Internal VrefQ	Write/Read DQ/DCC/ Internal VrefQ WDCA (optional) Write Training Monitor (optional) Per-pin VrefQ Adjustment (optional)
Differential Signaling on Power-up	Disabled		Disabled	Vendor specific (see vendor datasheet)
Equalization	Not Required		Not Required	Optional and Vendor specific
Fast Set/Get Features	Not Supported		Not Supported	Optional
NOTE 1 HSUL: High Speed Unterminated Logic NOTE 2 CTT: Center Tapped Termination NOTE 3 LTT: Low Tapped Termination NOTE 4 ODT: On Die Termination NOTE 5 DBI: Data Bus Inversion NOTE 6 DCC: Duty Cycle Correction NOTE 7 3.6 GT/s is not mandatory, NAND vendors may only support up to 3.2GT/s (see vendor datasheet).				

3.2 Supported Features and Operating Conditions Versus Data Transfer Rate

Table 3.2-1 — Supported Features and Operating Conditions Versus Data Transfer Rate

Feature			~200 Mbps	~400 Mbps	~800 Mbps	~1200 Mbps, ~1600 Mbps, ~1800 Mbps, ~2000 Mbps, ~2200 Mbps, ~2400 Mbps	~2800 Mbps, ~3200 Mbps, ~3600 Mbps
VccQ			1.2 V				
I/O Type	Single-ended Signaling for DQS and RE ^{1, 2}	NAND	Supported	Not supported			
		Host	Optional				
	Differential Signaling for DQS and RE	NAND	Supported				
		Host	Optional	Required			
ZQ Calibration		NAND	Supported				
		Host	Optional		Required		
Training (DCC)		NAND	Not supported			Required	
		Host					
Training (Read)		NAND	Supported				
		Host	Optional			Required	
Training (Write)		NAND	Supported				
		Host	Optional for Matched DQS NAND, Required for Unmatched DQS NAND			Required for both Unmatched DQS and Matched DQS NAND	
Training (WDCA)		NAND	Optional				
		Host	Optional				
On Die (NAND) Termination	CTT	NAND	Supported				
		Host	Optional ³				
	LTT	NAND	Supported				
		Host	Optional ³				
Equalization		NAND	Optional and Vendor Specific				
		Host	Optional and Vendor Specific				
NOTE 1 For CTT mode, the device can be used up to 200 Mbps without Differential Signals. To use high speed over 200 Mbps,							
NOTE 2 Differential Signals shall be used and asserted before High-speed setting.							
NOTE 3 For LTT mode, Differential Signaling is always required, even below 200 Mbps. Host can enable/disable On Die (NAND) Termination.							

3.3 Supported VrefQ Versus Data Transfer Rate

Table 3.3-1 — Supported VrefQ Versus Data Transfer Rate

Feature				~60 Mbps	~80 Mbps	~200 Mbps	> 200 Mbps
VrefQ	CTT ¹	Internal VrefQ (Default Level)	NAND	Supported	Not Supported		
			Host				
		Internal VrefQ (VccQ/2 setting)	NAND	Optional			Optional ²
			Host				
		External VrefQ (VccQ/2)	NAND	Optional ²			
			Host				
	LTT ³	Internal VrefQ	NAND	Supported			
			Host				
		External VrefQ	NAND	Not Supported			
			Host				

NOTE 1

The host and NAND shall power-up with the CTT interface enabled and with Internal VrefQ. The maximum data rate supported with the default internal VrefQ setting is only up to ~60Mbps and further initialization may be done at a faster data rate (up to ~200Mbps) on the CTT interface, provided that either the Internal VrefQ is configured to VccQ/2 or External VrefQ has been enabled for use on both the NAND and the Host.

NOTE 2

NAND External VrefQ support is optional. In the case where NAND support for External VrefQ has been removed, then NAND shall use Internal VrefQ, and the NAND vendor may recommend an Internal VrefQ setting that shall be used for high speed CTT interface operations or may require CTT interface Internal VrefQ training. If a device does not support >200Mbps operations with Internal VrefQ, then External VrefQ shall be required for >200Mbps operations

NOTE 3

The host shall ensure that the NAND internal VrefQ is within the NAND Minimum Internal VrefQ Allowable Range allowed for the LTT interface prior to enabling the LTT interface, and at any time while the LTT interface is active. External VrefQ shall always be disabled when the device runs in LTT mode.

4 Physical Interface

4.1 Input Specifications

4.1.1 AC/DC Levels

4.1.1.1 Combo Interface Devices

4.1.1.1.1 CTT Interface (1.2 V VccQ) AC/DC Levels

Table 4.1-1 — CTT Interface Single-Ended AC and DC Input Levels for Control and DQ-related Signals

Parameter	Symbol	Up to 1200 Mbps	>1200 Mbps up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps 2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC input high for control signals	V _{IH,CNT} (DC)	0.7*V _{CCQ}			0.7*V _{CCQ}	1	V
DC input low for control signals	V _{IL,CNT} (DC)	0.3*V _{CCQ}			0.3*V _{CCQ}		
AC input high for control signals	V _{IH,CNT} (AC)	0.8*V _{CCQ}			0.8*V _{CCQ}		
AC input low for control signals	V _{IL,CNT} (AC)	0.2*V _{CCQ}			0.2*V _{CCQ}		
DC input high for DQ-related signals w/o V _{REFQ}	V _{IH,DQrel} (DC)	0.7*V _{CCQ}			0.7*V _{CCQ}	2, 3	
DC input low for DQ-related signals w/o V _{REFQ}	V _{IL,DQrel} (DC)	0.2*V _{CCQ}			0.2*V _{CCQ}		
AC input high for DQ-related signals w/o V _{REFQ}	V _{IH,DQrel} (AC)	0.8*V _{CCQ}			0.8*V _{CCQ}		
AC input low for DQ-related signals w/o V _{REFQ}	V _{IL,DQrel} (AC)	0.1*V _{CCQ}			0.1*V _{CCQ}		
DC input high for DQ-related signals for Data Input w/ V _{REFQ}	V _{IH,DQrel} (DC)	V _{REFQ} +0.100	V _{REFQ} +0.100 (ONFI)	V _{REF} Q+0.08	V _{REF} Q+0.07	2, 4, 5	
			V _{REF} Q+0.08(Toggle)				
DC input low for DQ-related signals for Data Input w/ V _{REFQ}	V _{IL,DQrel} (DC)	V _{REFQ} -0.100	V _{REF} Q-0.100 (ONFI)	V _{REF} Q-0.08	V _{REF} Q-0.07		
			V _{REF} Q-0.08(Toggle)				
AC input high for DQ-related signals for Data Input w/ V _{REFQ}	V _{IH,DQrel} (AC)	V _{REFQ} +0.150	V _{REF} Q+0.150 (ONFI)	V _{REF} Q+0.100	V _{REF} Q+0.095		
			V _{REF} Q+0.100 (Toggle)				
AC input low for DQ-related signals for Data Input w/ V _{REFQ}	V _{IL,DQrel} (AC)	V _{REFQ} -0.150	V _{REF} Q-0.150 (Toggle)	V _{REF} Q-0.100	V _{REF} Q-0.095		
			V _{REF} Q+0.100 (Toggle)				

Table 4.1-1 — CTT Interface Single-Ended AC and DC Input Levels for Control and DQ-related Signals (cont'd)

NOTE 1	Control signals are CE_n, WE_n, ODT_n/WP_n, ALE, and CLE.
NOTE 2	DQ-related signals are RE_t, RE_n, DQS_t, DQS_c and DQ[7:0] and DBI. For RE_t, RE_n, DQS_t, and DQS_c these are single-ended signal requirements.
NOTE 3	Specs apply to NAND command, address bus cycles and unterminated data input cycles.
NOTE 4	V _{REFQ} may be External VrefQ or Internal VrefQ (if NAND device supports >200 Mbps with Internal VrefQ, see vendor datasheet).
NOTE 5	For DQ signals, at 1600 MT/s these specifications may be replaced by Rx Mask and VIH _{AC} specifications (see vendor datasheet), but above 1600MT/s the Rx Mask and VIH _{AC} specifications shall be used.

Table 4.1-2 — CTT Interface External Reference Voltage Requirements

Parameter	Symbol	Min	Max	Notes	Unit
External Reference Voltage	VREFQ(DC)	0.49*VccQ	0.51*VccQ	1	V
NOTE 1 See NAND vendor datasheet if External VrefQ is supported for CTT interface.					

Table 4.1-3 — CTT Interface Differential AC and DC Input Levels and Cross-Point

Table 4-10 CTT Interface Differential AC and DC Input Levels and Cross Point							
Parameter	Symbol	Up to 1200 Mbps	>1200 Mbps up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps, 2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC differential input	V _{ID} (DC)	0.200	0.200 (ONFI)	0.160	0.140	1	V
			0.160 (Toggle)				
AC differential input	V _{ID} (AC)	0.300	0.300 (ONFI)	0.200	0.190		
			0.200 (Toggle)				
AC differential input cross-point	V _{IX}	0.5xVccQ±0.120	0.5xVccQ±0.080	0.5xVccQ±0.080	0.5xVccQ±0.068	2	
NOTE 1	VID(DC) and VID(AC) specify the input differential voltage VTR-VCP required for switching where VTR is the ‘true’ input signal while VCP is the ‘complementary’ input signal. The minimum values are equal to VIH(DC) – VIL(DC) and VIH(AC) – VIL(AC), respectively.						
NOTE 2	For CTT, the typical value of V _{IX} is expected to be about 0.5*VccQ of the transmitting device and V _{IX} is expected to track variations in VREFDQ. V _{IX} indicates the voltage at which differential input signals must cross.						

4.1.1.1.2 LTT Interface (1.2 V VccQ) AC/DC Levels

Table 4.1-4 — LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals

Parameter	Symbol	<1600 Mbps	1600 Mbps, 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC input high for control signals	V _{IH.CNT} (DC)	0.7*V _{ccQ}					1	V
DC input low for control signals	V _{IL.CNT} (DC)	0.3*V _{ccQ}						
AC input high for control signals	V _{IH.CNT} (AC)	0.8*V _{ccQ}						
AC input low for control signals	V _{IL.CNT} (AC)	0.2*V _{ccQ}						
DC input high for DQ-related signals (Unterminated)	V _{IH.DQrel.underm} (DC)	0.5*V _{ccQ}					2, 3, 7	
DC input low for DQ-related signals (Unterminated)	V _{IL.DQrel.underm} (DC)	0.080						
AC input high for DQ-related signals (Unterminated)	V _{IH.DQrel.underm} (AC)	0.5*V _{ccQ}						
AC input low for DQ-related signals (Unterminated)	V _{IL.DQrel.underm} (AC)	0.060						
DC input high for DQ-related signals w/ V _{REFQ} (Terminated)	V _{IH.DQrel} (DC)	V _{cent_DQrel} + 0.080				V _{cent_DQrel} + 0.060	2, 4, 5	
DC input low for DQ-related signals w/ V _{REFQ} (Terminated)	V _{IL.DQrel} (DC)	V _{cent_DQrel} - 0.080				V _{cent_DQrel} - 0.060		
AC input high for DQ-related signals w/ V _{REFQ} (Terminated)	V _{IH.DQrel} (AC)	V _{cent_DQrel} + 0.100				V _{cent_DQrel} + 0.085	2, 4, 6	
AC input low for DQ-related signals w/ V _{REFQ} (Terminated)	V _{IL.DQrel} (AC)	V _{cent_DQrel} - 0.100				V _{cent_DQrel} - 0.085		

Table 4.1-4 — LTT Interface Single-Ended AC and DC Input Levels for Control and DQ-Related Signals (cont'd)

NOTE 1	Control signals are CE_n, WE_n, ODT_n/WP_n, ALE and CLE.
NOTE 2	DQ-related signals are RE_t, RE_n, DQS_t, DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t and DQS_c these are single-ended signal requirements.
NOTE 3	Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled.
NOTE 4	Vcent_DQ _{rel} shall be regarded as Vcent_RE, Vcent_DQS and Vcent_DQ for RE_t/RE_c, DQS_t/DQS_c, and DQ[7:0] signals, respectively.
NOTE 5	For DQ signals, DC signal requirements are replaced with the Rx Mask
NOTE 6	For DQ signals, AC signal requirements are replaced with the VIH _L _AC specification.
NOTE 7	NAND vendors may support a higher VIL.DQ _{rel} .unterm or lower VIH.DQ _{rel} .unterm specification. See vendor datasheet.

Table 4.1-5 — LTT Interface Differential AC and DC Input Levels and Cross-Point

Parameter	Symbol	Up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DC differential input	V _{ID} (DC)	0.160	0.160	0.160	0.120	1	V
AC differential input	V _{ID} (AC)	0.200	0.200	0.200	0.170		
AC differential input cross-point	V _{IX}	VREFDQ ± 0.064	VREFDQ ± 0.064	VREFDQ ± 0.064	VREFDQ ± 0.054	2	
NOTE 1 V _{ID} (DC) and V _{ID} (AC) specify the input differential voltage V _{TR} -V _{CP} required for switching where V _{TR} is the 'true' input signal while V _{CP} is the 'complementary' input signal. The minimum values are equal to V _{IH} (DC) – V _{IL} (DC) and V _{IH} (AC) – V _{IL} (AC) respectively.							
NOTE 2 For LTT, the typical value of V _{IX} is expected to be about VREFDQ of the NAND Flash Memory internal setting value by VREF Training and V _{IX} is expected to track variations in VREFDQ. V _{IX} indicates the voltage at which differential input signals must cross.							

4.1.1.2 Legacy CTT-only Devices

Table 4.1-6 — Single-Ended AC and DC Input Levels for Control Signals¹ and DQ-related Signals²

Parameter	Symbol	Min.	Max.	Unit
DC input high for control signals ¹	VIH.CNT(DC)	0.7*V _{CCQ}	V _{CCQ}	V
DC input low for control signals ¹	VIL.CNT(DC)	V _{SSQ}	0.3*V _{CCQ}	
AC input high for control signals ¹	VIH.CNT(AC)	0.8*V _{CCQ}	Overshoot spec	
AC input low for control signals ¹	VIL.CNT(AC)	Undershoot spec	0.2*V _{CCQ}	
DC input high for DQ-related signals ² without VREFQ	VIH.DQ(DC)	0.7*V _{CCQ}	V _{CCQ}	
DC input low for DQ-related signals ² without VREFQ	VIL.DQ(DC)	V _{SSQ}	0.3*V _{CCQ}	
AC input high for DQ-related signals ² without VREFQ	VIH.DQ(AC)	0.8*V _{CCQ}	Overshoot spec	
AC input low for DQ-related signals ² without VREFQ	VIL.DQ(AC)	Undershoot spec	0.2*V _{CCQ}	
DC input high for DQ-related signals ² with VREFQ (1.8 V V _{ccQ})	VIH.DQ(DC)	Note 3	V _{CCQ}	
DC input low for DQ-related signals ² with VREFQ (1.8 V V _{ccQ})	VIL.DQ(DC)	V _{SSQ}	Note 3	
AC input high for DQ-related signals ² with VREFQ (1.8 V V _{ccQ})	VIH.DQ(AC)	Note 3	Note 3	
AC input low for DQ-related signals ² with VREFQ (1.8 V V _{ccQ})	VIL.DQ(AC)	Note 3	Note 3	
DC input high for DQ-related signals ² with VREFQ (1.2 V V _{ccQ})	VIH.DQ(DC)	V _{REFQ} +0.1	V _{CCQ}	
DC input low for DQ-related signals ² with VREFQ (1.2 V V _{ccQ})	VIL.DQ(DC)	V _{SSQ}	V _{REFQ} -0.1	
AC input high for DQ-related signals ² with VREFQ (1.2 V V _{ccQ})	VIH.DQ(AC)	V _{REFQ} +0.15	Overshoot spec	
AC input low for DQ-related signals ² with VREFQ (1.2 V V _{ccQ})	VIL.DQ(AC)	Undershoot spec	V _{REFQ} -0.15	
NOTE 1 Control signals are CE_n, WE_n, WP_n, ALE and CLE				
NOTE 2 DQ-related signals are RE_n, DQS_n, DQs				
NOTE 3 Refer to vendor specification				

4.1.1.2 Legacy CTT-only Devices (cont'd)

Table 4.1-7 — Single-Ended AC and DC Output Levels for Control Signals¹ and DQ-related Signals²

Parameter	Symbol	Min.	Max.	Unit
DC Output high for control signals	VOH.CNT(DC)	0.7*V _{CCQ}	-	V
DC Output low for control signals	VOL.CNT(DC)	-	0.3*V _{CCQ}	
AC Output high for control signals	VOH.CNT(AC)	0.8*V _{CCQ}	-	
AC Output low for control signals	VOL.CNT(AC)	-	0.2*V _{CCQ}	
AC Output high for DQ-related signals (1.2 V V _{ccQ})	VOH.DQ(AC) (w/ termination)	V _{TT} + 0.1*V _{CCQ}	-	
AC Output low for DQ-related signals (1.2 V V _{ccQ})	VOL.DQ(AC) (w/ termination)	-	V _{TT} - 0.1*V _{CCQ}	
NOTE 1 Control signals are R/B_n				
NOTE 2 DQ-related signals are DQS_n, DQs				

Table 4.1-8 — Differential AC and DC Input/Output Levels (1.2 V VccQ)

Parameter	Symbol	Min.	Unit
DC differential input ¹	VID(DC)	0.2	V
AC differential input	VID(AC)	0.3	
AC differential output	VOD(AC)	0.2*V _{CCQ}	
NOTE 1 VID(AC) specifies the input differential voltage V _{TR} -V _{CP} required for switching, where V _{TR} is the "true" input signal and V _{CP} is the "complementary" input signal. The minimum value is equal to V _{IH} (AC) - V _{IL} (AC).			

Table 4.1-9 — Differential Signals Cross Point (1.2 V VccQ)

Parameter	Symbol	Min.	Max.	Unit
AC differential input cross point ¹	V _{IX}	0.5*V _{CCQ} - 0.12	0.5*V _{CCQ} +0.12	V
AC differential output cross point ²	V _{OX}	0.5*V _{CCQ} - 0.15	0.5*V _{CCQ} +0.15	
NOTE 1 The typical value of V _{IX} is expected to be about 0.5 * V _{CCQ} of the transmitting device and V _{IX} (AC) is expected to track variations in V _{CCQ} . V _{IX} (AC) indicates the voltage at which differential input signals must cross.				
NOTE 2 V _{OX} shall be guaranteed only after ZQ calibration completed.				

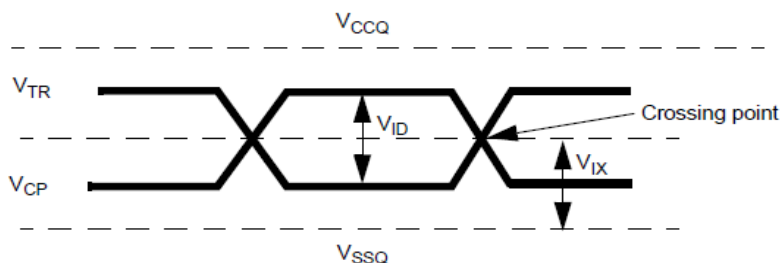


Figure 4.1-1 — Differential Signal Levels

4.1.2 NAND DQ Rx Mask Specifications

The DQ input receiver (Rx) mask defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and is not the valid data-eye. The DQ Rx mask for voltage and timing is shown in the figure below and is applied per individual DQ pin. The DQ Rx mask is evaluated at the die pads.

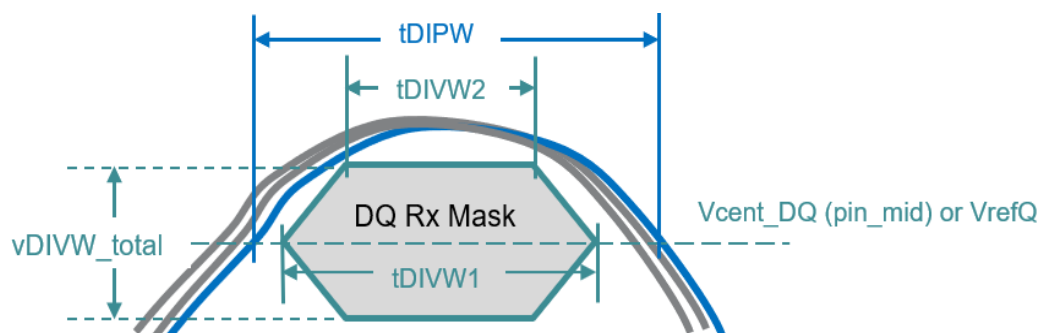


Figure 4.1-2 — DQ Rx Mask Definition

Table 4.1-10 — NAND CTT Interface Rx Mask Specifications

Interface	Parameter	Symbol	<1200 Mbps	1200 Mbps	1600 Mbps, 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps, 2800 Mbps, 3200 Mbps	3600 Mbps	Unit
CTT	DQ Rx Mask Voltage Total	vDIVW_total	N/A	N/A	200	180	140	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) or VrefQ ¹	tDIVW1	N/A	N/A	0.48	0.48	0.48	UI
	DQ Rx Mask Timing ² Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	tDIVW2	N/A	N/A	0.30	0.30	0.30	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid) or VrefQ	tDIPW	0.62	0.66	0.66	0.66	0.66	UI
NOTE 1 Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used.								
NOTE 2 At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.								

4.1.2 NAND DQ Rx Mask Specifications (cont'd)

Table 4.1-11 — NAND LTT Interface Rx Mask Specifications

Interface	Parameter	Symbol	<1200Mbps	1200 Mbps, 1600 Mbps, 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Unit
LTT	DQ Rx Mask Voltage Total	vDIVW _{total}	160	160			120	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	tDIVW1	0.48	0.48			0.48	UI
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW _{total} /2	tDIVW2	0.30	0.30			0.30	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid)	tDIPW	0.62	0.66			0.66	UI

4.1.3 Controller DQ Rx Mask Specifications

The Controller DQ RX Mask specifications in this section are applicable to controllers that support the data rates listed in Table 4.1-12 and Table 4.1-13.

Table 4.1-12 — Controller CTT Interface Rx Mask Specifications^{1,2,3}

Interface	Parameter	Symbol	2000Mbps, 2200Mbps, 2400Mbps,	2800Mbps, 3200Mbps	3600Mbps	Unit
CTT	DQ Rx Mask Voltage Total	vDIVW _{total}	180	180	140	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) or VrefQ	tDIVW1	0.40	0.40	0.40	UI
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW _{total} /2	tDIVW2	0.25	0.25	0.25	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid) or VrefQ	tDIPW	0.50	0.50	0.50	UI
NOTE 1 Vcent_DQ (pin_mid) shall be replaced by VrefQ in the case where External VrefQ is used or Internal VrefQ without Vref training is used. NOTE 2 At 1600Mbps, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate. NOTE 3 System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.						

4.1.3 Controller DQ Rx Mask Specifications (cont'd)

Table 4.1-13 — Controller LTT Interface Rx Mask Specifications¹

Interface	Parameter	Symbol	2000Mbps, 2200Mbps, 2400Mbps	2800Mbps, 3200Mbps	3600Mbps	Unit
LTT	DQ Rx Mask Voltage Total	vDIVW_total	160	160	120	mV
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	tDIVW1	0.40	0.40	0.40	UI
	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) $\pm$ vDIVW_total/2	tDIVW2	0.25	0.25	0.25	UI
	DQ Input Pulse Width at Vcent_DQ (pin_mid)	tDIPW	0.50	0.50	0.50	UI
NOTE 1 System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.						

4.1.4 Vcent_DQ (pin_mid) Definition

Vcent_DQ (pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given NAND die.

Each Vcent_DQ is defined by the center (i.e., widest opening) of the cumulative data input eye as depicted in Figure 4.1-3.

Since the DQ Rx mask is centered around Vcent_DQ (pin_mid), any pin-to-pin Vcent_DQ variation must be accounted for in the DQ Rx Mask.

Similarly, Vcent_RE_t, Vcent_RE_c, Vcent_DQS_t, and Vcent_DQS_c are defined by the center of the cumulative data input eye for RE_t, RE_c, DQS_t and DQS_c respectively. Vcent_RE_t and Vcent_RE_c are collectively denoted as Vcent_RE. Vcent_DQS_t and Vcent_DQS_c are collectively denoted as Vcent_DQS.

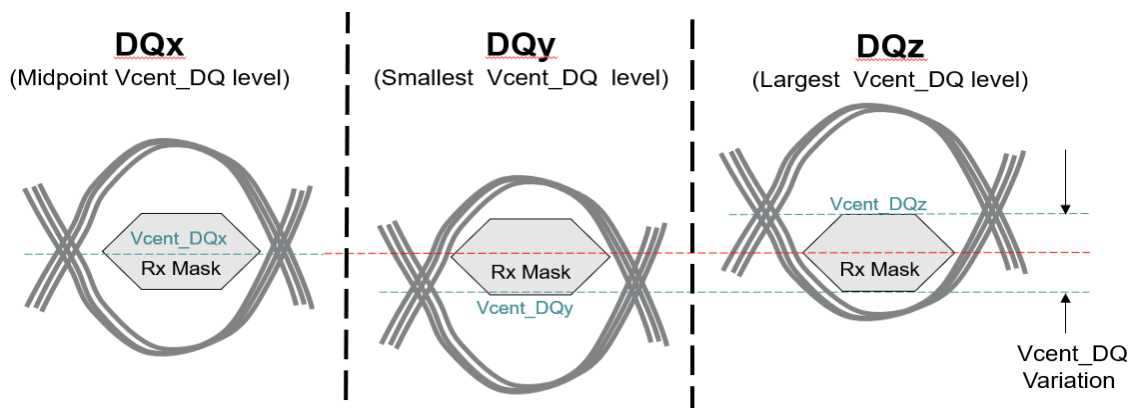


Figure 4.1-3 — Vcent_DQ (pin_mid) Definition

4.1.5 CTT and LTT Interface (1.2 V VccQ) VIHL_AC Definition

The minimum DQ AC input pulse amplitude (pk-pk) is given by the VIHL_AC specification.

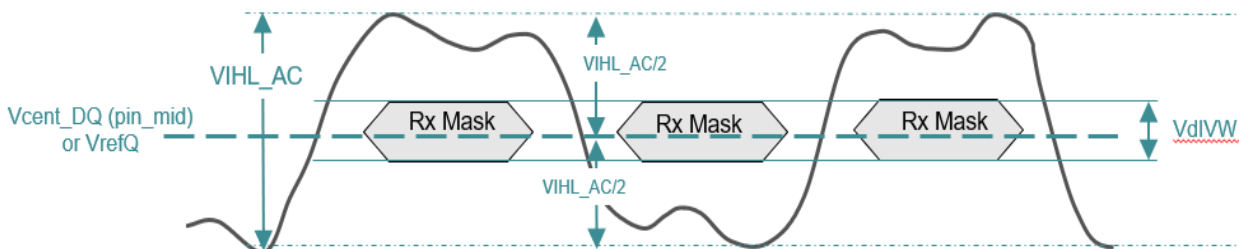


Figure 4.1-4 — VIHL_AC Definition

Table 4.1-14 — VIHL_AC CTT and LTT Interface (1.2 V VccQ) Specifications

Parameter	Symbol	Interface	Up to 1800 Mbps	2000 Mbps, 2200 Mbps, 2400 Mbps	2800 Mbps, 3200 Mbps	3600 Mbps	Notes	Unit
DQ AC input pulse amplitude pk-ok	VIHL_AC_CTT	CTT	220			190	1, 2, 3	mV
	VIHL_AC_LTT	LTT	200			170		
NOTE 1 The DQ only input pulse amplitude must meet or exceed VIHL_AC at any point over the total UI, except when no transitions are occurring for that UI.								
NOTE 2 VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). For CTT interface, Vcent_DQ (pin_mid) is replaced by VrefQ as the center reference level in the case where External VrefQ is used or Internal VrefQ without Vref training is used.								
NOTE 3 There are no timing requirements above or below VIHL_AC levels.								

4.1.6 NAND Minimum Internal VrefQ Allowable Range

Table 4.1-15 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Internal VrefQ Value1 and Value2 Settings (1.2 V VccQ)

Interface	Parameter	Symbol	Min	Max	Notes	Unit
CTT	Minimum allowable range upper limit	VrefQ_CTT_HI	-	55%	1, 2, 3	VccQ
	Minimum allowable range lower limit	VrefQ_CTT_LO	45%	-		
LTT	Minimum allowable range upper limit	VrefQ_LTT_HI	-	40%		VccQ
	Minimum allowable range lower limit	VrefQ_LTT_LO	160	-		mV
NOTE 1	The host shall not set the NAND internal VrefQ to a setting beyond the allowable range even during Write Training Internal VrefQ training.					
NOTE 2	These specs define the allowable range for NAND internal VrefQ settings but do not represent the needed settings for high speed operations. The needed settings for high-speed operations are obtained from either NAND vendor recommendation or through Internal VrefQ Training.					
NOTE 3	Some NAND device may offer a wider allowable range. See vendor datasheet.					

Table 4.1-16 — NAND Minimum Internal VrefQ Allowable Range for NAND Devices that Support Value3 Settings (1.2 V VccQ)

Interface	Parameter	Symbol	Min	Max	Notes	Unit
CTT	Minimum allowable range upper limit	VrefQ_CTT_HI	-	55%	1, 2, 3	VccQ
	Minimum allowable range lower limit	VrefQ_CTT_LO	45%	-		
LTT	Minimum allowable range upper limit	VrefQ_LTT_HI	-	31.75%		VccQ
	Minimum allowable range lower limit	VrefQ_LTT_LO	160	-		mV
NOTE 1	The host shall not set the NAND internal VrefQ to a setting beyond the allowable range even during Write Training Internal VrefQ training.					
NOTE 2	These specs define the allowable range for NAND internal VrefQ settings but do not represent the needed settings for high speed operations. The needed settings for high-speed operations are obtained from either NAND vendor recommendation or through Internal VrefQ Training.					
NOTE 3	Some NAND device may offer a wider allowable range. See vendor datasheet.					

4.2 Output Specifications

4.2.1 Output Drive and ODT Strengths

4.2.1.1 Combo Interface Devices CTT Drive Strengths

Table 4.2-1— CTT Interface Allowed Pull-Down and Pull-Up Drive Strengths

$R_{ONPD}, R_{ONPU}^{1,2}$	
[ohm]	Unit
25	RZQ/12
37.5 (Recommended Default)	RZQ/8
42.9	RZQ/7
50	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
NOTE 1 For R_{ONPD} and R_{ONPU} values, 37.5Ω and 50Ω are mandatory while the rest are vendor specific.	
NOTE 2 With ZQ Calibration, R_{ONPD} and R_{ONPU} tolerance from the nominal value (when measured at 0.5*VccQ pad voltage) is ±15%	

4.2.1.2 Legacy CTT-Only Devices Interface Drive Strengths

The device may be configured with multiple driver strengths with 'SET FEATURE' command. There are Underdrive (i.e., 50 Ohm), Nominal (i.e., 35 Ohm or 37.5 Ohm), Overdrive 1 (i.e., 25 Ohm) and Overdrive 2 (i.e., 18 Ohm) options. A NAND device supports Nominal and Underdrive as mandatory, and Overdrive1 and Overdrive2 as optional.

Table 4.2-2 — DQ Driver Strength Settings

Setting	Driver Strength
Overdrive 2	18 Ohms (Optional)
Overdrive 1	25 Ohms (Optional)
Nominal	35 Ohms or 37.5 Ohms
Underdrive	50 Ohms

4.2.1.3 LTT Interface Drive Strengths

4.2.1.3.1 LTT Interface Pull-Down

Table 4.2-3 — LTT Interface Allowed Pull-Down Drive Strengths

R_{ONPD}	
[ohm]	Unit
25	RZQ/12
37.5 (PDDS Location2 Default)	RZQ/8
42.9	RZQ/7
50 (PDDS Location1 Default)	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
NOTE 1 For R_{ONPD} values, 37.5 Ω and 50 Ω are mandatory while the rest are vendor specific. NOTE 2 With ZQ Calibration, R_{ONPD} tolerance from the nominal value is $\pm 15\%$ (when measured at a pad voltage of VOH_{nom}). NOTE 3 The default value when PDDS bit locations are in Location1 (see Feature Address 22h) is 50 Ω while the default value when PDDS bit locations are in Location2 (see Feature Address 10h) is 37.5 Ω. NOTE 4 Since the default output pull-down drive strength values may be different among NAND vendors, the NAND LTT pull-down shall be configured by the host to the desired value prior to enabling the LTT interface.	

4.2.1.3.2 LTT Interface Pull-Up

Table 4.2-4 — Allowable VOH_{nom} Configurations

$VOH_{pu,nom}$	VOH_{nom} (mV) @1.2 V V_{ccQ}	Min	Nom	Max	Unit
$V_{ccQ}/3$ (default)	400	0.85	1.0	1.15	VOH_{nom}
$V_{ccQ}/2.5$ (optional)	480	0.85	1.0	1.15	VOH_{nom}
NOTE 1 $VOH_{pu,nom} = V_{ccQ}/3$ is mandatory and shall be the default, while $VOH_{pu,nom} = V_{ccQ}/2.5$ is optional. NOTE 2 VOH_{nom} accuracy requirements are after ZQ calibration NOTE 3 VOH_{nom} accuracy requirements only apply at valid CH_ODT values					

4.2.1.3.2 LTT Interface Pull-Up

Table 4.2-5 — Allowable CH_ODT Configurations

Rtt		VOHpu,nom	
[ohm]	Unit	VccQ/3	VccQ/2.5
25	RZQ/12	Valid	Valid
37.5	RZQ/8	Valid	Valid
42.9	RZQ/7	Valid	Valid
50	RZQ/6	Valid (default)	Valid
60	RZQ/5	Valid	Valid
75	RZQ/4	Valid	Valid
100	RZQ/3	Valid	Valid
150	RZQ/2	Valid	Valid
300	RZQ/1	Valid	Valid
NOTE 1 Support for CH_ODT value of 50Ω when VOHpu,nom = VccQ/3 is mandatory and shall be the default setting. Support for other CH_ODT values is vendor specific. NOTE 2 Support for VOHpu,nom = VccQ/2.5 is optional. When VOHpu,nom = VccQ/2.5 is supported by a device the CH_ODT configurations that are supported as well as the default value are vendor specific.			

4.2.1.4 CTT and LTT Interface ODT

Table 4.2-6 — Allowable NAND ODT Rtt Values for CTT and LTT Interfaces

Rtt	
[ohm]	Unit
25	RZQ/12
37.5	RZQ/8
42.9	RZQ/7
50	RZQ/6
60	RZQ/5
75	RZQ/4
100	RZQ/3
150	RZQ/2
300	RZQ/1
Disabled (Default)	N/A
NOTE 1 The default value of ODT Rtt = Disabled is mandatory, while the ODT Rtt values supported by a device is vendor specific.	

Table 4.2-7 — ODT Accuracy Specifications

Interface	VOUT	Min	Nom	Max	Notes	Unit
CTT	VIL(AC) to VIH(AC)	0.85	1.0	1.67	1,2,3	RZQ/n
LTT	0.1*VccQ	0.75	1.0	1.15	3	
	0.33*VccQ	0.85	1.0	1.15		
	0.5*VccQ	0.85	1.0	1.35		
NOTE 1	On CTT interface, for data rates where Rx mask is not used, VIL(AC) = VIL.DQrel (AC) and VIH(AC) = VIH.DQrel (AC)					
NOTE 2	On CTT interface, for data rates where Rx mask is used, VIL(AC) = Vcent_DQ(pin_mid) – VIH_AC/2 and VIH(AC) = Vcent_DQ(pin_mid) + VIH_AC/2.					
NOTE 3	All values are after ZQ Calibration.					